



AN 907: Enabling 5G Wireless Acceleration in FlexRAN

for the Intel® FPGA Programmable Acceleration Card N3000



Online Version



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AN-907

ID: **683275**

Version: **2020.09.10**

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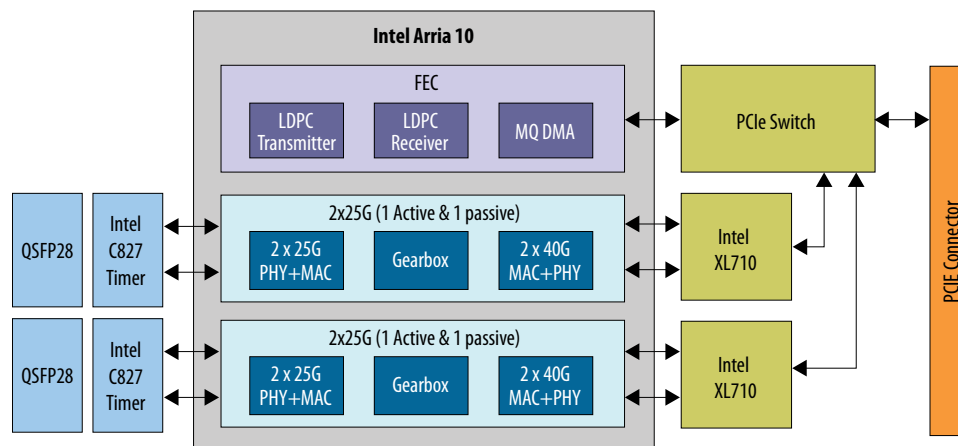
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1. About the 5G Wireless Acceleration Reference Design

The 5G Wireless Acceleration reference design provides IP (Intel FPGA IP and software drivers) to support fronthaul IO and 5G channel coding (forward error correction (FEC)).

The Intel FPGA PAC N3000 provides an on-board PCIe switch that connects fronthaul and 5G channel coding functions to a PCIe Gen3x16 edge connector. The Intel FPGA PAC N3000 is a general-purpose acceleration card for networking.

Figure 1. Data flow for the user image, FEC, and Fronthaul IO



1.1. 5G User Image Features

FEC features:

- Functionality independent of 25G I/O (look-aside model).
- Support for one physical function (PF) and 8 virtual functions (VFs) simultaneously accessing acceleration.
- 64 queues supported equally split between uplink and downlink.
- Multiqueue high-performance DMA
- Hybrid automatic repeat request (HARQ) block
- LDPC transmitter with interleaving and rate matching.
- LDPC receiver with de-interleaving function and reverse rate matching.
- Load balancer distributes the pending requests to transmitter and receiver.

- Early termination CRC24B.
- Software enablement by baseband device (bbdev) API (targeted to upstream to Data Plane Development Kit (DPDK).
- Function-level reset.

Fronthaul IO features:

- 25G MAC and 25G PHY IP connectivity to retimer and a quad small form factor pluggable (QSFP28).
- 40G MAC and 40G PHY IP connectivity to Intel XL710 networking device.
- Gearbox to enable 25G connectivity to QSFP28.
- IEEE 1588 PTP support.
- Software enablement by Open Platform Acceleration Environment (OPAE), DPDK and bbdev.

Related Information

- [5G LDPC-V Intel FPGA IP User Guide](#)
- [IEEE 1588 V2 Test: Intel FPGA Programmable Acceleration Card N3000](#)

1.2. About the Intel PAC N3000

You enable the Intel PAC N3000 through six main firmware components. Intel also provides a software package for the Intel PAC N3000. Intel creates and maintains five of these firmware components, are not specific to the user image or application you run on the N3000. These firmware components manage the board management control and factory image and the interface configuration (PCIe and Ethernet).

The Intel PAC N3000 supports a user image. A remote system update (RSU) capable page (page 1) in an on-board 1 Gb flash stores the user image. A non-RSU capable page (page 0) of the same 1 Gb flash stores a fail over factory image..

Intel develops and owns all of the following Intel PAC N3000 components (including all updates) except the Intel® Arria® 10 flash page 1 user image:

- Intel MAX® 10 Nios flash.
 - Fixed configuration.
 - RSU capable.
 - Intel loads the binary image.
- PCIe software.
 - Intel flashes the binary images.
 - Fixed configuration for PCIe configuration.
 - Not RSU capable.
- Intel C827 retimer.
 - Intel flashes the binary EEPROM.
 - Power-up configuration initialization by Intel Arria 10 soft Nios processor through Intel MAX 10.
 - Fixed configuration for transceiver.
 - Encrypted.
- Intel XL710.
 - Intel flashes the binary images.
 - Fixed configuration for transceiver configuration.
 - RSU capable.
- Intel Arria 10 flash factory image page 0.
 - Intel flashes the binary images.
 - Not RSU capable.
- Intel Arria 10 flash page 1 user image.
 - RSU capable.
 - Intel provides the top-level reference design under a software license agreement.
 - Contains multiple encrypted IP blocks provided under a software license agreement.
 - You own the production image and design.

Related Information

- [Intel® FPGA PAC N3000 AFU Developer Guide](#)
- [Intel® FPGA PAC N3000 Data Sheet](#)
- [Security User Guide: Intel FPGA Programmable Acceleration Card N3000](#)
- [Intel Acceleration Stack User Guide: Intel FPGA Programmable Acceleration Card N3000](#)

1.2.1. Factory Image for 2x2x25 GbE

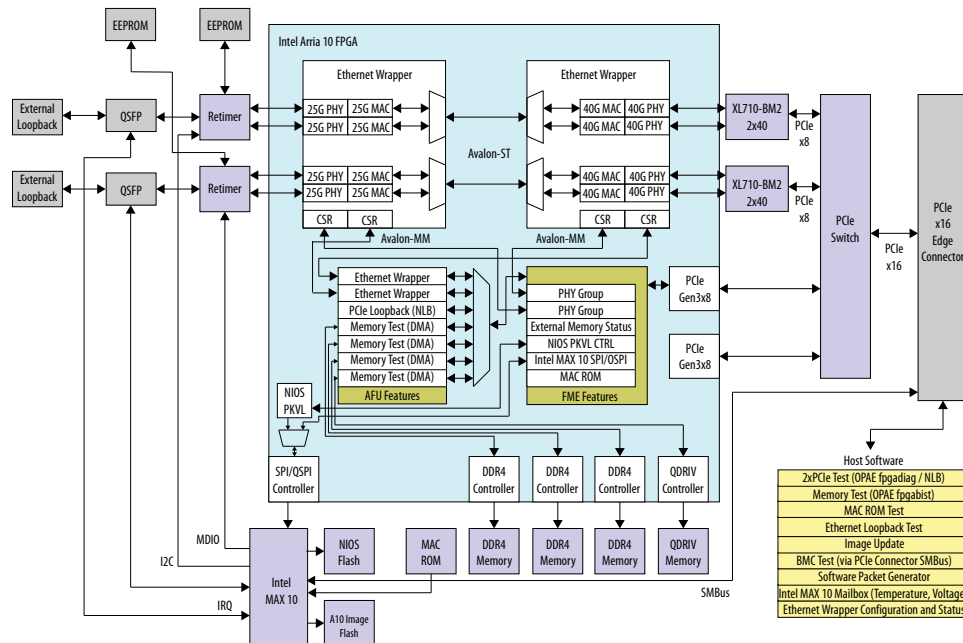
Page 0 of the flash contains the factory image. This image tests and diagnoses the Intel PAC N3000.

The factory image:

- Tests the image that enables PCIe, Ethernet, and memory diagnostics:
 - PCIe near-end loopback testing
 - Memory testing using DMA reads and writes
 - Ethernet loopback test
- Enables the RSU for the user image in flash

If the user image update fails, the Intel PAC N3000 restarts with the factory image, you can then reload the user image.

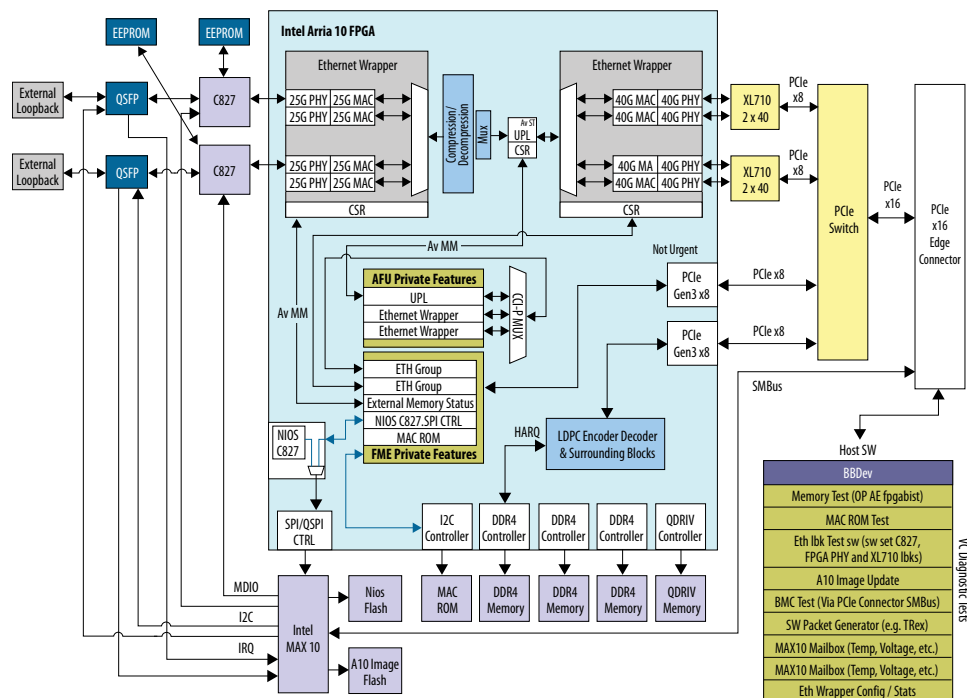
Figure 2. Factory Image Block Diagram for 2x2x25 GbE



2. 5G User Image Description

The user image performs fronthaul IO and 5G channel coding. Contact Intel for the user image.

Figure 3. 5G User Image



2.1. User Image Power Management

On-board power monitoring restricts the board temperature to 100°C. In the event of reaching this limit, the board is automatically shut down. The user image power consumption and thermal profile must fit within this envelope.

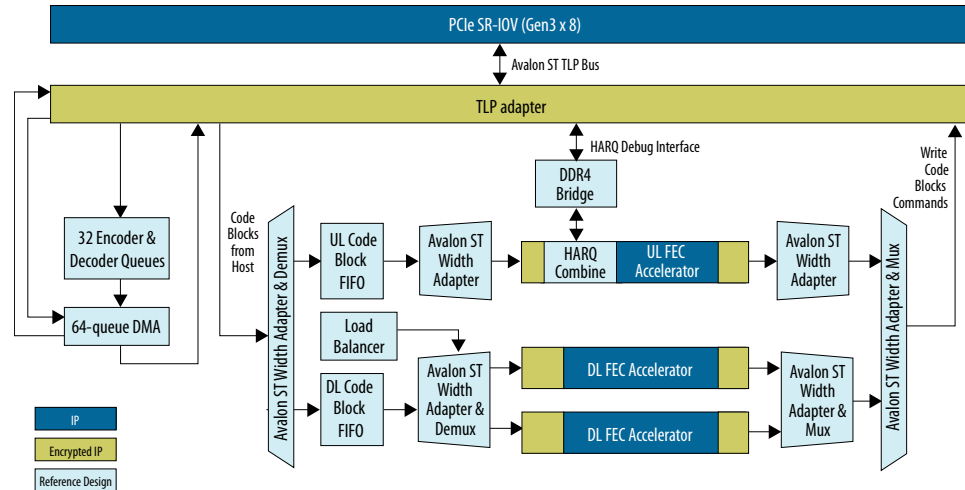
For different situations with different functions, the power consumptions are different. As a reference point, the raw power consumption of the FPGA for the 5G user image is about 60 W @ 100°C junction temperature. The Intel PAC N3000 card power consumption is about 100 W.

2.2. 5G Channel Coder

Send and receive code blocks for the encoder and decoder over PCIe to or from the host using the descriptor format defined in the Data Plane Development Kit (DPDK) and the baseband device. Contact Intel for the descriptor format.

The channel coders queue and process these blocks based on the load balancing decisions.

Figure 4. 5G Channel Coder



The downlink FEC accelerator consists of the 5G LDPC-V transmitter and the uplink FEC accelerator consists of the 5G LDPC-V receiver. The input to the downlink FEC accelerator is 32-bit data and the output data is 32-bit wide. For more information on the 5G LDPC-V transmitter and receiver, refer to the *5G LDPC-V Intel FPGA IP User Guide*.

Figure 5. Transmitter Signals

This figure does not show the Avalon streaming interface signals

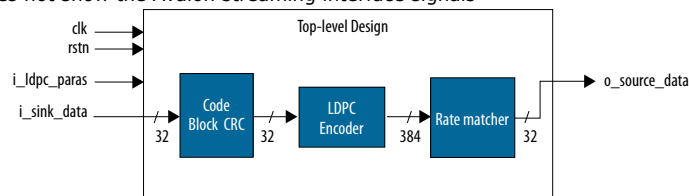
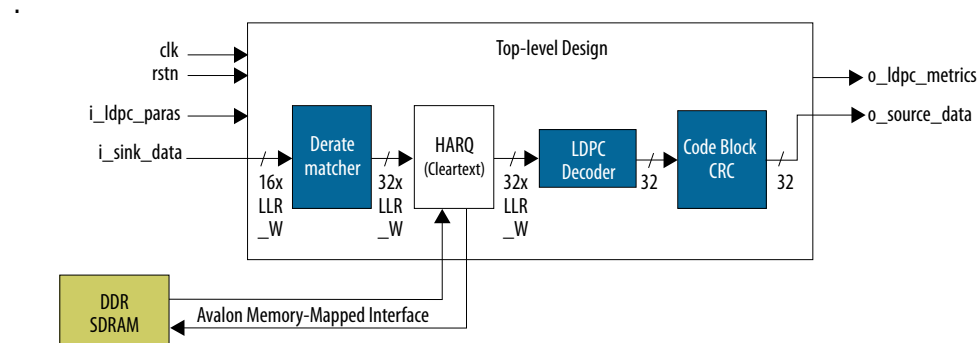


Figure 6. Receiver Signals

This figure does not show the Avalon streaming interface signals



Related Information

- [Data Plane Development Kit Website](#)
- [Baseband Device Library](#)
- [5G LDPC-V Transmitter Signals](#)
- [5G LDPC-V Receiver Signals](#)
- [5G LDPC-V Intel FPGA IP User Guide](#)

2.2.1. 5G Channel Coder Throughput

The Intel FPGA PAC N3000 5G channel coder accelerator contains two encoders and one decoder. The throughput depends on the traffic model.

For a single encoder, the clock rate, code block size (base graph number, lifting factor), code rate affect the throughput.

Figure 7. Downlink throughput for BG1

The figure shows the downlink throughput with different parameters for BG1 (2 encoder engines).

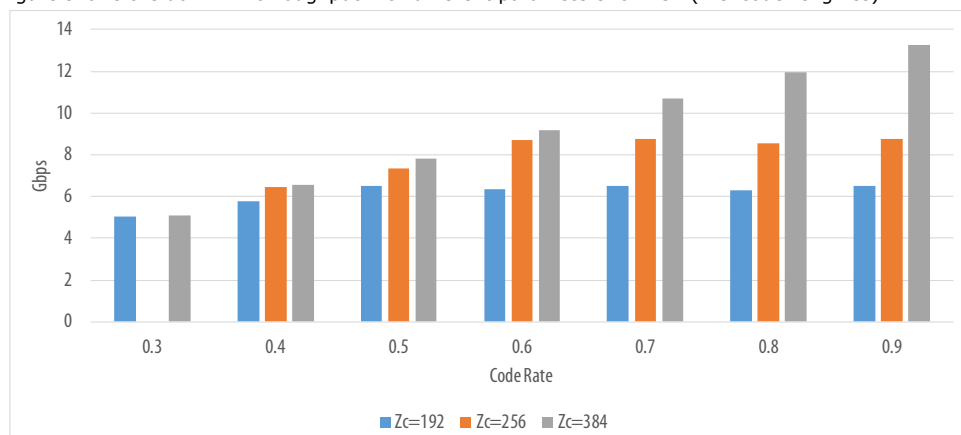
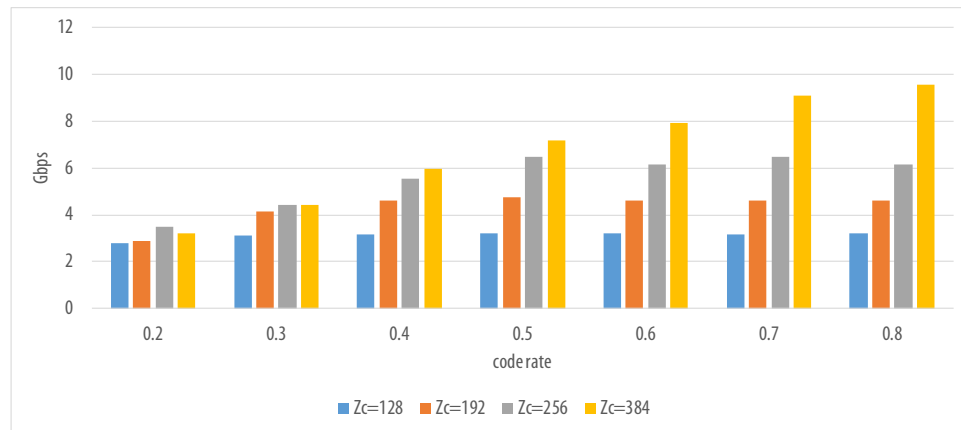


Figure 8. Downlink throughput for BG2

The figure shows the downlink throughput for BG2 with different parameters (2 encoder engines).



For a single decoder, the clock rate, code block size (base graph number, lifting factor), code rate, and iteration number affect the throughput.

Figure 9. Uplink throughput for BG1

The figure shows the uplink throughput with different parameters for BG1 (iteration number is 6).

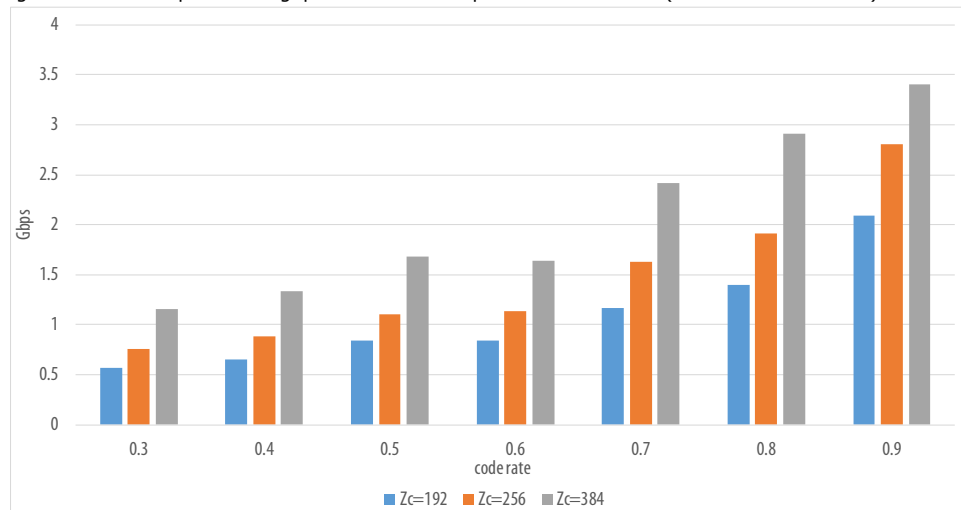
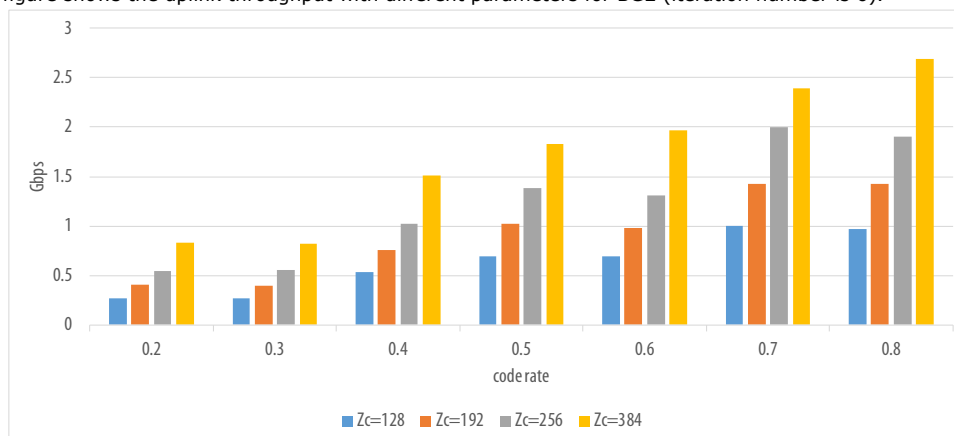


Figure 10. Uplink throughput for BG2

The figure shows the uplink throughput with different parameters for BG2 (iteration number is 6).



2.2.2. 5G LDPC-V Transmitter and Receiver Test Cases

The tables show some test case examples of the LDPC transmitter and receiver, not a complete list. Each test case uses different values or sizes for base graph, Zc value, K' value, code rate, Qm, E value, k0 value, ON/OFF code block CRC

Table 1. Test Cases for the Downlink

test case	BG	Zc	K'	Code Rate	Qm	E	K0	CRC
0	0	10	184	1/3	1	300	0	ON
1	0	20	400	1/2	4	520	0	ON
2	0	40	800	3/4	4	900	600	ON
3	0	10	184	8/9	1	260	180	OFF
4	0	4	88	2/3	1	80	0	OFF
5	0	5	104	2/3	4	100	120	OFF
6	1	240	2352	1/2	1	2800	0	ON
7	1	256	2520	1/3	2	3200	2048	ON
8	1	9	88	1/3	8	96	117	ON
9	1	80	720	1/3	8	864	1200	OFF

Table 2. Test Cases for the Uplink

test case	BG	Zc	K'	Code Rate	Qm	E	K0	CRC
0	0	10	216	1/3	2	280	330	ON
1	0	20	440	1/2	6	504	440	ON
2	0	40	880	3/4	6	882	0	ON
3	0	10	216	8/9	2	240	0	OFF
4	0	4	80	2/3	2	80	32	OFF

continued...

5	0	5	96	2/3	6	102	0	OFF
6	1	240	2400	1/2	6	2802	0	ON
7	1	256	2560	1/3	4	3200	256	ON
8	1	9	80	1/3	8	96	54	ON
9	1	80	800	1/3	8	840	1600	OFF

Related Information

5G LDPC-V Intel FPGA IP User Guide

2.2.3. 5G VRAN Universal Verification Methodology

The vRAN universal verification methodology (UVM) simulation test environment for the 5G channel coder incorporates the transmitter or receiver and the DMA subsystem. The test environment does not include the preverified transaction layer packet (TLP) adapter.

The tests randomly select 2,000 test patterns from 110,000 test patterns to test the decoding function and randomly selects 2,000 test patterns from 110,000 test patterns to test the encoding function. The tests also test the randomization (and functional coverage) of system scenarios such as HARQ, physical and virtual function (PF and VF) access, queue flushing, and reset. The reference design includes the UVM test plan, 5G_LDPC_Test_Plan.xls.

Figure 11. UVM Tests

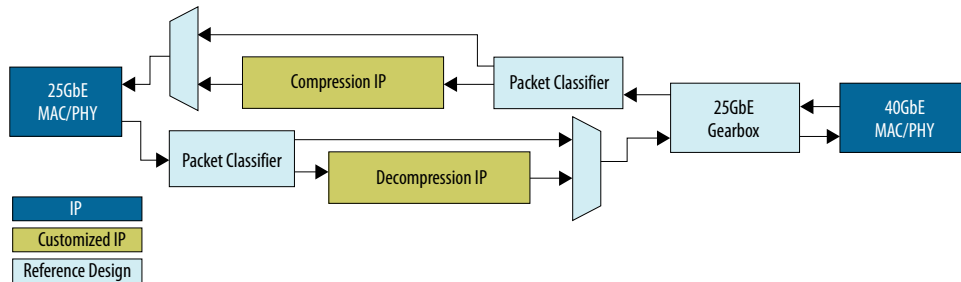
Coverage Matrix		Verification Requirements
Sect Title	Description	Constraints
1 Register		
1.1 access property	RW : read-write RO : read-only W1C : write 1 to clear detail refer to sect2.9 in design spec	Based on reg field operation. Every reg field will be tested in PF side. Besides, static configuration reg fields 'vf queue flush status write back address' and regs 'ring control registers' will also be tested in each VFs side, because they support VF write.
1.2 static configuration registers	Every field in this registers can be configured by PF, and they are read only in each VFs side, except 'queue flush status write back address' related fields. 'queue flush status write back address' related fields can be configured by each VFs and PF. detail refer to sect2.9.1 in design spec	Write reg fields with random value by each VFs and PF, and then read them back by each VFs and PF. (The read data (except 'queue flush status write back address' related fields) should match the write data by PF (based on access property). The read data of 'queue flush status write back address' related fields should match the write data by the same Fid
1.3 queue mapping registers	Every field in these registers can be configured by PF, and they are read only in each VFs side. detail refer to sect2.9.2 in design spec	configure the registers to map the queue to random Fid by PF, read them back by each VFs and PF for check. PF: read data should match the write data VFx: read data should be 'hfff...fff'. set static configuration register field 'Queue-PF/VF mapping done' to 1, and then read Queue mapping registers back by each VFs and PF for check. PF: read data should match the write data VFx: read data should equal the queue ID if this queue is assigned to VFx, otherwise, the read data should be 'hfff...fff'. repeat above operations to make sure each Queue has been mapped to each

2.3. Fronthaul IO

The user image fronthaul IO is a simple passthrough pipe between 40GbE with 1588/PTP and 25GbE with 1588/PTP.

You can add customized IP based on the packet process between 40GbE and 25GbE, e.g. compression and decompression IPs for O-RAN.

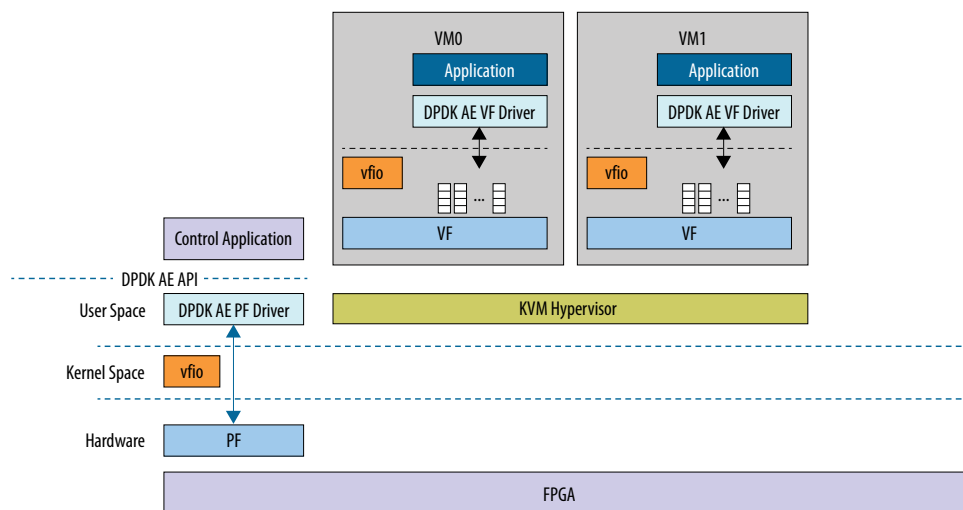
Figure 12. Fronthaul IO



2.4. User Image Software

The user image requires software components and drivers, which support the descriptor format and physical function drivers. The user image software supports the DPDK BBDev API, FlexRAN, and OS/Orchestration.

Figure 13. User Image Architecture



3. Document Revision History for AN 907: Enabling 5G Wireless Acceleration in FlexRAN for the Intel® FPGA Programmable Acceleration Card N3000

Document Version	Changes
2020.09.10	<ul style="list-style-type: none">Added figures to <i>5G Channel Coder Throughput</i>.Updated <i>Receiver signals</i> figure.Updated <i>Factory Image for 2x2x25 GbE</i>.Removed <i>O-RAN Compression and Decompression</i>
2020.01.30	Initial release.