The Video Waveform Generator comprises several tools for analysing the content of a video signal.

**Figure 1. Block diagram of the Video Waveform Generator Intel FPGA IP Solution**

### Summary

An IP solution comprising of a Waveform Engine and associated IP blocks creates and overlays four popular waveforms onto the original video at the output. The available tools are; color component waveforms, a chrominance vectorscope, a CIE color chart and color component histograms. You can customise the specifics of the analysis and the arrangement of the overlay and create your own measurement graticules.

### Functional Description

The IP Solution consists of several sub-cores which handle video processing, memory, and control. The video datapath includes a color space converter (CSC), a frame buffer, a video crosspoint, and a waveform engine. Initially, the input video passes to a color space converter block, which is arranged to receive YUV- or RGB-formatted video and output a large bus combining YUV and RGB color spaces. In order to correctly calculate the values for the different color spaces, you need to indicate the input sampling format via the I²C control interface.

When the values for all color spaces are calculated, the video passes to the waveform engine which performs the required analysis and draws the waveforms. These waveforms are then combined with the original video and the graticule which is stored in the frame buffer. User graticules and labels are transferred via the I²C control interface described below. A video crosspoint at the output allows you to bypass the overlay and pass video through with no modifications.
Key Features

- Simple Clocked Video input and output
- Simple control using I²C interface commands
- Small FPGA resource footprint (Approximately 42K ALUTS, 68K Registers, 198 DSPs, 500 M20Ks)
- Low latency (Less than 2 video lines)
- Supports image resolutions up to 4096x2160 P60
- Waveform tile
- Vectorscope tile
- Histogram tile
- CIE chart tile
- Up to 4 tiles displayed at the same time
- User defined tile sizes
- User defined lookup table (LUT) and color space conversion tables
- User downloadable graticules

The WFM Solution is controlled entirely via an I²C command interface. It is intended that a host processor sends commands to the WFM Solution to display and configure each waveform tile. Each command is decoded by the WFM Solution and actioned. The I²C host interface provides diagnostic and status information back to the host for monitoring purposes.

The framebuffer overlay is alpha-blended (RGBA/YUVA) to provide live mixing of graticules, custom annotations, menus or any other graphics on the video stream. All graphics overlay data is user-generated and downloaded over the I²C interface. The video-frame-buffer is provided for end user customization. Graphics elements / fonts are not provided.

An external DDR Memory interface is required. The WFM Solution uses a 512bit Memory Mapped interface to DMA to/from external memory and the WFM engine during operation. The External memory is used to store the history data that is required to deliver the high-quality persistence & decay visualisations. Each Waveform Tile has an 8-bit granularity in pixel-depth delivering a very rich and detailed waveform image seen in broadcast quality waveform monitors.

Figure 2. Raw waveform tiles before adding user graticules
Applications
- Video monitor display
- Video router signal monitoring
- Multi-viewer signal monitoring

Design Example
An example of the use of the Waveform Generator Solution is available on an HDMI-based design implemented on an Intel Arria® 10 GX FPGA Development Kit equipped with a Bitcmedia HDMI 2.0 FMC. A block diagram of the design is shown in Figure 3.

The input to the Solution connects to the HDMI IP core configured as a receiver. The output of the Solution (carrying the input video overlaid with analysis waveforms) connects to an HDMI core configured as a transmitter.

An Intel External Memory Interface (EMIF) is instantiated and connects to the waveform solution's memory-mapped Avalon interface to connect to memory on the reference board.

A softcore Nios II processor is instantiated in the example design and controls the Solution via its I²C interface. A JTAG interface allows a host PC to communicate with the Nios II during runtime. This is optional and can be omitted from customer designs if required.

Recommended Device and Speed Grade
The Video Waveform Generator Intel FPGA IP Solution is compatible with the Intel Arria® 10 device family.

Figure 3. Example implementation with HDMI in and out

Figure 4. Example of overlaid video