Intel® 500 Series Chipset Family Platform Controller Hub (PCH)

Specification Update

Revision 002

May 2021

Document Number: 635220-002

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Contents

Tables

Revision History

Document Number	Revision Number	Description	Revision Date
635220	001	• Initial Release	March 2021
635220	002	• Added Q570 and W580 in Table 2-1	May 2021

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1 Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents table. This document is a compilation of device and document errata and specification clarifications and changes. It is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into the specification update and are no longer published in other documents. This document may also contain information that has not been previously published.

1.1 Affected Documents

Document Title	Document Number
Intel® 500 Series Chipset Family Platform Controller Hub (PCH) Datasheet, Volume 1 of 2	635218
Intel® 500 Series Chipset Family Platform Controller Hub (PCH) Datasheet, Volume 2 of 2	636174

1.2 Nomenclature

Errata are design defects or errors. Errata may cause the behavior of the PCH to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present in all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

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2 Identification Information

2.1 Marking

Table 2-1. PCH Lines Component Identification

PCH Stepping	Top Marking (S-Spec)	Notes
B1	SRKM2	Desktop / Workstation Intel® Chipset H510
B1	SRKM5	Desktop / Workstation Intel® Chipset B560
B1	SRKM6	Desktop / Workstation Intel® Chipset H570
B1	SRKM3	Desktop / Workstation Intel® Chipset Z590
B1	SRKM4	Desktop / Workstation Intel® Chipset Q570
B1	SRKM7	Desktop / Workstation Intel® Chipset W580

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3 Summary Tables of Changes

The following tables indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the product. Intel may fix some of the errata in a future stepping of the component and account for the other outstanding issues through documentation or specification changes as noted. These tables use the following notations:

3.1 Codes Used in Summary Table

Stepping	Description
X	Erratum exists in the stepping indicated. Specification Change that applies to the stepping indicated.
(No mark) or (Blank Box)	This erratum is fixed or not applicable in listed stepping or Specification Change does not apply to listed stepping.

Status	Description
Doc	Document change or update that is implemented.
Planned Fix	This erratum may be fixed in a future stepping of the product.
Fixed	This erratum has been previously fixed in Intel® hardware, firmware, or software.
No Fix	There are no plans to fix this erratum.

3.2 Errata Summary Table

Erratum ID	Stepping	Errata
	B0	
1	No Fix	Intel Trace Hub Pipe Line Empty
2	No Fix	SATA Enclosure Management LED Messaging
3	No Fix	eSPI SBLCL Register Bit Not Cleared by PLTRST#
4	No Fix	S0ix Entry When Connecting an USB-C* Power Adapter
5	No Fix	PCIe Clock Maximum Rising/Falling Edge Rate and VCROSS
6	No Fix	Integrated GbE Controller Reset on D3 Exit
7	No Fix	xHCI Link Protocol Field Value - USB 3.2 Gen 1x2 and 2x2
8	No Fix	USB VTIO Device Capabilities Field Length
9	No Fix	xHCI Force Header Command

3.3 Specification Changes

No.	Specification Changes
	No specification changes for this revision of the specification update.

3.4 Specification Clarifications

No.	Specification Clarifications
	No specification clarification for this revision of this specification update.

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4 Errata Details

1	Intel Trace Hub Pipe Line Empty
Problem	The Intel Trace Hub Pipe Line Empty bit (CSR_MTB_BAR, Offset 0xD4) for a given output port may be set while the Input Buffer Empty for the associated output port is not set. This will only happen when the captureDone signal is de-asserted by clearing the ForceCaptureDone bit (CSR_MTB_BAR, Offset 0xD8) is cleared or the StoreQual[0] signal is de-asserted by the Trigger Unit before the pipe line is empty, and the destination is either system memory or USB (DCI).
Implication	There may be valid trace data in the trace source input buffer which did not get sent to the destination (output port).
Workaround	None identified. CaptureDone should be cleared or de-asserted after the pipe line is empty.
Status	For the steppings affected, refer to the Summary Table of Changes.

2	SATA Enclosure Management LED Messaging
Problem	When sending a SATA enclosure LED message and all SATA ports are either idle or disabled, the PCH may not transmit the LED message due to an internal clock gating issue.
Implication	The LED status for SATA enclosure may be incorrect.
Workaround	None identified. Enclosure Management SW can poll the Enclosure Management (EM_CTL) - Offset 20h bit 8 register for a 0 value immediately before writing LED messages.
Status	For the steppings affected, refer to the Summary Table of Changes.

3	eSPI SBLCL Register Bit Not Cleared by PLTRST#
Problem	The IOSF-SB eSPI Link Configuration Lock (SBLCL) bit (offset 4000h, bit 27 in eSPI PCR space) is reset by RSMRST# assertion instead of PLTRST# assertion.
Implication	If the SBLCL bit is set to 1, software will not be able to access the eSPI device Capabilities and Configuration register in the reserved address range (0h - 7FFh) until RSMRST# asserts.
Workaround	If software needs to access the eSPI device reserved range 0h - 7FFh while SBLCL bit is set to 1, a RSMRST# assertion should be performed.
Status	For the steppings affected, refer to the Summary Table of Changes.

4	S0ix Entry When Connecting an USB-C* Power Adapter
Problem	Connecting a USB-C* power adapter to a PCH USB port may cause a race condition that can prevent the system from entering S0ix. This issue only occurs on designs where the USB-C Power Delivery (PD) implements Out Of Band (OOB) messaging to communicate with the PCH for port mapping.

Implication	The system may fail to enter S0ix.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

5	**PCIe Clock Maximum Rising/Falling Edge Rate and VCROSS**
Problem	The PCIe Clock Output signals (CLKOUT_PCIE_P/N) may not meet the maximum Rising/Falling Edge Rate and VCROSS specifications as defined in the PCI Express Card Electromechanical Specification Revision 3.0, section 2.1.3, REFCLK AC Specifications.
Implication	There are no known functional failures due to this erratum.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

6	**Integrated GbE Controller Reset on D3 Exit**
Problem	Upon GbE controller D3 exit, the GbE host driver performs a controller reset. During this reset, software accesses to the GbE MMIO registers may not complete.
Implication	The system may hang. Note: This erratum has only been observed in a synthetic environment.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

7	**xHCI Link Protocol Field Value - USB 3.2 Gen 1x2 and 2x2**
Problem	The xHCI Host Controller reports the value of 0h for the Link Protocol (LP) bits [15:14] in register XECP_SUPP_USB3_6 (MMIO offset 8038h) and XECP_SUPP_USB3_7 (MMIO offset 803Ch), which does not meet the xHCI specification revision 1.2.
Implication	There are no known functional failures due to this erratum.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

8	**USB VTIO Device Capabilities Field Length**
Problem	The xHCI spec version 1.2 defines the PCI Express Capability structure offset 04h Device Capabilities (DVSEC) field to be 8 bytes. The USB Virtualization Based Trusted IO (VTIO) Management controller implements the DVSEC field as 12 bytes.
Implication	An USB controller driver may not be able to enable the USB VTIO controller.
Workaround	None identified. To mitigate this erratum, an Independent Software Vendor could account for the field length in the USB controller driver.
Status	For the steppings affected, refer to the Summary Table of Changes.

9	**xHCI Force Header Command**
Problem	When USB 3.2 Gen 2x2 capability is enabled, the xHCI controller fails to execute the Force Header Command.
Implication	xHCI CV TD4.12 - Force Header Command Test may report an error. Note: The Force Header Command is only used by the USB-IF Command Verifier (xHCI CV) tool for device testing. There are no known functional failures due to this erratum.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

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5 Specification Changes

There are no specification changes in this revision of the Specification Update.

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6 Specification Clarification

There are no specification clarifications in this revision of the Specification Update.

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