

# **Dynamic LED Backlight Control and Debug on Embedded Display Port (eDP) Panels using PWM Control Techniques**

**White Paper**

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***November 2016***

***Ajit Kumar K. P  
Graphics Platform Application Engineer  
Internet of Things Group, Intel***



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## Contents

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<b>1.0</b>	<b>Revision History .....</b>	<b>4</b>
<b>2.0</b>	<b>Executive Summary.....</b>	<b>5</b>
2.1	Terminology .....	5
2.2	Overview of eDP Backlight Brightness Control.....	6
2.2.1	Controlling eDP Panel Backlight Brightness using Pulse Width Modulation.....	6
2.2.2	Controlling PWM Signals using Backlight PWM Control Registers .....	7
2.2.3	Display Configuration of the Platform .....	8
2.2.4	Setting Up PWM Backlight Control Parameters during POST using Intel Binary Modification Program (BMP).....	9
2.3	Backlight Control Techniques.....	11
2.3.1	Using UEFI Shell Commands in VBIOS or GOP Mode.....	11
2.3.2	Decoding Backlight PWM Control Registers .....	13
2.3.3	Using the Intel® In-Target Probe (ITP) .....	14
2.3.4	Using the Power Options Settings in the Windows Operating System.....	14
2.3.5	Using other VBIOS and GOP Method .....	16
2.4	PWM Signal Debug and Verification using an Oscilloscope.....	16
2.4.1	Verifying the Values of the Backlight PWM Control Register .....	17
2.4.2	Changing the Values of the Backlight PWM Control Register .....	17
<b>Appendix A</b>	<b>.....</b>	<b>19</b>

## Figures

Figure 1.	eDP Panel Brightness Control Using the Duty Cycle of the PWM Signal.....	7
Figure 2.	Dynamic eDP Panel Brightness by Varying the ON Period of the Duty Cycle .....	7
Figure 3.	Bakersport CRB eDP Port C to eDP Panel Pin Connection.....	10
Figure 4.	Backlight Control Parameters in VBT.....	11
Figure 5.	Display Panel Brightness Setting in Windows.....	15
Figure 6.	Color Enhancements Setting in Intel Graphics Control Panel .....	16
Figure 7.	Pin Out Details of the eDP Port on a Typical Intel CRB .....	19
Figure 8.	Pin Out Details of the eDP Panel Connector .....	19

## Tables

Table 1.	Terminology .....	5
Table 2.	Backlight PWM Control Registers Description.....	9



## 1.0 *Revision History*

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Date	Revision	Description
November 2016	001	Initial release.

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## 2.0 Executive Summary

This paper presents techniques that use Pulse Width Modulation (PWM) for controlling and debugging the backlight brightness on embedded DisplayPort (eDP) displays connected to computing platforms powered by Intel processors.

The Intel® Atom™ processor has the ability to dynamically control the backlight brightness of eDP panels using Pulse Width Modulation (PWM). This feature is used in many embedded systems such as Point of Sale (POS) and In-Vehicle Infotainment (IVI) systems where the display brightness is dynamically adjusted depending on the ambient light.

As such, the eDP VESA specifications include the following techniques to dynamically control the backlight brightness of eDP panels:

- Using Pulse Width Modulation (PWM)
- Using AUX channel to control the DPCD registers (eDP v1.2 and higher)

Generally on Intel platforms, dynamic eDP backlight brightness control is implemented using the PWM technique via Intel graphics drivers, Graphics Output Protocol (GOP) in UEFI BIOS, and Video BIOS (VBIOS) in legacy BIOS.

**Note:** All references in this document refer to the Bay Trail platform. Other platforms may have different display configurations and register definitions.

## 2.1 Terminology

**Table 1. Terminology**

Term	Description
BAR	Base Address Register
BIOS	Basic Input/Output System. The Intel® Embedded Media and Graphics Driver interacts with two BIOS systems: system BIOS and Video firmware (i.e., VBIOS, GOP, and EPOG)
BMP	Binary Modification Program; allows customizing the data in Video BIOS Table
CRB	Customer Reference Board
eDP	Embedded DisplayPort
GOP	Graphics Output Protocol
IGD	Integrated Graphics Device
MMIO	Memory-Mapped I/O
OROM	Option ROM; code that is integrated with the system BIOS and resides on a flash chip on the motherboard. The Intel Embedded Video BIOS is an example of an Option ROM.



Term	Description
PCIe	Peripheral Component Interface Express
POST	Power On Self Test
PWM	Pulse Width Modulation
System BIOS	The standard BIOS used for basic input and output operations on PCs
SOC	System On Chip
SUT	System Under Test
VBIOS	Video Basic Input Output System; a component of system BIOS that drives graphics
VBT	The Video BIOS Table (VBT) is a block of customizable platform-specific data used by the Video BIOS and device drivers such as Flat Panel Timings, OEM definable Mode Timing, GPIO pins, Clock, and more.
VESA	Video Electronics Standards Organization

## 2.2 Overview of eDP Backlight Brightness Control

### 2.2.1 Controlling eDP Panel Backlight Brightness using Pulse Width Modulation

The eDP panel backlight can be dynamically controlled by applying Pulse Width Modulation (PWM) to the power supplied to the eDP panel backlight. To adjust the backlight brightness, the duty cycle of the PWM signal is varied accordingly. The duty cycle is the ratio of ON time compared with the time period of the PWM signal as shown in [Figure 1](#). By adjusting the duty cycle, a precise backlight brightness control can be achieved. This is the primary method in controlling the brightness of the eDP panel backlight.

The terms backlight brightness and duty cycle used in this document are interchangeable and are denoted in percentages. The duty cycle's percentage is a measure of time in which the eDP panel backlight is physically turned on. To achieve maximum or 100% backlight brightness, the duty cycle would be 100% of the PWM signal period. Likewise, to set the backlight brightness to different brightness levels such as 50% (medium brightness) or 10% (low brightness), the duty cycle is adjusted accordingly as shown in [Figure 2](#). The typical parameters that need to be taken into consideration for backlight brightness are the PWM duty cycle, frequency, high-level voltage, and low-level voltage.

Intel graphics drivers and firmware (either GOP or VBIOS) achieve dynamic backlight brightness on eDP panels by controlling the PWM signals that are outputted to the panels. The PWM signals are controlled by programming the Backlight PWM Control Registers in the display adapter (Bus 0, Device 2, Function 0) Memory-Mapped I/O (MMIO) address space.



Figure 1. eDP Panel Brightness Control Using the Duty Cycle of the PWM Signal

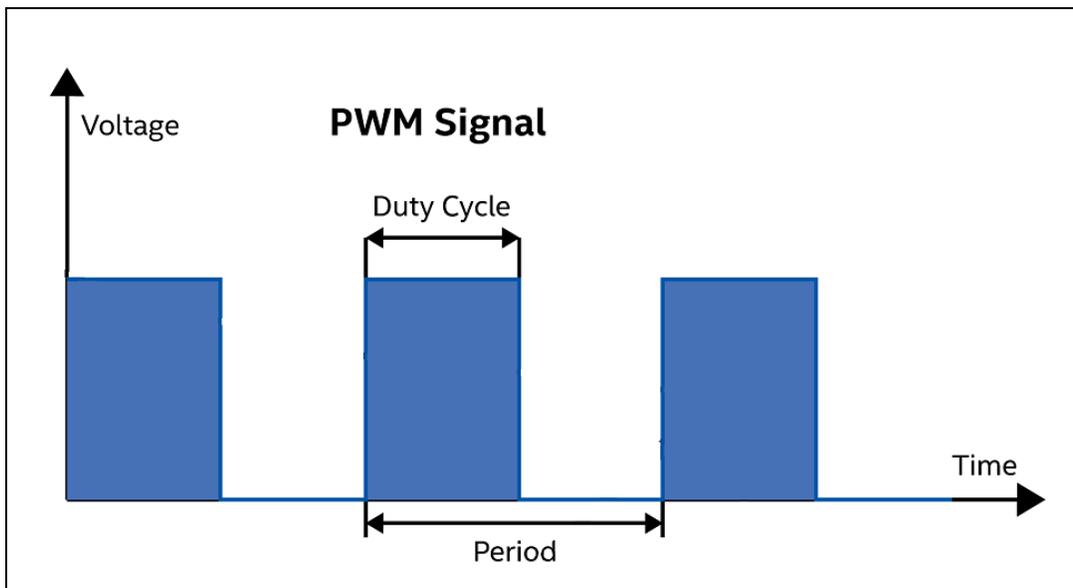
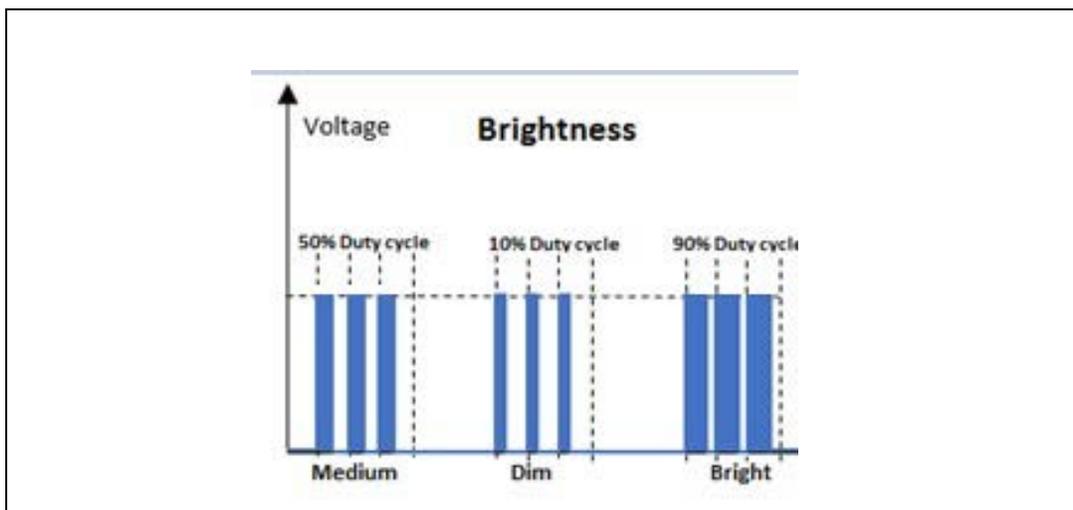


Figure 2. Dynamic eDP Panel Brightness by Varying the ON Period of the Duty Cycle



### 2.2.2 Controlling PWM Signals using Backlight PWM Control Registers

The Pulse Width Modulation (PWM) frequency and duty cycle of the PWM signal supplied to eDP panels are controlled (via graphics driver or firmware) by programming the values in the Backlight PWM Control Registers. The registers—PipeA\_BLC\_PWM\_CTL or PipeB\_BLC\_PWM\_CTL—are selected depending on which display pipe is associated with the eDP port. The Backlight PWM Control Registers' description is shown in Table 2. For further information on Backlight control registers,



refer to [https://01.org/sites/default/files/documentation/intel\\_os\\_gfx\\_prm\\_vol10\\_-\\_display\\_0.pdf](https://01.org/sites/default/files/documentation/intel_os_gfx_prm_vol10_-_display_0.pdf).

The address offset for the PipeA\_BLC\_PWM\_CTL register is 61254h while the address offset for the PipeB\_BLC\_PWM\_CTL register is 61354h. These address offsets will then be referenced with the MMIO base address for Display registers to determine the absolute address. The details for calculating the absolute address are explained in later sections.

**Note:** Since PipeA\_BLC\_PWM\_CTL and PipeB\_BLC\_PWM\_CTL are Memory mapped I/O (MMIO) Registers, 61254h and 61354h are only address offsets and cannot be used to read or write to the registers directly. In order to read or write to these registers, it is necessary to determine and use the absolute address.

### 2.2.3 Display Configuration of the Platform

On any given platform, it is important to understand the display configuration to determine which display pipe and port is associated with the eDP panel. In the case of the Bay Trail platform, the eDP port can be configured as PortB (DDIO) or PortC (DDI1). This can be configured in the Video BIOS Table (VBT) using the Binary Modification Program (BMP) tool.

**Note:** For the Intel Bay Trail Bakersport Customer Reference Board (CRB), the eDP panel port can only be configured as PortC (DDI1).

Furthermore, the boot display algorithm in the VBT determines whether a display device is primary or secondary depending on the type and number of display devices attached to the platform. The display pipe assignment depends on the boot display algorithm. For example, if the eDP panel is the only display device attached to the Bay Trail platform, it will naturally be assigned as the primary display. In order to control the eDP panel backlight, the graphics driver and firmware (VBIOS or GOP) would need to program the PipeA\_BLC\_PWM\_CTL (PipeA Backlight PWM Control Register).

In Clone Display mode, the boot display algorithm will determine whether the eDP panel is assigned as primary or secondary display based on the type of display devices attached. This will in turn determine which display pipe must be used to control the eDP panel backlight. If the eDP panel is set as the primary display, the PipeA\_BLC\_PWM\_CTL register would need to be programmed to control the eDP panel backlight. If the eDP's panel is the secondary display, then the PipeB\_BLC\_PWM\_CTL register would need to be programmed instead.

For the Intel Bay Trail Bakersport CRB, the eDP port is only available at PortC (DDI1). To control the frequency and duty cycle of the PWM signal supplied to the eDP panel, PipeA\_BLC\_PWM\_CTL or PipeB\_BLC\_PWM\_CTL registers are programmed. These registers directly control the frequency and duty cycle of the PWM signal generated at DDI1\_BKLT\_CTRL pin on the Bay Trail System On Chip (SOC). The signal from the DDI1\_BKLT\_CTRL pin is routed to Pin 36 (L\_BRIGHTNESS) on the eDP Port C of the CRB



as shown in Figure 3. The signal passes through the connector cable and connects to Pin 23 (BL\_PWM\_DIM) on the eDP panel connector. For details of the pin out for both connectors, refer to Appendix A.

**Table 2. Backlight PWM Control Registers Description**

Bit	Description
31:16	Backlight Modulation Frequency. The field determines the total number of time-based events in a complete cycle of the modulated backlight control. This is normally set once during the initialization phase based on the frequency of the clock that is being used and the desired PWM frequency. This value represents the period of the PWM stream in the display core clocks ([CTG] 100MHz HRAW clocks multiplied by 128 or 25MHz S0IX clocks multiplied by 16).
15:0	Backlight Duty Cycle. This field determines the number of time-based events for the active portion of the PWM backlight control. The value should not be larger than the backlight modulation frequency value.  A value of zero will turn the backlight off and a value equal to the backlight modulation frequency will set the backlight at maximum brightness. Changing this value will change the brightness of the backlight and will take effect at the end of the current PWM cycle. This value represents the active time of the PWM stream in the display core clock ([CTG] HRAW clock period multiplied by 128 or 25MHz S0IX clocks multiplied by 16).

## 2.2.4 Setting Up PWM Backlight Control Parameters during POST using Intel Binary Modification Program (BMP)

The Pulse Width Modulation backlight control frequency (Hz) and brightness (0-255) parameters, during POST, are typically preset in the Video BIOS Table (VBT) using the Intel BMP. The modified VBIOS or GOP firmware image can then be flashed into the Option ROM (OROM) of the system BIOS. During system POST or startup, the VBIOS or GOP firmware programs the Backlight PWM Control Registers with the values specified in the VBT. By default, the frequency and brightness values in the VBT are set to 200Hz and 255Hz (100%), respectively, as shown in Figure 4. This sets the brightness of the eDP panel to maximum and ensures that the POST screen is clearly visible.

**Note:** The latest BMP tool can be obtained from Intel® Validation Internet Portal (VIP). The following describes the various VBT fields associated with the PWM backlight control:

- Inverter Type: This option sets the backlight control inverter interface type.
  - PWM (Default) – The backlight brightness is controlled by the Intel graphics driver and VBIOS via the integrated PWM solution for the applicable chipsets.
  - None/External – The backlight brightness is controlled by the system BIOS via an external solution.
- Inverter Polarity: This setting specifies the backlight inverter polarity.
  - Normal (Default) – The backlight brightness value of 0 results in minimum brightness while the value of 255 results in maximum brightness.

- Inverted – The backlight brightness value of 0 results in maximum brightness while the value of 255 results in minimum brightness.
- Minimum Brightness: This setting defines the absolute minimum backlight brightness. The graphics driver will never go below the minimum backlight brightness set value. The values must be specified using the normal polarity semantics.
  - 0 (Default)
  - N/A
- POST Backlight Intensity: This setting sets the initial backlight brightness level during POST and is used only by the Video BIOS. This field is configurable with values ranging from 0 to 255. A value of 0 indicates zero brightness while a value of 255 indicates maximum brightness.
  - 255 (Default)
  - N/A
- PWM Inverter Frequency (Hz): This setting specifies the PWM inverter frequency. The frequency range is between 200Hz to 40kHz with support for decimal values.
  - 200Hz (Default)
  - N/A

**Note:** During POST, the GOP or VBIOS uses the frequency and duty cycle values that are preset in the VBT. However, changing the frequency or duty cycle values in GOP or VBIOS will not be retained by the OS. Upon entering the OS, the graphics driver will once again read the default frequency and duty cycle values from the VBT.

**Figure 3. Bakersport CRB eDP Port C to eDP Panel Pin Connection**

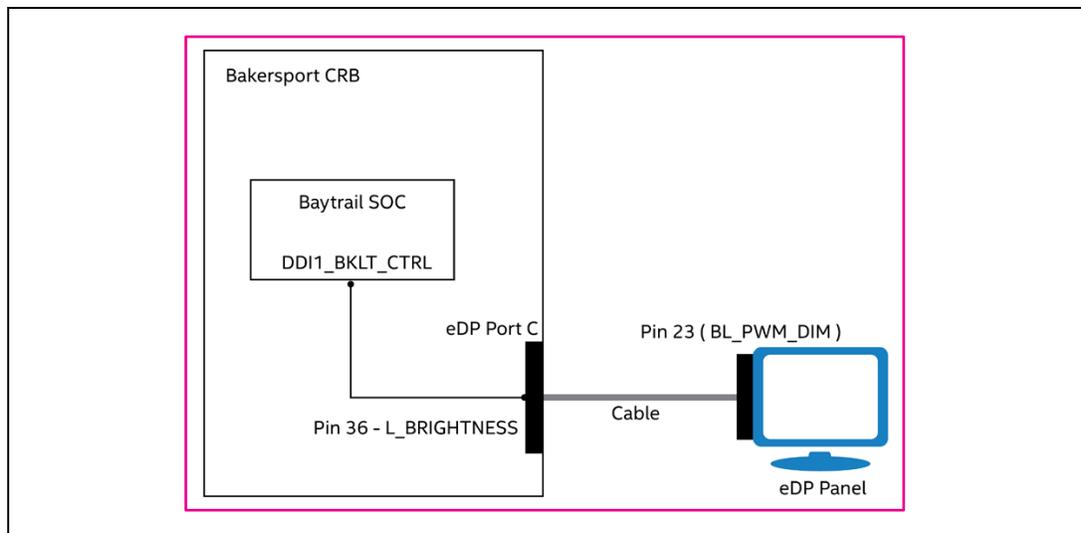
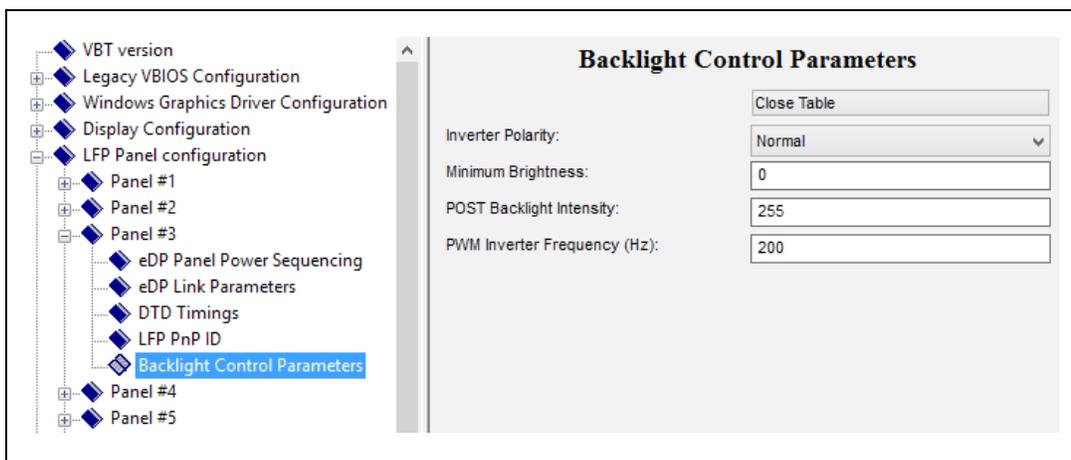




Figure 4. Backlight Control Parameters in VBT



## 2.3 Backlight Control Techniques

The following methods to control the PWM signals have been tested on the Intel® Bay Trail platform.

### 2.3.1 Using UEFI Shell Commands in VBIOS or GOP Mode

**Note:** The MMIO base address is assigned by the system BIOS during startup and this base address varies from one system to another. Even on the same system, the base address can change depending on the number of PCIe devices attached to the system.

1. Boot into the UEFI shell of the System Under Test (SUT) to determine the MMIO Base Address Register (BAR) of the Integrated Graphics Device (IGD) using either of the two UEFI shell commands below.

```
Shell> pci 0 2 0 -i
```



Or,

```
Shell> mm 00020010 -pci -w 4 PCI 0x020010: 0x88000000
```

The value 0x88000000 is the MMIO BAR for IGD.



2. Determine the base address of display registers. For the Bay Trail platform, the display registers reside at an offset of 0x180000 (display register base address) from the IGD BAR. This address is architecturally defined and can be found in the product datasheet:  
<http://www.intel.com/content/dam/www/public/us/en/documents/datasheets/atom-e3800-family-datasheet.pdf>.

**Note:** The address offset for display registers is likely to change from one SOC to another. Please refer the latest product data sheet to obtain the correct value.

The absolute address for the backlight control registers PipeA\_BLC\_PWM\_CTL and PipeB\_BLC\_PWM\_CTL comprises the following:

< IGD MMIO BAR> + <Display Register Base Address> + <Display Register Offset>

Therefore,

PipeA\_BLC\_PWM\_CTL absolute address = 0x88000000 + 0x180000 + 0x61254 = 0x881E1254

PipeB\_BLC\_PWM\_CTL absolute address = 0x88000000 + 0x180000 + 0x61354 = 0x881E1354

3. If eDP is associated with PipeA\_BLC\_PWM\_CTL, use its absolute address to read the PWM frequency and duty cycle with the following command:

```
Shell> mm 881E1254 -mmio -w 4
```

```
MEM 0x881E1254 : 0x14581458
```

The upper and lower DWORD of 0x14581458 represent a 300Hz frequency and 100% duty cycle, respectively. For decoding the DWORD, refer to the [Decoding Backlight PWM Control Registers](#) section.

4. The PWM duty cycle can be changed as shown in the following examples.
  - i. For 300Hz and 25% duty cycle (i.e 0x1458/4), enter the following command:

```
Shell> mm 881E1254 -mmio -w 4 0x14580516
```

- ii. For 300Hz and 50% duty cycle (i.e 0x1458/2), enter the following command:

```
Shell> mm 881E1254 -mmio -w 4 0x14580A2C
```

Change in the brightness levels of the panel should be noticeable in each of the above cases.

5. The PWM frequency can be changed as shown in the following examples.
  - i. For 200Hz and 100% duty cycle, enter the following command:



```
Shell> mm 881E1254 -mmio -w 4 0x1E841E84
```

- ii. For 300Hz and 50% duty cycle (i.e 0x1458/2), enter the following command:

```
Shell> mm 881E1254 -mmio -w 4 0x1E840F42
```

Again, the different levels of the panel backlight brightness should be noticeable.

**Note:** Frequency does not directly affect the panel brightness but instead affects the quality of the backlight. A low frequency value may cause flickering on the panel display.

### 2.3.2 Decoding Backlight PWM Control Registers

For example, the Backlight PWM Control Register contains the DWORD 0x14581458. The upper and lower DWORD represent the frequency and the duty cycle, respectively, i.e 0x1458 is the frequency, and the subsequent 1458 is the duty cycle.

- The PWM frequency (Hz) and duty cycle (percentage) are decoded using the following formulas:

#### Frequency

$$= 25\text{MHz} / (\text{Decimal Value of Upper DWORD} * 16)$$

$$= 25\text{MHz} / (D'[0x1458]*16)$$

$$= 25\text{MHz} / (5208*16)$$

$$= 300\text{Hz}$$

#### Duty Cycle

= A value equal to the backlight modulation frequency value. In this example, the duty cycle with the hexadecimal value of 0x1458 represents 100% duty cycle and a value of zero will turn the back-light off.

**Note:** The duty cycle value must not be more than the frequency value.

Therefore, the DWORD 0x14581458 represents a 300Hz PWM frequency and a 100% duty cycle.

- To decode the PWM frequency and duty cycle from decimal value to hexadecimal value:

Decimal value of the upper DWORD

$$= 25\text{MHz} / (\text{Frequency} * 16)$$

$$= 25\text{MHz} / (300\text{Hz} * 16)$$

$$= 5208$$

Converting the decimal value 5208 to Hex gives the value of 0x1458.



### 2.3.3 Using the Intel® In-Target Probe (ITP)

The advantage of using the ITP DAL commands to control the PWM signal is that the read and write to the hardware registers can be performed in VBIOS, GOP, or OS. In order to use ITP, the Intel® Platform Debug Tool (PDT) needs to be installed on a host system first. Contact your Intel representative for more details on setting up Intel® ITP.

**Note:** The following ITP commands can be run with White cover ITP access.

1. The PWM control registers can be accessed from the ITP command line. For decoding the DWORD, refer to the [Decoding Backlight PWM Control Registers](#) section. To read the PWM frequency and duty cycle from PipeA\_BLC\_PWM\_CTL, use the following commands:

```
>>> itp.halt()  
  
>>> itp.threads[0].mem("0x881E1254", 4)  
  
[32b] 0x14581458
```

The upper and lower DWORD of 0x14581458 represent the 300MHz frequency and 100% duty cycle, respectively.

2. To change the frequency and duty cycle to 400Hz and 50%, respectively:

```
>>> itp.threads[0].mem("0x881E1254", 4, 0x0F4207A1)
```

3. To change the frequency and duty cycle to 400Hz and 25%, respectively:

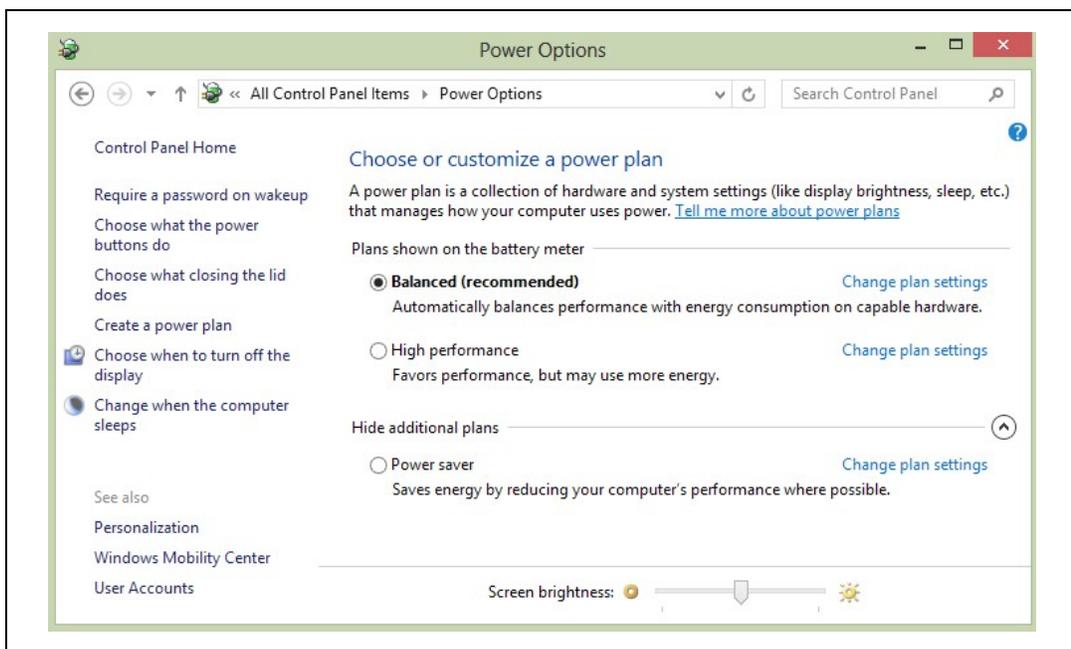
```
>>> itp.threads[0].mem("0x881E1254", 4, 0x0F4203D0)
```

### 2.3.4 Using the Power Options Settings in the Windows Operating System

The eDP panel backlight can also be controlled using the Power Options settings in the Control Panel of the Windows operating system as shown in [Figure 5](#).



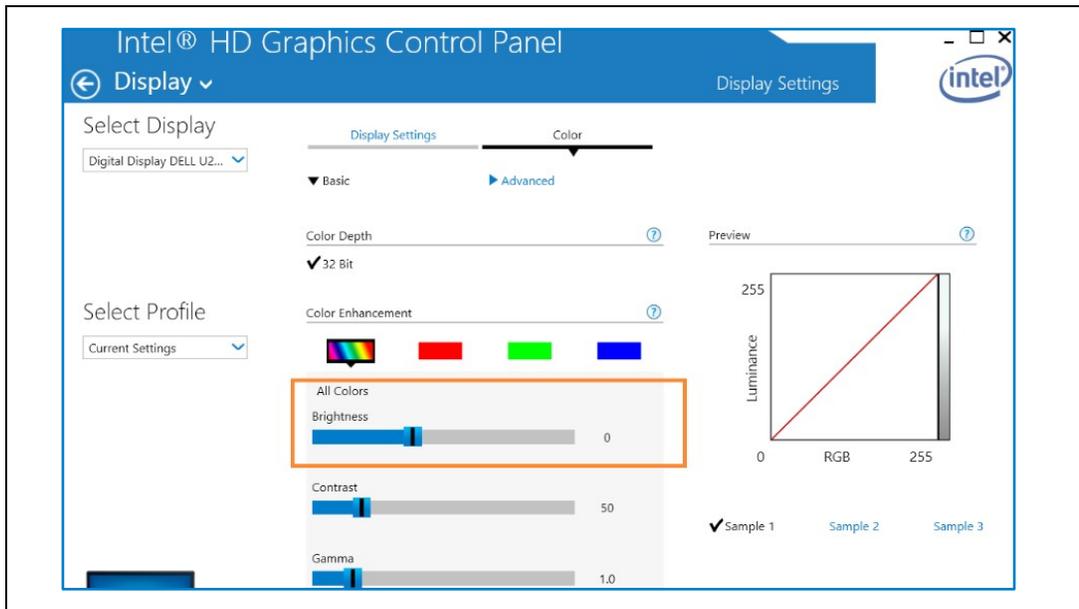
Figure 5. Display Panel Brightness Setting in Windows



The screen brightness setting above represents a 50% duty cycle and can be measured by an oscilloscope. For examples of measuring the display brightness using an oscilloscope, see the [Verifying the Values of the Backlight PWM Control Register](#) section.

**Note:** The highlighted brightness setting in the Intel® HD Graphics Control Panel (see [Figure 6](#)) does not control the eDP backlight. This setting only performs Color Enhancements through RGB/Luminance variation.

Figure 6. Color Enhancements Setting in Intel Graphics Control Panel



### 2.3.5 Using other VBIOS and GOP Method

1. For legacy VBIOS, the display backlight brightness can also be controlled using the INT10h VBIOS function by setting the Backlight Control (5F61h, 08h). The `dobios.exe` can be used in DOS mode to execute VBIOS functions.

**Note:** Contact your Intel representative for more information on VBIOS SPS or the `dobios.exe` tool.

For maximum brightness, use the following command:

```
C:\> dobios 5F61 08FF
```

2. Likewise in GOP mode, the GOP tester tool can also be used to control the backlight brightness.

Change the level of brightness using the following command:

```
>> IntelGopTester.efi -r <value 0 to 255>
```

## 2.4 PWM Signal Debug and Verification using an Oscilloscope

The PWM signals can be captured for debugging and verification purposes by using an oscilloscope. This is achieved by probing the signal at Pin 36 (L\_BRIGTHNESS) on the eDP port of the CRB, or at Pin 23 (BL\_PWM\_DIM) on the eDP panel connector. For details of the pin out for both connectors, refer to [Appendix A](#).



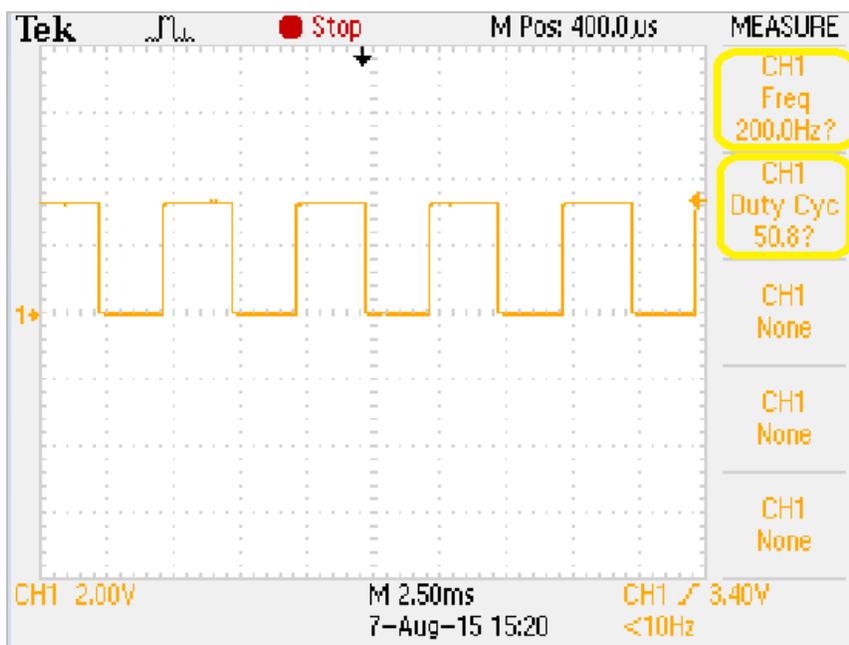
The following examples use ITP commands to configure the PWM signals, which are then captured on an oscilloscope.

### 2.4.1 Verifying the Values of the Backlight PWM Control Register

Enter the following command to show the frequency and duty cycle values in the Backlight PWM Control Registers using ITP commands:

```
>>> itp.threads[0].mem("0x881E1254",4)
[32b] 0x1E840FA0
```

The value 0x1E840FA0 above represents a 200Hz frequency, and a 50% duty cycle. Using an oscilloscope and probing pin 36 (L\_BRIGHTNESS) on the eDP port of the CRB, or at Pin 23 (BL\_PWM\_DIM) on the eDP panel connector produces the signal shown below.

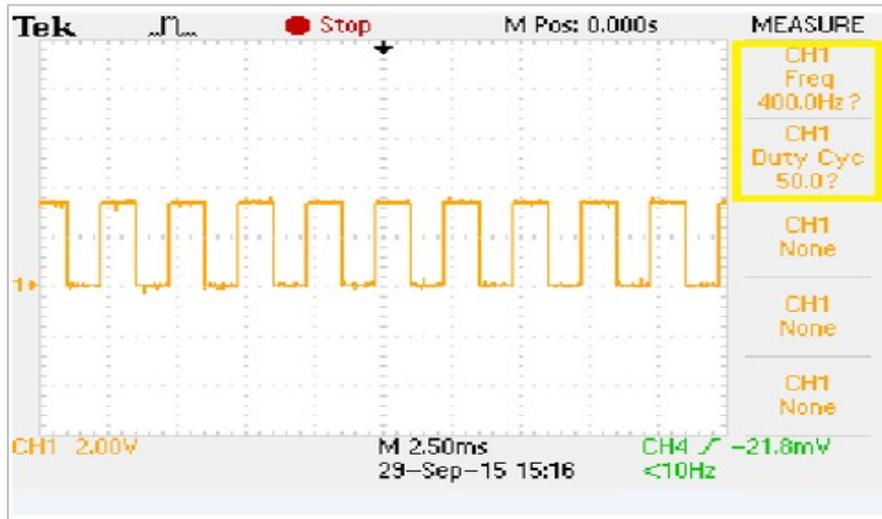


### 2.4.2 Changing the Values of the Backlight PWM Control Register

1. To change the frequency and duty cycle of the PWM signal to 400Hz and 50%, respectively:

```
>>> itp.threads[0].mem("0x881E1254",4,0x0F4207A1)
```

On the oscilloscope, the generated PWM signal appears as follows:



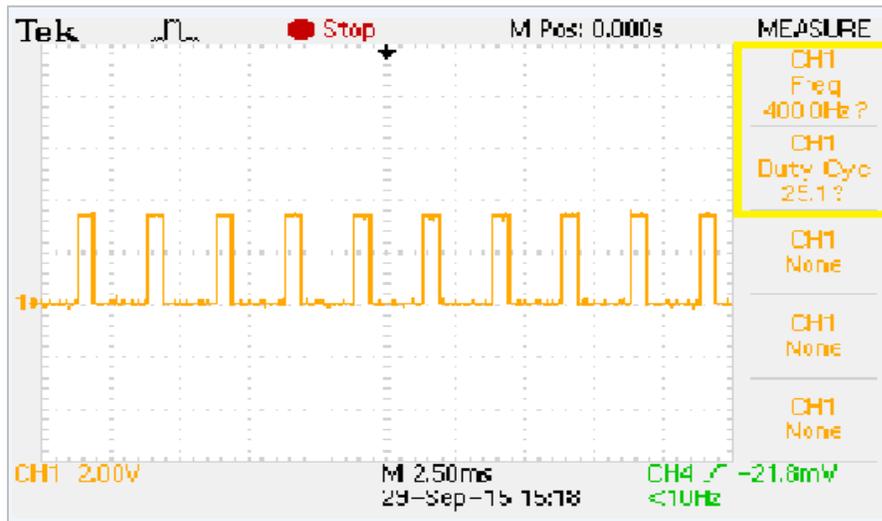
2. To change the frequency and duty cycle to 300Hz and 50%, respectively:

```
>>> itp.threads[0].mem("0x881E1254", 4, 0x14580A2C)
```

3. To change the frequency and duty cycle of the PWM signal to 400Hz and 25%, respectively:

```
>>> itp.threads[0].mem("0x881E1254", 4, 0x0F4203D0)
```

On the oscilloscope, the new PWM signal appears as follows:



**Note:** If there are any discrepancies found between the captured PWM signal and the actual eDP panel brightness display, contact your Intel representative.



## Appendix A

Figure 7. Pin Out Details of the eDP Port on a Typical Intel CRB

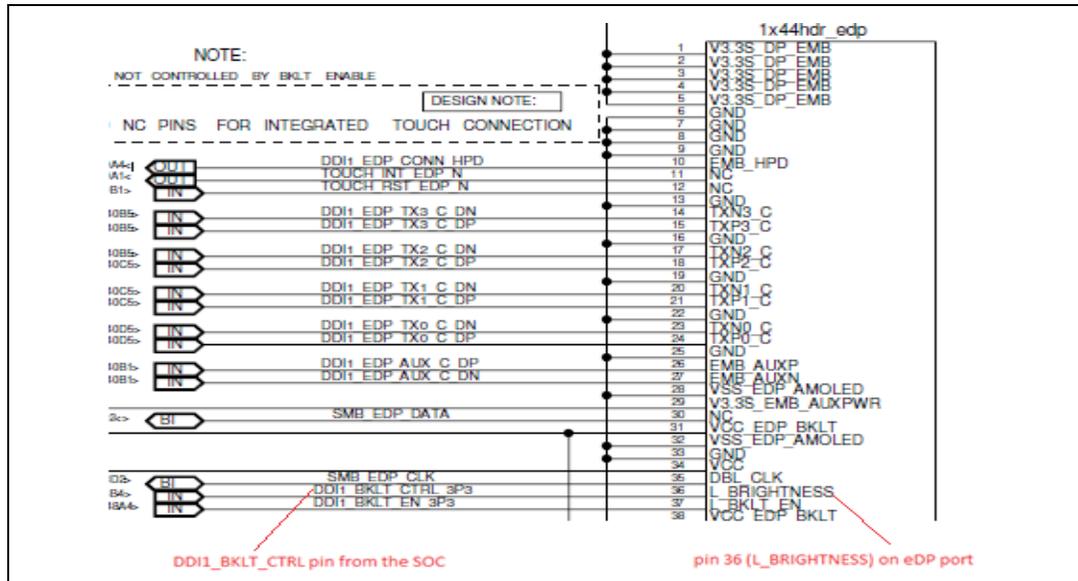


Figure 8. Pin Out Details of the eDP Panel Connector

