

SOLUTION BRIEF

Programmable Solutions
FPGA Video and Vision



Warp FPGA IP

The Intel Warp IP is a highly optimised FPGA IP Core for applying arbitrary warps to a real-time video stream

Summary

The Intel Warp IP is a highly optimised FPGA IP Core for applying arbitrary warps to a real-time video stream of up to 4096 x 2160 pixels and up to 60 frames per second. Maximum image quality is achieved through per-pixel filtering and bi-cubic interpolation on 4:4:4 video data at up to 10-bits per colour plane.

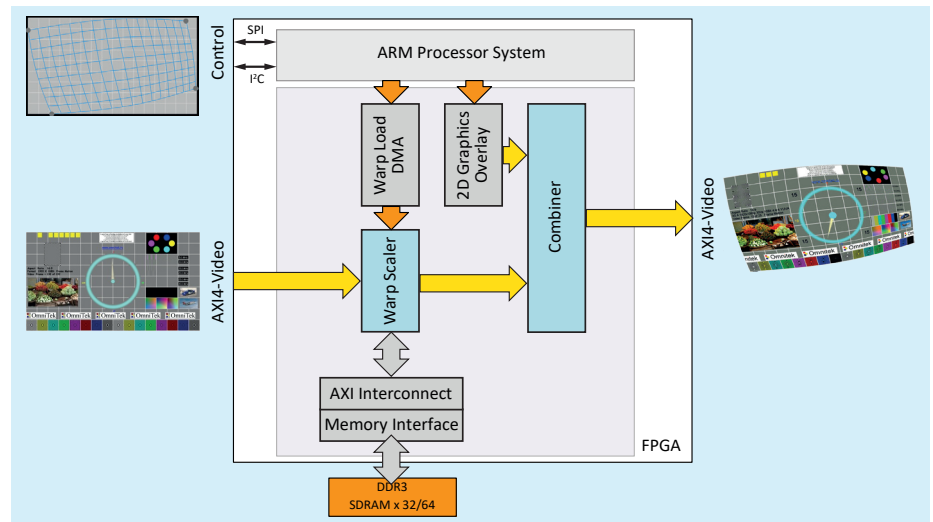


Figure 1. Functional block diagram of Intel's Warp IP solution

The lower diagram on the right illustrates the use of the Intel Warp IP in conjunction with Intel's Image Signal Processor (ISP) and HDR Tonemapping IP to process camera sensor array images. The sensor output is first fed into an ISP pipeline which can crop the image as required, then correct any camera anomalies before it is de-Bayered by the Colour Filter Array block. The image is then passed to our HDR Tone-mapping IP which uses statistical analysis to enhance the image contrast. The image stream is then passed to the Warp Processor to correct for lens distortion and apply any size and shape transformations that are required before the image is output. The system illustrated in the diagram also includes a 2D Graphics Overlay block and a Combiner block to allow graphics to be overlaid on the image.

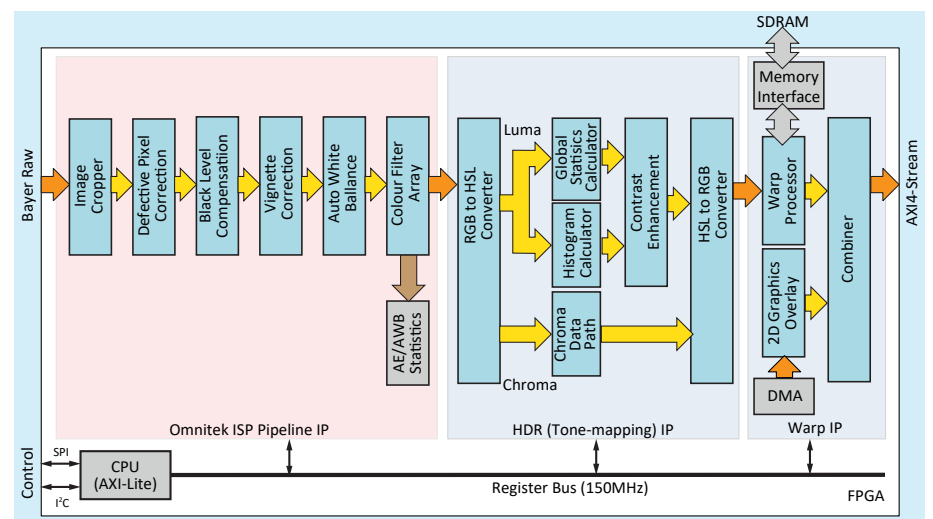


Figure 1. Typical Implementation of the Warp IP in a camera Image Signal Processing Pipeline

Key Features

- Very small resource footprint.
- Low latency (from 1 to 1/6th frame depending on transform).
- Efficient external memory interface.
- Low Pass Filter coefficient sets available for highest filter quality.
- Per-pixel low pass filtering.
- Flexible design using Individual IP Cores such as SDI, HDMI 2.0, LVDS and V-by-One to suit design and component constraints.
- Optional support for image sizes up to 4096 x 2160 at frame rates up to 60 fps.
- Full data buffering to allow input and output to operate in different clock domains.
- Fully compatible with other Intel IP, such as the ISP IP and OSVP IP Suite, via AXI4-Stream to provide a comprehensive image processing package.

Applications

The Warp IP can be used in a range of applications including:

- Projectors. See Projector IP data sheet
- 2D and 3D Image Capture & Projection
- Projection on to curved or distorted surfaces
- Camera lens distortion correction. See ISP IP data sheet
- Virtual Reality Head Sets
- Image Stitch. See Image Stitch IP data sheet
- Digital Signage
- Overlay of interactive graphical and web content
- Multiple input format support, via multiple input cores

Video Input/Output Formats

The Warp Processor Core can process video formats up to 4096x2160 resolution at 60Hz:

- 10-bit, RGB, 4:4:4 processing
- 8, 10 and 12-bit, 4:2:0, 4:2:2 and 4:4:4 processing when used in conjunction with Omnitek Scalable Video Processor (OSVP)



Intel provides these materials as-is, with no express or implied warranties.

All products, dates, and figures specified are preliminary, based on current expectations, and are subject to change without notice.

Intel, processors, chipsets, and desktop boards may contain design defects or errors known as errata, which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Intel technologies' features and benefits depend on system configuration and may require enabled hardware, software or service activation. Performance varies depending on system configuration. No product or component can be absolutely secure. Check with your system manufacturer or retailer or learn more at <http://intel.com>.

Some results have been estimated or simulated using internal Intel analysis or architecture simulation or modeling, and provided to you for informational purposes. Any differences in your system hardware, software or configuration may affect your actual performance.

Intel and the Intel logo are trademarks of Intel Corporation in the United States and other countries.

*Other names and brands may be claimed as the property of others.

© Intel Corporation

- Up to 600MHz pixel rate
- Support for 90° rotation of 2160x3840 input

Requirements

The Warp IP requires an ARM processor to provide real-time user interface Warp mesh updates (twice per second).

The Warp IP requires externally connected SDRAM. Typically a 64-bit wide @1.6GHz data rate (minimum), FFG package, 512MBytes. The ARM requires a 32 or 16-bit wide RAM @1066MHz minimum.

In addition to the optional IP Cores, the Warp Processor includes the following IP blocks to ensure the correct transfer of data from one optional IP core to another.

An optional **Input Rx** Core allows the connection of SDI, DisplayPort 1.2, HDMI 2.0, LVDS or TTL inputs.

An optional **Output Tx** Core allows the connection of SDI, DisplayPort 1.2, HDMI 2.0, V-by-One, LVDS or TTL outputs.

IP Sub Blocks

The **Warp Scaler** block manipulates the image either using high level instructions such as rotate, keystone, barrel or a mesh mapping from the **Warp load DMA** block. The input image is stored and manipulated in external SDRAM via the **AXI Interconnect**.

The **Combiner** block combines the Warped image from the **Warp Scaler** block with a 2D Graphic display from the **2D Graphics Overlay** block to create a combined image.

The **DMA Controller** provides efficient memory control and arbitrates between ARM processor and Warp memory usage.

Transforms

The Warp IP allows the input image to be transformed using a number of controls to perform:

- Fish-eye, barrel and general lens/screen distortion
- Keystone and pin-cushion correction
- Resizing and Rotation
- Perspective mapping
- Arbitrary Warps within 0.5x to 2x local scaling limit