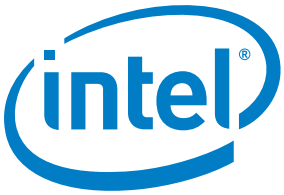

Intel® Quark™ Microcontroller Software Interface Pin Multiplexing

Reference Guide

November 2016

Document Number: 335291-001EN

Contents

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Revision History

Date	Revision	Description
November 2016	001	Initial release.

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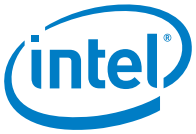

1.0 Introduction

1.1 Overview

The Intel® Quark™ Microcontroller Software Interface (QMSI) supports pin multiplexing. This document provides developers with the information required to program applications with the Intel® QMSI Pin Multiplexing module.

1.2 Audience and Purpose

This guide is intended for embedded programmers who wish to write code containing pin multiplexing functions for the Intel® Quark™ SE Microcontroller C1000.

1.3 Terminology

Table 1. Terminology

Term	Description
GPIO	General Purpose Input/Output
QMSI	Intel® Quark™ Microcontroller Software Interface

1.4 Reference Documents

Table 2. Reference Documents

Document	Document Number/Location
Intel® Quark™ SE Microcontroller C1000 Datasheet	334712-003EN
Intel® Quark™ Microcontroller Software Interface 1.1	333612-002EN
Intel® Quark™ Microcontroller Software Interface 1.3.1	GitHub

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2.0 Pin Multiplexing Setup

2.1 Intel® QMSI Pin Multiplexing Configuration

For detailed information about configuring the Intel® QMSI Pin Multiplexing module, please refer to the Intel® Quark™ Microcontroller Software Interface documents listed in Section 1.4, “Reference Documents”.

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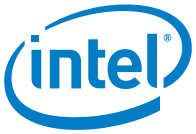

3.0 Intel® QMSI Pin Multiplexing Guidelines

The following sections describe a way to configure an Intel® QMSI Pin Multiplexing feature, using a GPIO as an example.

3.1 GPIO Pin Multiplexing Description

For all Pin Multiplexing functionality, there is a contiguous set of registers that work on EXTERNAL/Intel® QMSI pins 0-68. For the GPIO functionality, there is one register that deals with the associated pins for that one GPIO controller.

3.2 Configuring Intel® QMSI Pin Multiplexing for GPIO

To configure pin multiplexing for the Intel® Quark™ SE Microcontroller C1000, you must do the following:

- Set a PIN to a certain Intel® QMSI multiplexing function (for example, GPIO[25]):

```
qm_pmux_select (QM_PIN_ID_59, QM_PMUX_FN_0)
```

- Control a GPIO via an Intel® QMSI GPIO function, as GPIO[25] is on GPIO controller 0:

```
qm_gpio_set_pin (QM_GPIO_0, 25)
```

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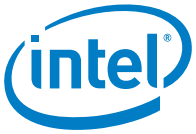
4.0 Intel® QMSI Pin Multiplexing for Peripherals

The mapping required to enable pin multiplexing for common peripherals is described in the following table.

Table 3. Pin and Muxing Functions Mapping for Peripherals

QMSI Pin ID	External Pin ID	QMSI Muxing	Function_0	Function_1	Function_2
QM_PIN_ID_0	GPIO[0]	QM_PMUX_FN_0	QM_GPIO_0		QM_SPI_0
QM_PIN_ID_1	GPIO[1]	QM_PMUX_FN_0	QM_GPIO_0		QM_SPI_0
QM_PIN_ID_2	GPIO[2]	QM_PMUX_FN_0	QM_GPIO_0		QM_SPI_0
QM_PIN_ID_3	GPIO[3]	QM_PMUX_FN_0	QM_GPIO_0		QM_SPI_0
QM_PIN_ID_4	GPIO[4]	QM_PMUX_FN_0	QM_GPIO_0		
QM_PIN_ID_5	GPIO[5]	QM_PMUX_FN_0	QM_GPIO_0		
QM_PIN_ID_6	GPIO[6]	QM_PMUX_FN_0	QM_GPIO_0		
QM_PIN_ID_7	GPIO[7]	QM_PMUX_FN_0	QM_GPIO_0		
QM_PIN_ID_8	GPIO_SS[0]	QM_PMUX_FN_0	QM_SS_GPIO_0		QM_UART_1
QM_PIN_ID_9	GPIO_SS[1]	QM_PMUX_FN_0	QM_ SS_GPIO_0		QM_UART_1
QM_PIN_ID_10	GPIO_SS[2]	QM_PMUX_FN_0	QM_ SS_GPIO_0		
QM_PIN_ID_11	GPIO_SS[3]	QM_PMUX_FN_0	QM_ SS_GPIO_0		
QM_PIN_ID_12	GPIO_SS[4]	QM_PMUX_FN_0	QM_ SS_GPIO_0		
QM_PIN_ID_13	GPIO_SS[5]	QM_PMUX_FN_0	QM_ SS_GPIO_0		
QM_PIN_ID_14	GPIO_SS[6]	QM_PMUX_FN_0	QM_ SS_GPIO_0		
QM_PIN_ID_15	GPIO_SS[7]	QM_PMUX_FN_0	QM_ SS_GPIO_0		
QM_PIN_ID_16	GPIO_SS[8]	QM_PMUX_FN_0	QM_ SS_GPIO_0		QM_UART_1
QM_PIN_ID_17	GPIO_SS[9]	QM_PMUX_FN_0	QM_ SS_GPIO_0		QM_UART_1
QM_PIN_ID_18	UART0_RXD	QM_PMUX_FN_0	QM_UART_0		
QM_PIN_ID_19	GPIO[31]	QM_PMUX_FN_1	QM_UART_0	QM_GPIO_0	
QM_PIN_ID_20	I2C0_SCL	QM_PMUX_FN_0	QM_I2C_0		
QM_PIN_ID_21	I2C0_SDA	QM_PMUX_FN_0	QM_I2C_0		
QM_PIN_ID_22	I2C1_SCL	QM_PMUX_FN_0	QM_I2C_1		
QM_PIN_ID_23	I2C1_SDA	QM_PMUX_FN_0	QM_I2C_1		
QM_PIN_ID_24	I2C0_SS_SDA	QM_PMUX_FN_0	QM_SS_I2C_0		
QM_PIN_ID_25	I2C0_SS_SCL	QM_PMUX_FN_0	QM_SS_I2C_0		
QM_PIN_ID_26	I2C1_SS_SDA	QM_PMUX_FN_0	QM_SS_I2C_1		
QM_PIN_ID_27	I2C1_SS_SCL	QM_PMUX_FN_0	QM_SS_I2C_1		
QM_PIN_ID_28	SPI0_SS_MISO	QM_PMUX_FN_0	QM_SS_SPI_0		
QM_PIN_ID_29	SPI0_SS_MOSI	QM_PMUX_FN_0	QM_SS_SPI_0		
QM_PIN_ID_30	SPI0_SS_SCK	QM_PMUX_FN_0	QM_SS_SPI_0		
QM_PIN_ID_31	SPI0_SS_CS_B[0]	QM_PMUX_FN_0	QM_SS_SPI_0		



QMSI Pin ID	External Pin ID	QMSI Muxing	Function_0	Function_1	Function_2
QM_PIN_ID_32	SPI0_SS_CS_B[1]	QM_PMUX_FN_0	QM_SS_SPI_0		
QM_PIN_ID_33	GPIO[29]	QM_PMUX_FN_1	QM_SS_SPI_0	QM_GPIO_0	
QM_PIN_ID_34	GPIO[30]	QM_PMUX_FN_1	QM_SS_SPI_0	QM_GPIO_0	
QM_PIN_ID_35	SPI1_SS_MISO	QM_PMUX_FN_0	QM_SS_SPI_1		
QM_PIN_ID_36	SPI1_SS_MOSI	QM_PMUX_FN_0	QM_SS_SPI_1		
QM_PIN_ID_37	SPI1_SS_SCK	QM_PMUX_FN_0	QM_SS_SPI_1		
QM_PIN_ID_38	SPI1_SS_CS_B[0]	QM_PMUX_FN_0	QM_SS_SPI_1		
QM_PIN_ID_39	SPI1_SS_CS_B[1]	QM_PMUX_FN_0	QM_SS_SPI_1		
QM_PIN_ID_40	SPI1_SS_CS_B[2]	QM_PMUX_FN_0	QM_SS_SPI_1	QM_UART_0	
QM_PIN_ID_41	SPI1_SS_CS_B[3]	QM_PMUX_FN_0	QM_SS_SPI_1	QM_ UART_0	
QM_PIN_ID_42	GPIO[8]	QM_PMUX_FN_0	QM_GPIO_0	QM_SPI_1	
QM_PIN_ID_43	GPIO[9]	QM_PMUX_FN_0	QM_GPIO_0	QM_SPI_1	
QM_PIN_ID_44	GPIO[10]	QM_PMUX_FN_0	QM_GPIO_0	QM_SPI_1	
QM_PIN_ID_45	GPIO[11]	QM_PMUX_FN_0	QM_GPIO_0	QM_SPI_1	
QM_PIN_ID_46	GPIO[12]	QM_PMUX_FN_0	QM_GPIO_0	QM_SPI_1	
QM_PIN_ID_47	GPIO[13]	QM_PMUX_FN_0	QM_GPIO_0	QM_SPI_1	
QM_PIN_ID_48	GPIO[14]	QM_PMUX_FN_0	QM_GPIO_0	QM_SPI_1	
QM_PIN_ID_49	GPIO[15]	QM_PMUX_FN_0	QM_GPIO_0		
QM_PIN_ID_50	GPIO[16]	QM_PMUX_FN_0	QM_GPIO_0		
QM_PIN_ID_51	GPIO[17]	QM_PMUX_FN_0	QM_GPIO_0		
QM_PIN_ID_52	GPIO[18]	QM_PMUX_FN_0	QM_GPIO_0		
QM_PIN_ID_53	GPIO[19]	QM_PMUX_FN_0	QM_GPIO_0		
QM_PIN_ID_54	GPIO[20]	QM_PMUX_FN_0	QM_GPIO_0		
QM_PIN_ID_55	GPIO[21]	QM_PMUX_FN_0	QM_GPIO_0	QM_SPI_0	
QM_PIN_ID_56	GPIO[22]	QM_PMUX_FN_0	QM_GPIO_0	QM_SPI_0	
QM_PIN_ID_57	GPIO[23]	QM_PMUX_FN_0	QM_GPIO_0	QM_SPI_0	
QM_PIN_ID_58	GPIO[24]	QM_PMUX_FN_0	QM_GPIO_0	QM_SPI_0	
QM_PIN_ID_59	GPIO[25]	QM_PMUX_FN_0	QM_GPIO_0	QM_SPI_0	
QM_PIN_ID_60	GPIO[26]	QM_PMUX_FN_0	QM_GPIO_0	QM_SPI_0	
QM_PIN_ID_61	GPIO[27]	QM_PMUX_FN_0	QM_GPIO_0	QM_SPI_0	
QM_PIN_ID_62	GPIO[28]	QM_PMUX_FN_0	QM_GPIO_0		
QM_PIN_ID_63	GPIO_SS[10]	QM_PMUX_FN_0	QM_ SS_GPIO_0	QM_ PWM_0	
QM_PIN_ID_64	GPIO_SS[11]	QM_PMUX_FN_0	QM_ SS_GPIO_0	QM_ PWM_0	
QM_PIN_ID_65	GPIO_SS[12]	QM_PMUX_FN_0	QM_ SS_GPIO_0	QM_ PWM_0	
QM_PIN_ID_66	GPIO_SS[13]	QM_PMUX_FN_0	QM_ SS_GPIO_0	QM_ PWM_0	
QM_PIN_ID_67	GPIO_SS[14]	QM_PMUX_FN_0	QM_ SS_GPIO_0		
QM_PIN_ID_68	GPIO_SS[15]	QM_PMUX_FN_0	QM_ SS_GPIO_0