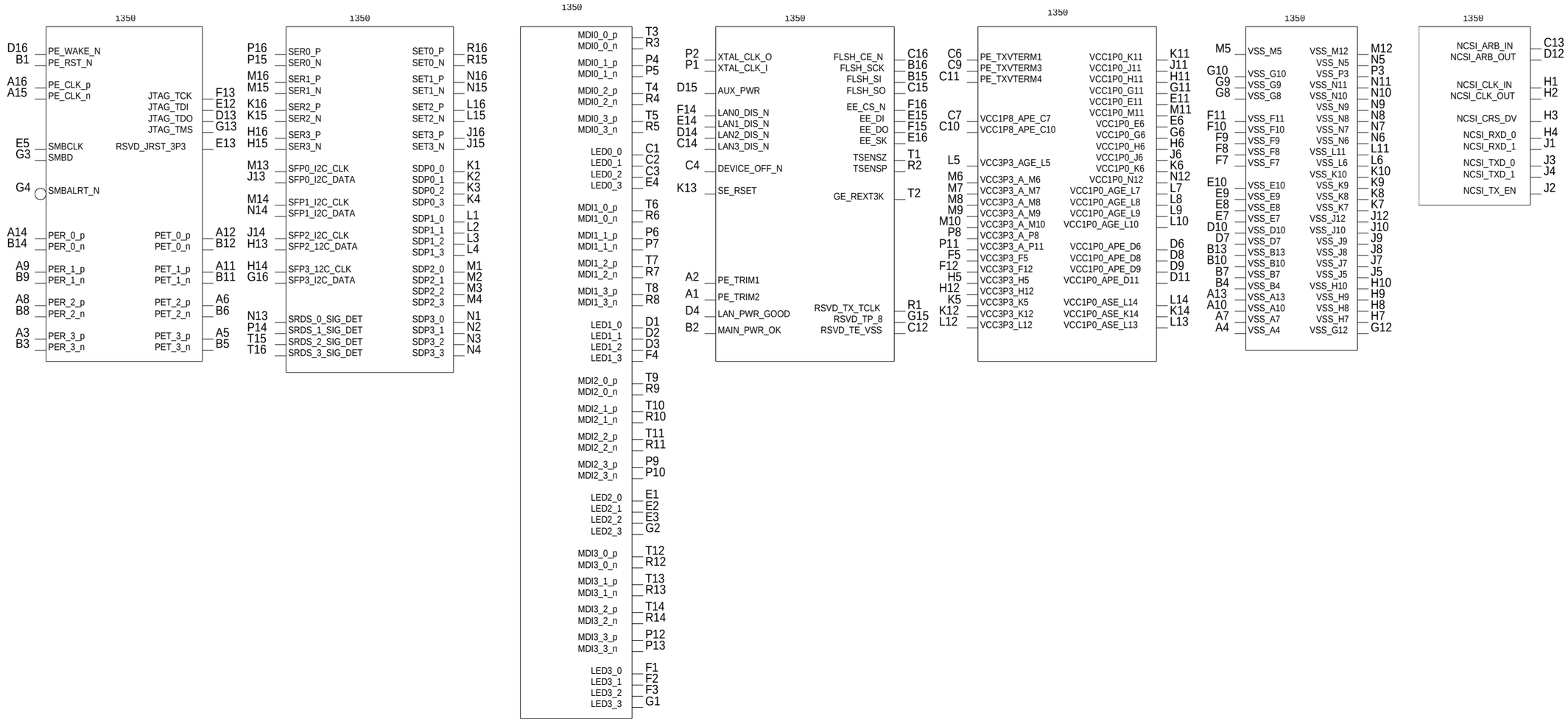
I350 REFERENCE DESIGN



LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE I350 REFERENCE DESIGN	SIZE B	CODE	DOCUMENT NUMBER 323852-002	REV 2.0	DATE 2011-06-22	SHEET 1

REVISION CONTROL

0.95 - SVR & TSENS PIN CHANGE
1.00 - PRELIMINARY
2.00 - RELEASED

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2111 N.E. 25th AVENUE
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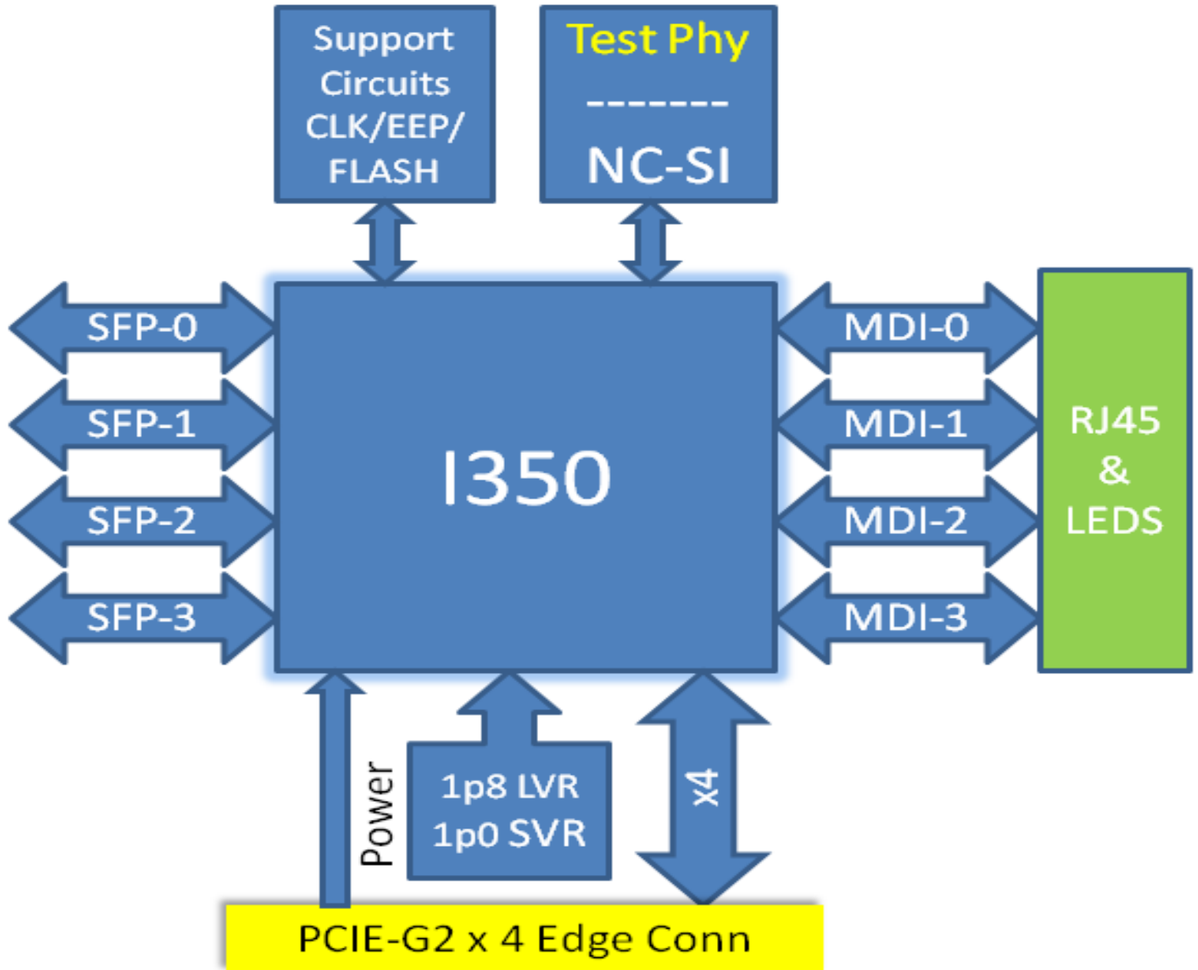
I350 Reference Design



THE I350 HAS 4 BASE-T INTERFACES AND 4 SERDES INTERFACES CONNECTED TO 4 PCIE FUNCTIONS. EACH PCIE FUNCTION CAN BE SWITCHED TO EITHER THE BASE-T INTERFACE OR THE SERDES INTERFACE. THE SWITCH IS CONFIGURED WITH A STATIC EEPROM SETTING OR DYNAMICALLY THROUGH A REGISTER SETTING.

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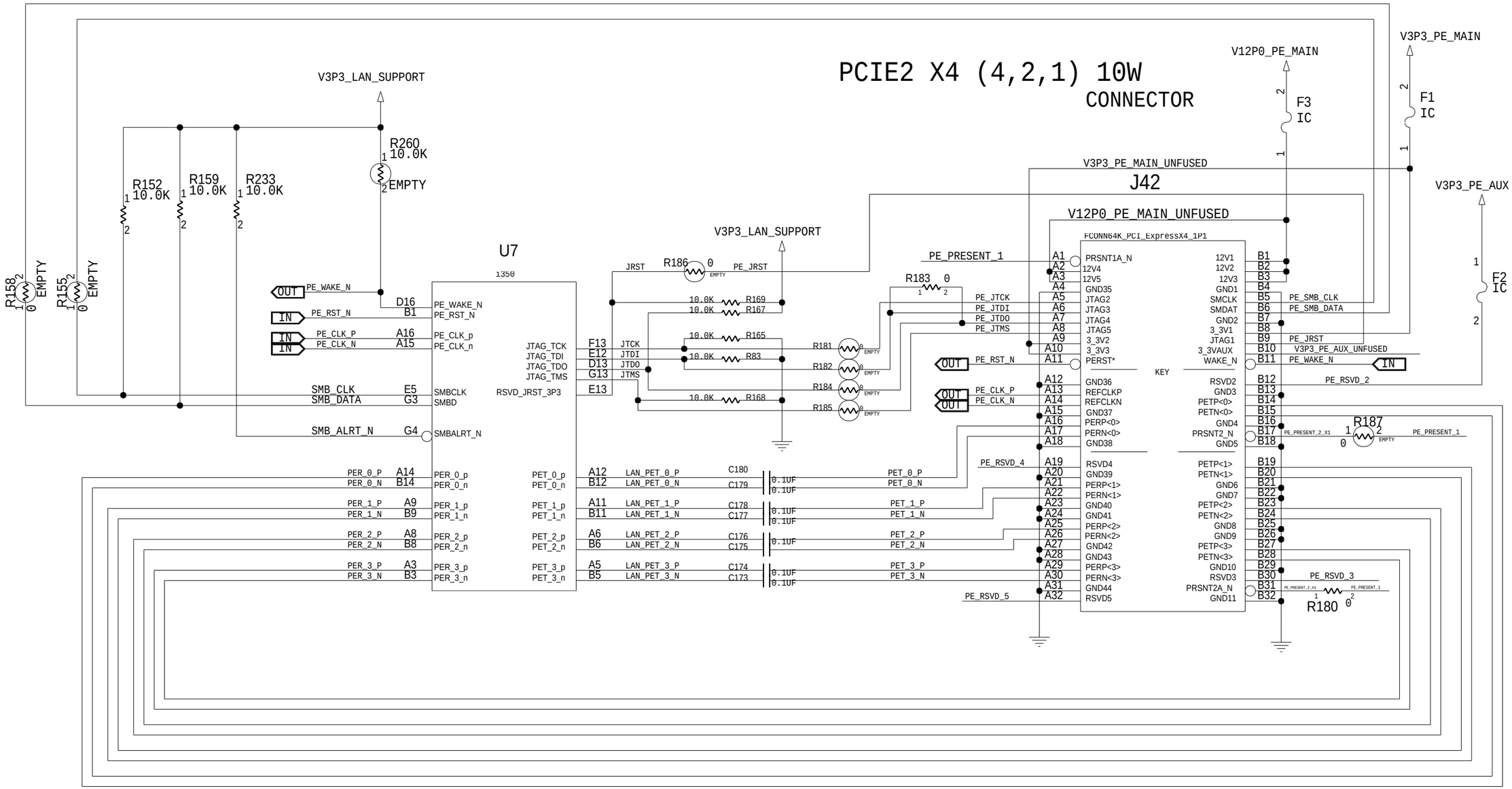
PCIE - SMB - JTAG



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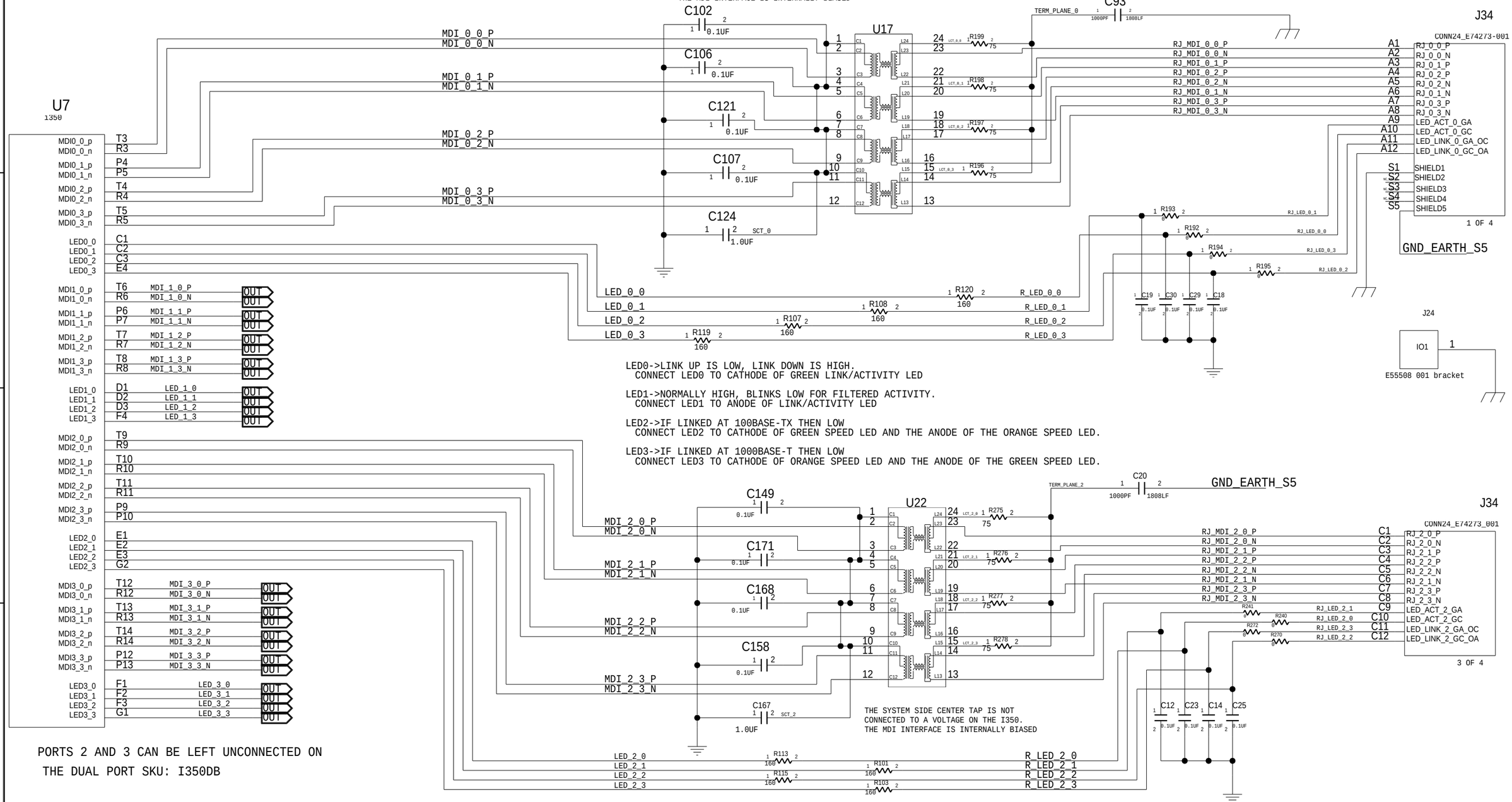
MDI 10BASE-T/100BASE-TX/1000BASE-T

THE MDI INTERFACE ON THE I350 IS INTERNALLY TERMINATED.
EXTERNAL MDI TERMINATION IS NOT REQUIRED

THE SYSTEM SIDE CENTER TAP IS NOT
CONNECTED TO A VOLTAGE ON THE I350.
THE MDI INTERFACE IS INTERNALLY BIASED



LED0->LINK UP IS LOW, LINK DOWN IS HIGH.
CONNECT LED0 TO CATHODE OF GREEN LINK/ACTIVITY LED

LED1->NORMALLY HIGH, BLINKS LOW FOR FILTERED ACTIVITY.
CONNECT LED1 TO ANODE OF LINK/ACTIVITY LED

LED2->IF LINKED AT 100BASE-TX THEN LOW
CONNECT LED2 TO CATHODE OF GREEN SPEED LED AND THE ANODE OF THE ORANGE SPEED LED.

LED3->IF LINKED AT 1000BASE-T THEN LOW
CONNECT LED3 TO CATHODE OF ORANGE SPEED LED AND THE ANODE OF THE GREEN SPEED LED.

THE SYSTEM SIDE CENTER TAP IS NOT
CONNECTED TO A VOLTAGE ON THE I350.
THE MDI INTERFACE IS INTERNALLY BIASED

PORTS 2 AND 3 CAN BE LEFT UNCONNECTED ON
THE DUAL PORT SKU: I350DB

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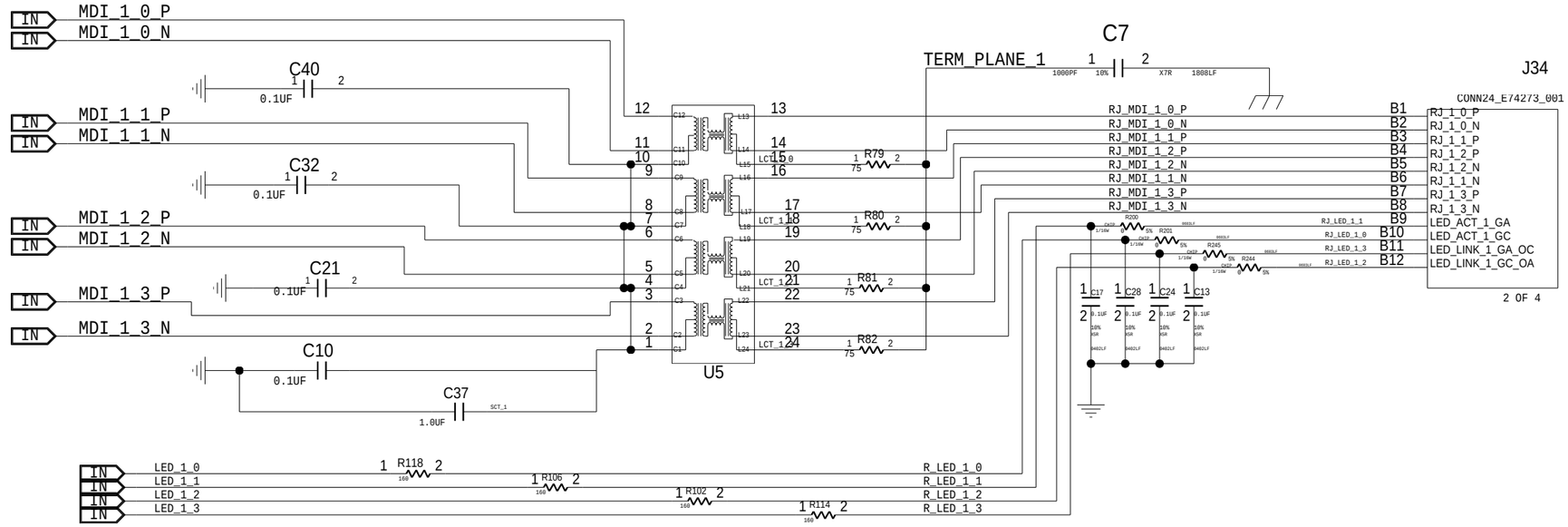
MDI 10BASE-T/100BASE-TX/1000BASE-T

THE SYSTEM SIDE CENTER TAP IS NOT
CONNECTED TO A VOLTAGE ON THE I350.
THE MDI INTERFACE IS INTERNALLY BIASED

THE MDI INTERFACE ON THE 82580 IS INTERNALLY TERMINATED.
EXTERNAL MDI TERMINATION IS NOT REQUIRED



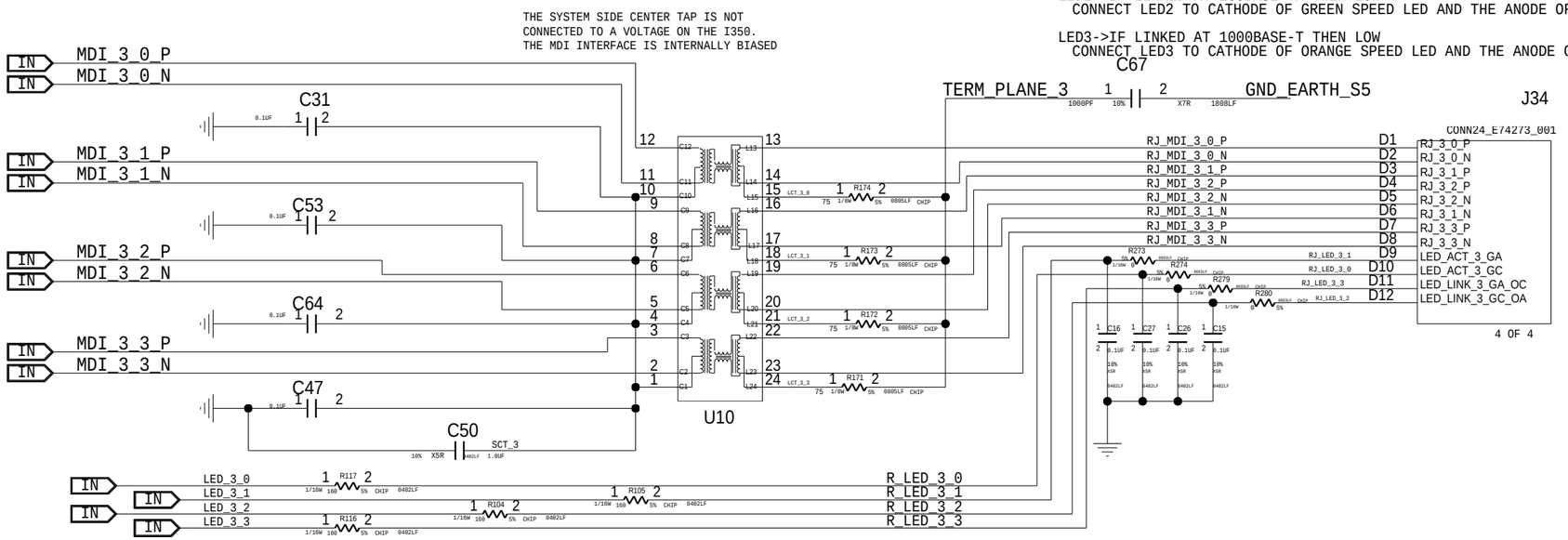
LED0->LINK UP IS LOW, LINK DOWN IS HIGH.
CONNECT LED0 TO CATHODE OF GREEN LINK/ACTIVITY LED

LED1->NORMALLY HIGH, BLINKS LOW FOR FILTERED ACTIVITY.
CONNECT LED1 TO ANODE OF LINK/ACTIVITY LED

LED2->IF LINKED AT 100BASE-TX THEN LOW
CONNECT LED2 TO CATHODE OF GREEN SPEED LED AND THE ANODE OF THE ORANGE SPEED LED.

LED3->IF LINKED AT 1000BASE-T THEN LOW
CONNECT LED3 TO CATHODE OF ORANGE SPEED LED AND THE ANODE OF THE GREEN SPEED LED.

THE SYSTEM SIDE CENTER TAP IS NOT
CONNECTED TO A VOLTAGE ON THE I350.
THE MDI INTERFACE IS INTERNALLY BIASED



HEATSINK

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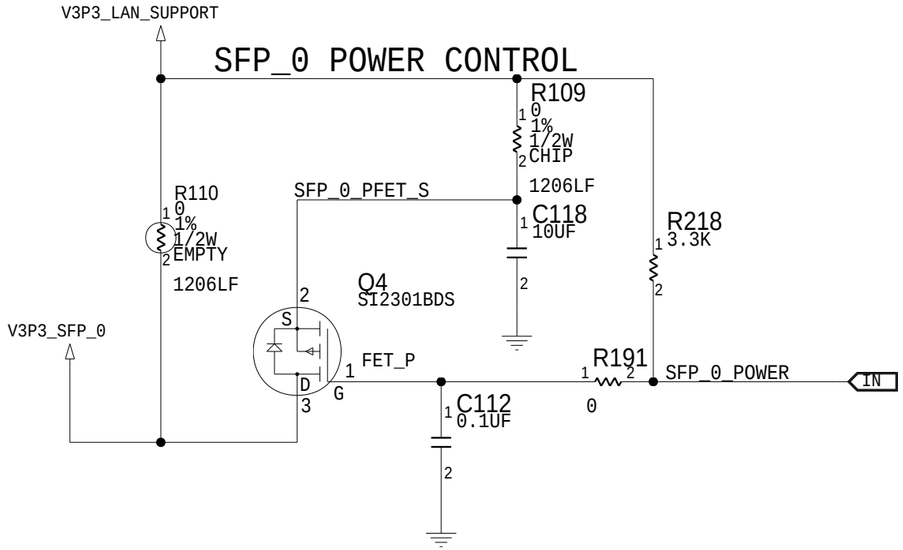
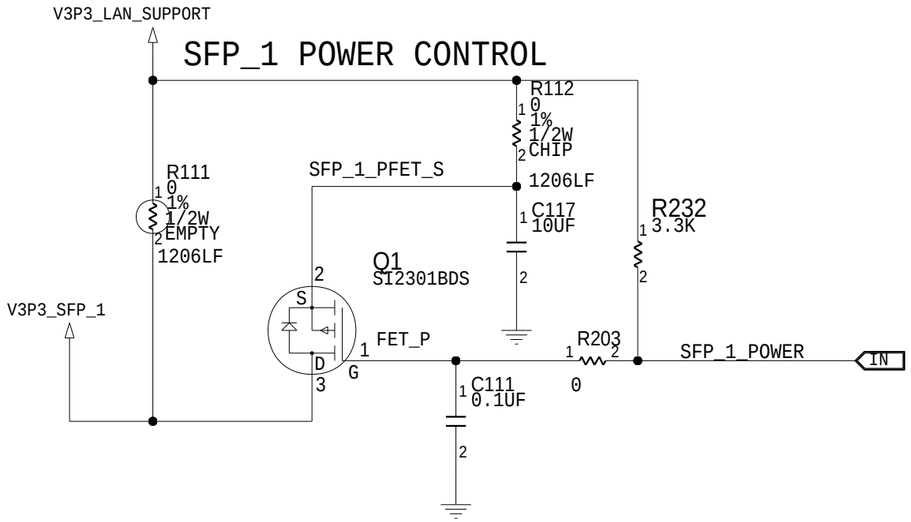
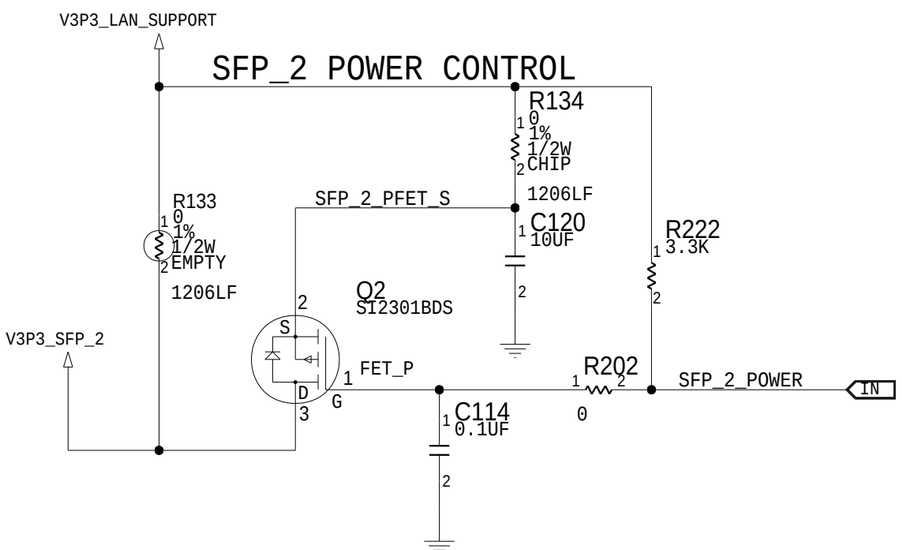
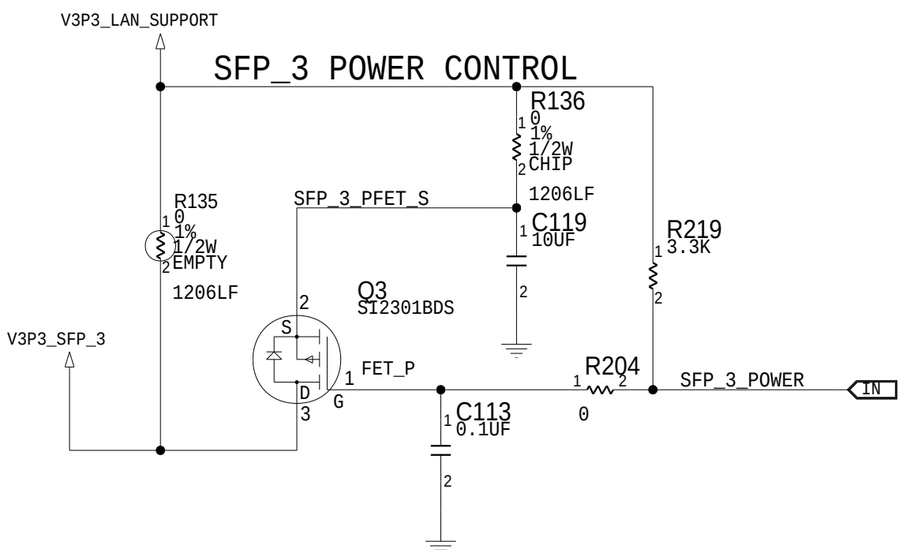
SFP MODULES MAY NEED TO BE SHUT DOWN WHILE IN LOW POWER STATES
THESE FETS ALLOW SOFTWARE TO CONTROL THE SFP MODULE POWER.









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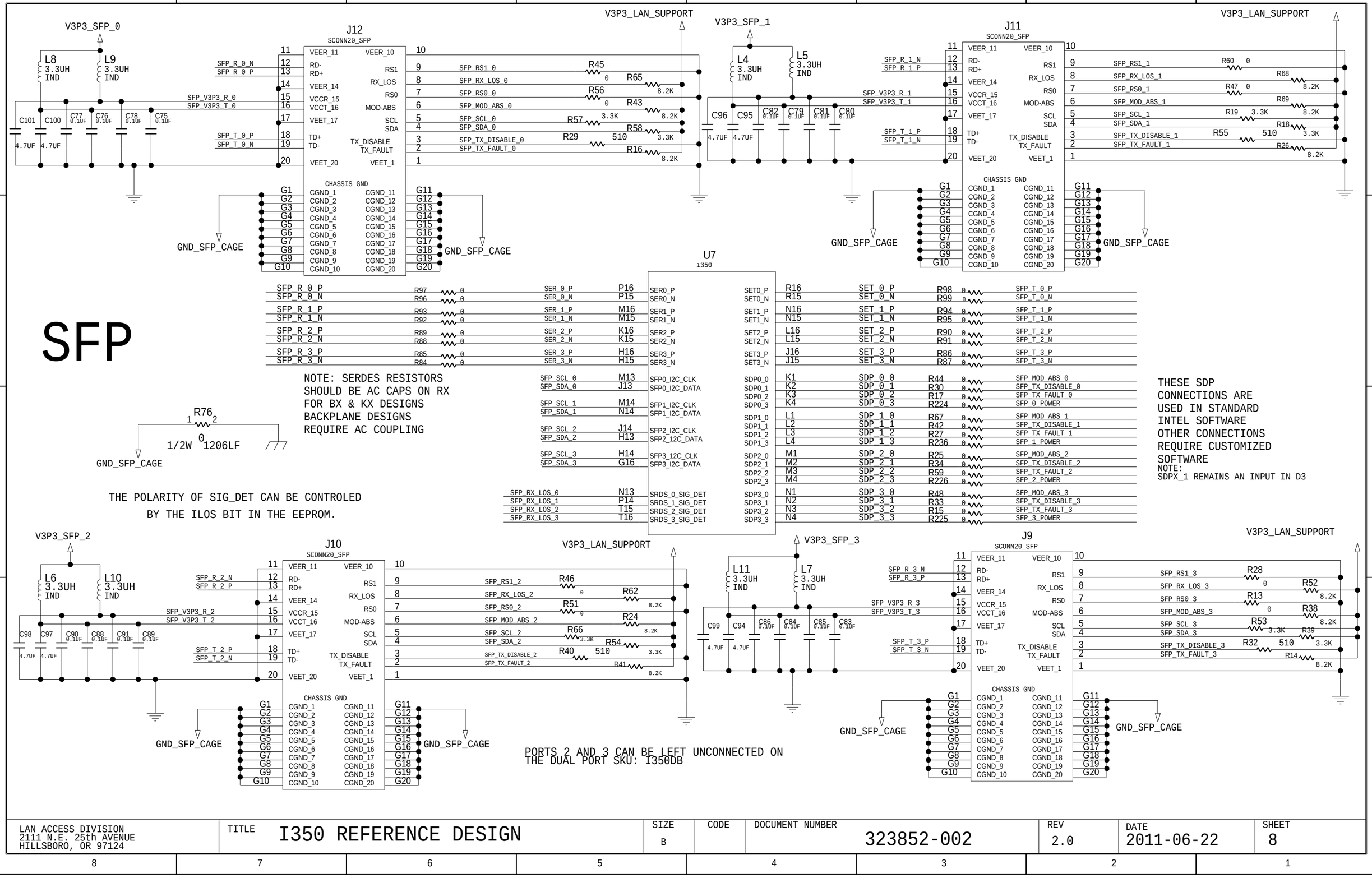
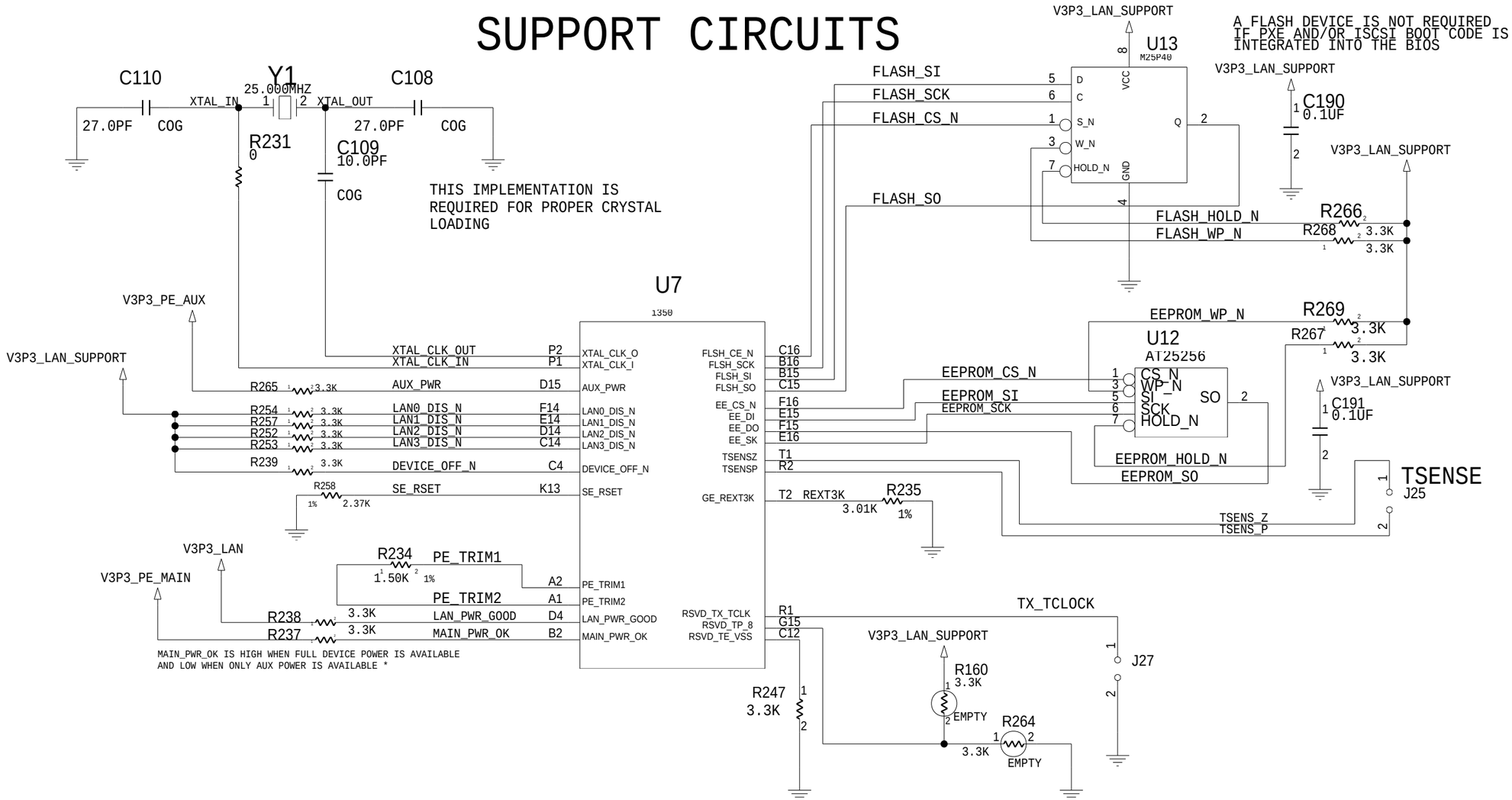
SFP



LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE: I350 REFERENCE DESIGN	SIZE: B	CODE	DOCUMENT NUMBER: 323852-002	REV: 2.0	DATE: 2011-06-22	SHEET: 8

SUPPORT CIRCUITS



* WHEN MAIN_PWR_OK TRANSITIONS FROM HIGH TO LOW THE KEEP_PHY_LINK_UP BIT IS CLEARED.
THIS PREVENTS THE DEVICE FROM USING TOO MUCH POWER EVEN IN THE CASE THAT THE BMC WAS TRYING TO BLOCK PHY STATUS CHANGES.

IF THE POWER SUPPLIES CAN PROVIDE ENOUGH POWER TO POWERVILLE TO MAINTAIN A 1000BASE-T LINK AT ALL TIMES
AND IF THE BMC WANTS LINK TO SURVIVE WHEN THE KEEP_PHY_LINK_UP IS SET EVEN IF MAIN POWER IS NOT AVAILABLE
THE MAIN_PWR_OK SHOULD BE PULLED UP TO 3.3V AT ALL TIMES.
IN THIS CASE, ENSURE PULL-UPS ARE CONNECTED TO POWER SUPPLIES DERVIVED FROM AUX POWER.

THE EXACT 3.3K OHM VALUE OF THE PULL-UP RESISTER IS NOT CRITICAL. 0 OHM TO 10K OHM IS OK.

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POWER SUPPLIES

V1P8_LAN

C134 1.0UF
C152 0.01UF
C122 1000PF
C153 1000PF
C156 1.0UF
C144 0.01UF
C148 1000PF
C33 47UF
C22 10UF

V3P3_LAN

C123 1.0UF
C116 0.01UF
C115 1000PF
C130 1.0UF
C141 0.01UF
C126 1000PF
C150 1000PF
C55 47UF 1206LF
C105 10UF
C145 1.0UF
C146 0.01UF
C164 1000PF
C163 1000PF

U7
1350

C6	PE_TXVTERM1	VCC1P0_K11	K11
C9	PE_TXVTERM3	VCC1P0_J11	J11
C11	PE_TXVTERM4	VCC1P0_H11	H11
		VCC1P0_G11	G11
		VCC1P0_E11	E11
C7	VCC1P8_APE_C7	VCC1P0_M11	M11
C10	VCC1P8_APE_C10	VCC1P0_E6	E6
		VCC1P0_G6	G6
		VCC1P0_H6	H6
L5	VCC3P3_AGE_L5	VCC1P0_J6	J6
		VCC1P0_K6	K6
M6	VCC3P3_A_M6	VCC1P0_N12	N12
M7	VCC3P3_A_M7	VCC1P0_AGE_L7	L7
M8	VCC3P3_A_M8	VCC1P0_AGE_L8	L8
M9	VCC3P3_A_M9	VCC1P0_AGE_L9	L9
M10	VCC3P3_A_M10	VCC1P0_AGE_L10	L10
P8	VCC3P3_A_P8		
P11	VCC3P3_A_P11	VCC1P0_APE_D6	D6
F5	VCC3P3_F5	VCC1P0_APE_D8	D8
F12	VCC3P3_F12	VCC1P0_APE_D9	D9
H5	VCC3P3_H5	VCC1P0_APE_D11	D11
H12	VCC3P3_H12		
K5	VCC3P3_K5	VCC1P0_ASE_L14	L14
K12	VCC3P3_K12	VCC1P0_ASE_K14	K14
L12	VCC3P3_L12	VCC1P0_ASE_L13	L13

U7
1350

M5	VSS_M5	VSS_M12	M12
		VSS_N5	N5
G10	VSS_G10	VSS_P3	P3
G9	VSS_G9	VSS_N11	N11
G8	VSS_G8	VSS_N10	N10
		VSS_N9	N9
F11	VSS_F11	VSS_N8	N8
F10	VSS_F10	VSS_N7	N7
F9	VSS_F9	VSS_N6	N6
F8	VSS_F8	VSS_L11	L11
F7	VSS_F7	VSS_L6	L6
		VSS_K10	K10
E10	VSS_E10	VSS_K9	K9
E9	VSS_E9	VSS_K8	K8
E8	VSS_E8	VSS_K7	K7
E7	VSS_E7	VSS_J12	J12
D10	VSS_D10	VSS_J10	J10
D7	VSS_D7	VSS_J9	J9
B13	VSS_B13	VSS_J8	J8
B10	VSS_B10	VSS_J7	J7
B7	VSS_B7	VSS_J5	J5
B4	VSS_B4	VSS_H10	H10
A13	VSS_A13	VSS_H9	H9
A10	VSS_A10	VSS_H8	H8
A7	VSS_A7	VSS_H7	H7
A4	VSS_A4	VSS_G12	G12

V1P0_LAN

C151 1000PF
C143 1000PF
C125 1000PF
C132 1000PF
C128 0.01UF
C129 1.0UF
C139 1000PF
C182 1000PF
C131 0.01UF
C154 1.0UF
C138 1000PF
C137 1000PF
C127 0.01UF
C142 1.0UF
C155 1000PF
C181 1000PF
C165 0.01UF
C183 1.0UF
C159 10UF
C60 47UF

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POWER SUPPLY TREE

POWER SUPPLIES SHOWN ARE SUGGESTED EXAMPLES.
THEY SHOULD BE OPTIMIZED FOR EACH DESIGN
BY POWER INTEGRITY ENGINEER.

V12P0_PE_MAIN

J40
1
2
CONN THLF

TPS40055 SVR
12P0-3P3V
SHEET 14

12-TO-4.4 V BUCK
TPS40055
VIN = 8 TO 40 V
IOUT_MAX = 5 A

EFFICIENCY ~ 80%
PMAX ~ 11 W
V ~ 12 V ± 8%
I_MAX ~ 1 A

V3P3
DIODE_OR

SHEET 13

V3P3_OR

J39
1
2
CONN THLF

IDEAL DIODE

V3P3_PE_AUX

J41
1
2
CONN THLF

LTC4352
VIN = 0 TO VCC V
IOUT_MAX = 2.5 A

V5P0_SATA
EXTERNAL
AUX PWR

V3P3
ENABLE
SHEET 15

P ~ 8.74 W
V = 3.7-4.0 V

LTC3533
BUCK/BOOST
SVR FOR V3P3

SHEET 14

VIN = 1.8 TO 5.5 V
IOUT_MAX = 2 A (BUCK)
1.5 A (BOOST)

EFFICIENCY ~ 90%
P_IN ~ 5.8 W

V3P3_POWER

PMAX = 5.23 W
V = 3.3 V ± 9%
I_MAX = 1.46 A

J47 CONN THLF
1
2

R137
0 1%
1/2W CHIP 1206LF

J46
2
4
1
3

V3P3_LAN

J44 CONN THLF
1
2

R130
0 1%
1/2W CHIP 1206LF

J45
2
4
1
3

V3P3_LAN_SUPPORT

I350-LVR

SHEET 16

V1P8_POWER

J33 CONN THLF
1
2

R140
0 1%
1/2W CHIP 1206LF

J23
2
4
1
3

V1P8_LAN

I350-SVR

SHEET 16

V1P0_POWER

J48 CONN THLF
1
2

R154
0 1%
1/2W CHIP 1206LF

THLF J49 CONN
2
4
1
3

V1P0_LAN

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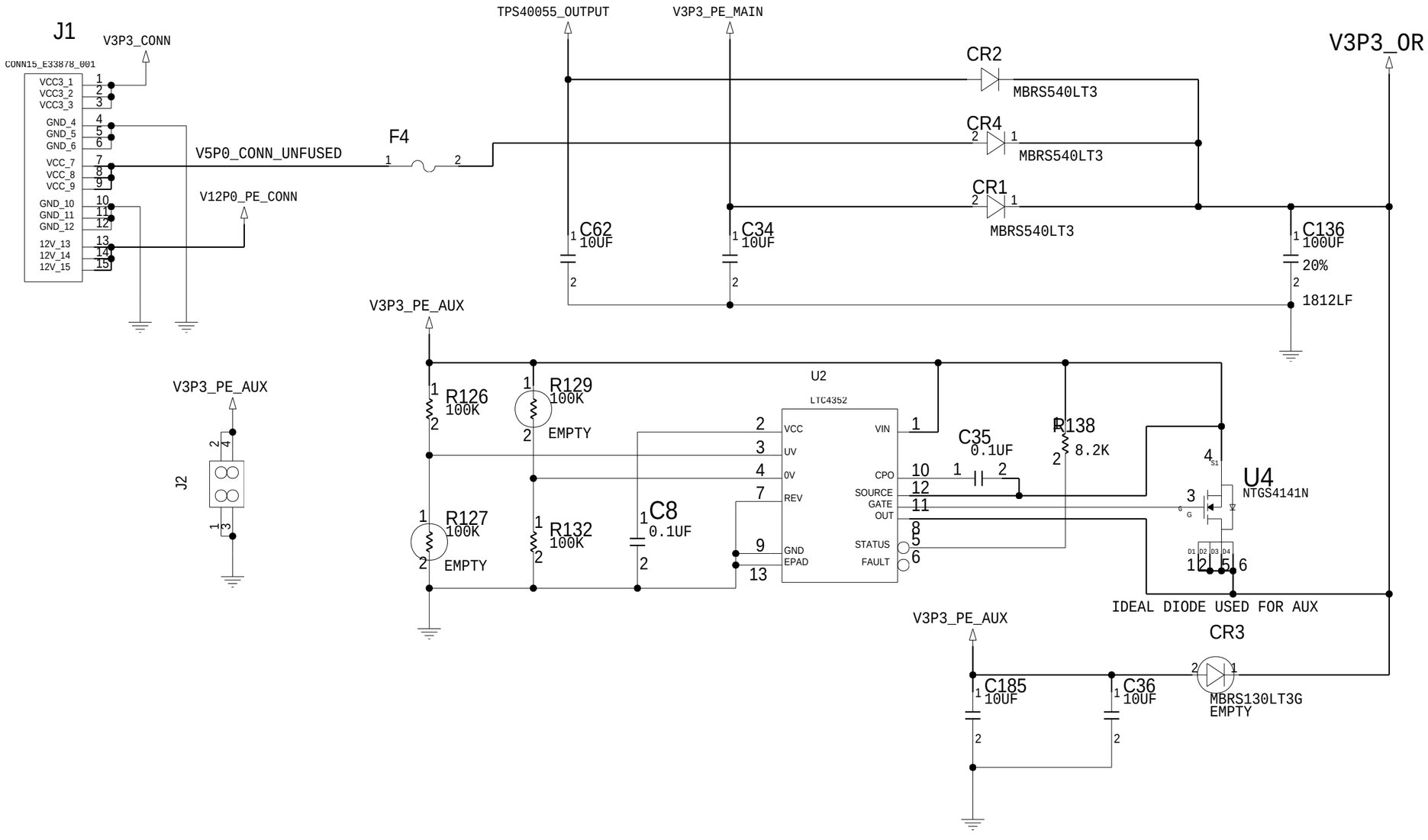
POWER MUX (AUX / MAIN SWITCH)



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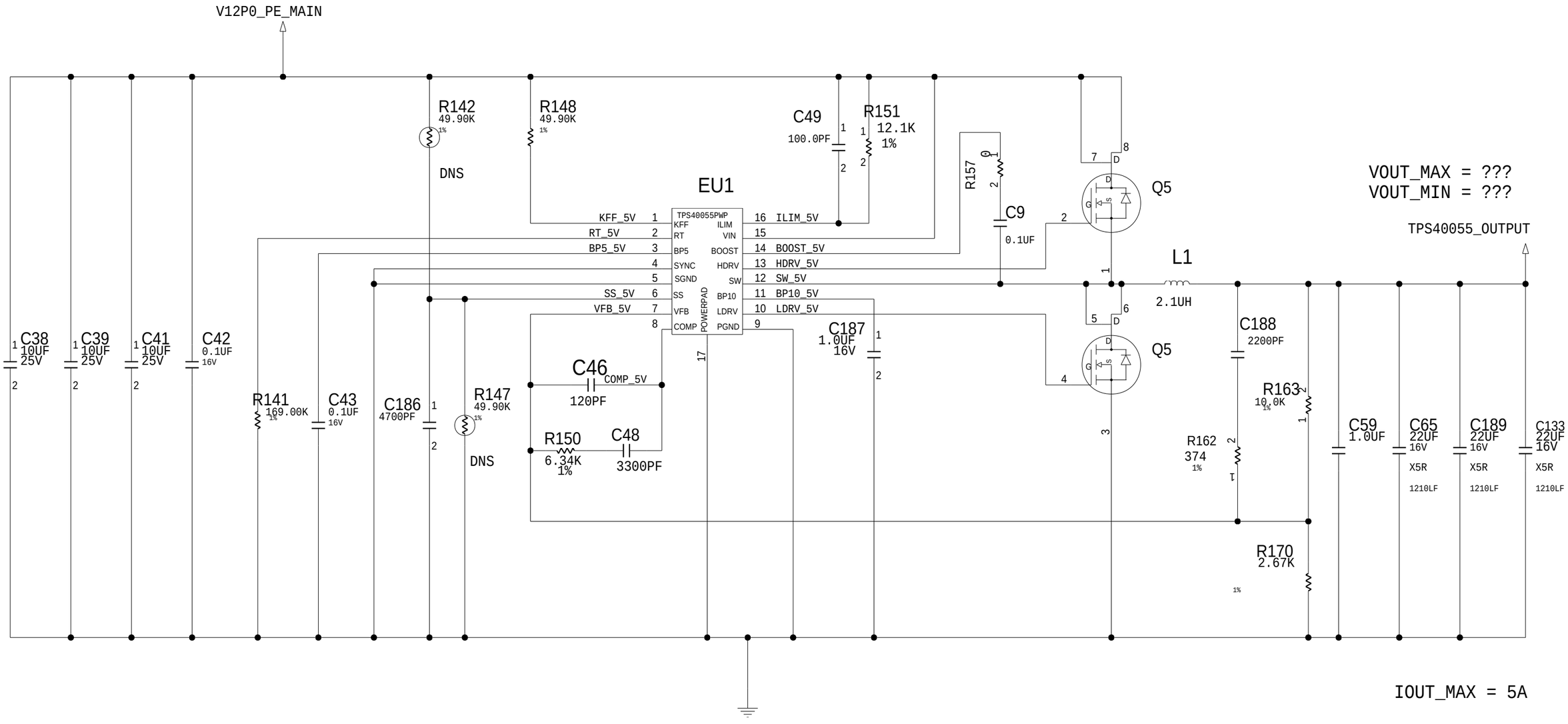
TPS40055 SWITCHING REGULATOR

POWER SUPPLY (12P0-3P3)



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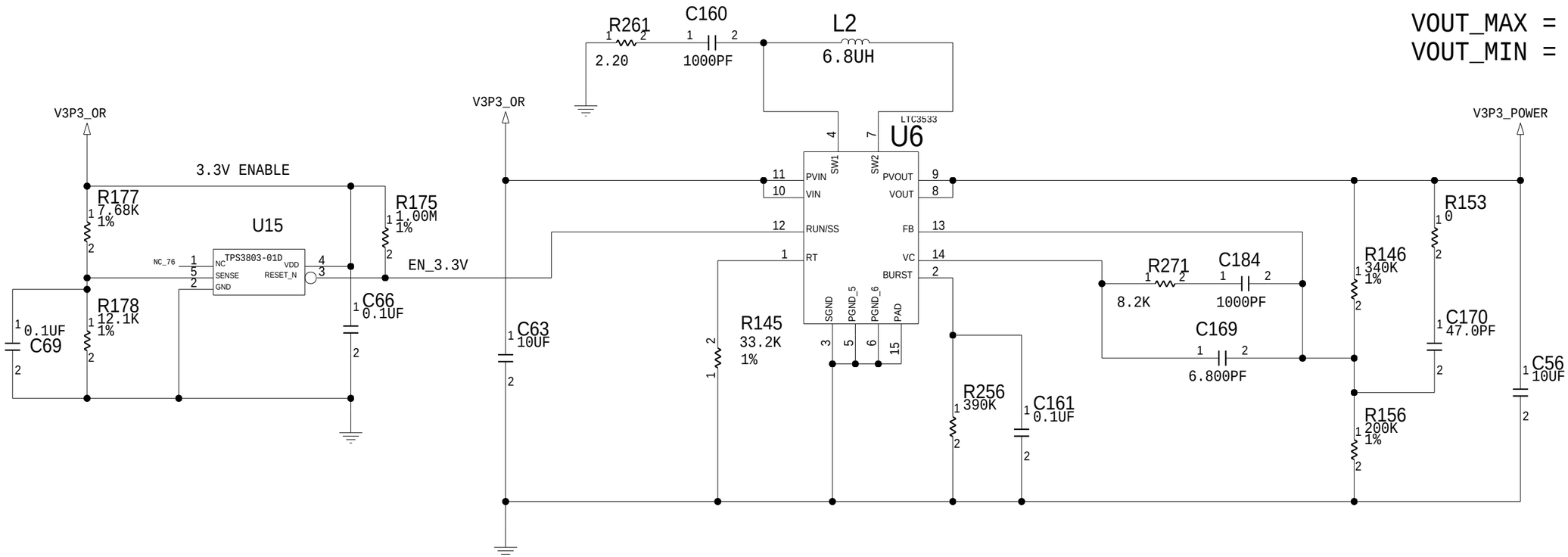
LTC3533 BUCK/BOOST REGULATOR FOR 3.3V

(REQUIRED FOR 4-PORT SFP OPERATION)



VOLTAGE BOOST REQUIRED TO COMPENSATE FOR
VOLTAGE DROP FROM DIODE OR CIRCUIT.
MANY DESIGNS MAY NOT REQUIRE A BOOST CIRCUIT.

$I_{3533\text{-}MAX}$ = 1.5A

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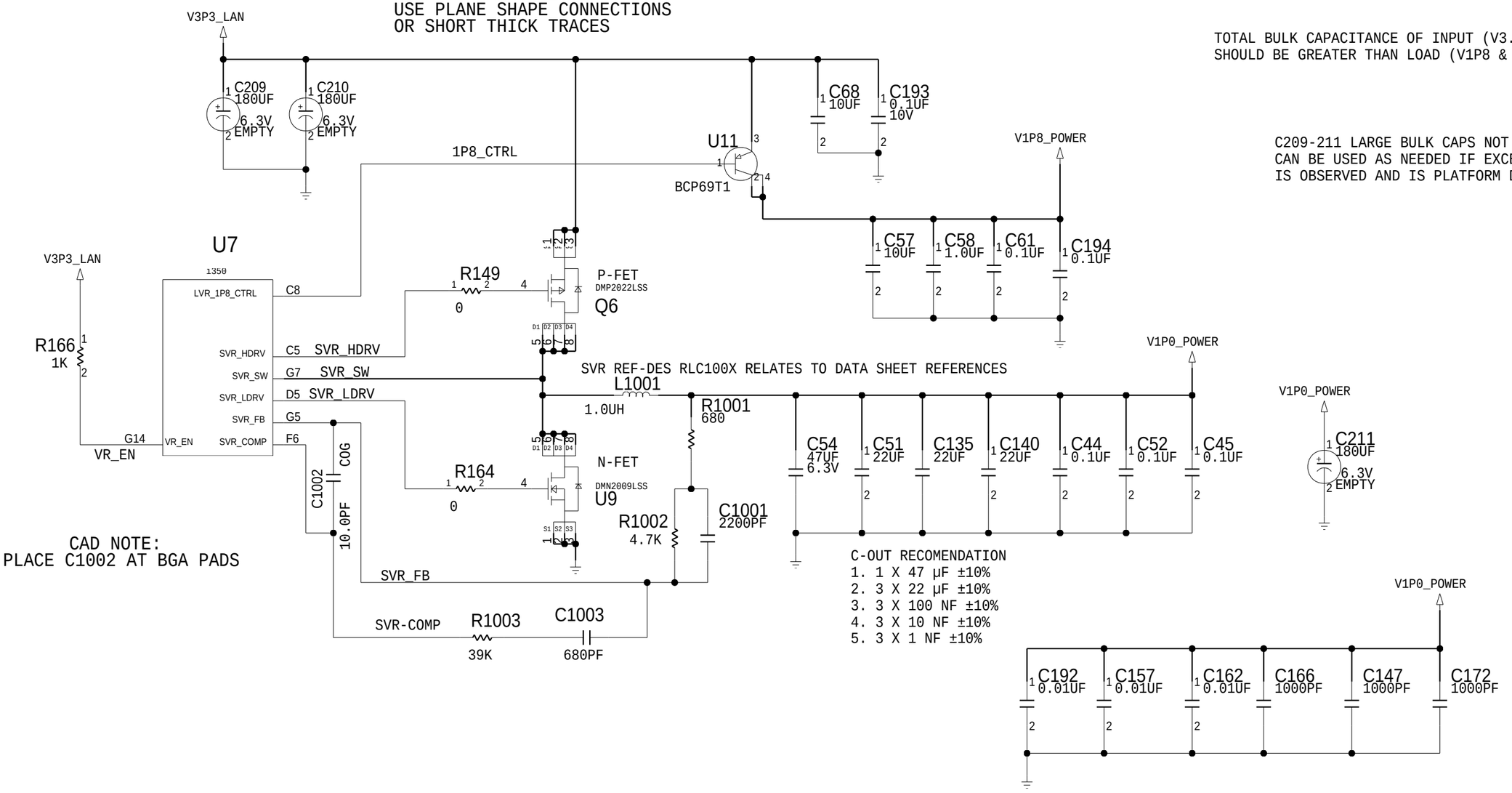
INTEGRATED 1.0V SVR & 1.8V LVR

CAD NOTE:
KEEP VR PARTS CLOSE TO BGA
USE PLANE SHAPE CONNECTIONS
OR SHORT THICK TRACES

TOTAL BULK CAPACITANCE OF INPUT (V3.3_LAN).
SHOULD BE GREATER THAN LOAD (V1P8 & V1P0).

C209-211 LARGE BULK CAPS NOT REQUIRED.
CAN BE USED AS NEEDED IF EXCESS RIPPLE
IS OBSERVED AND IS PLATFORM DEPENDANT.



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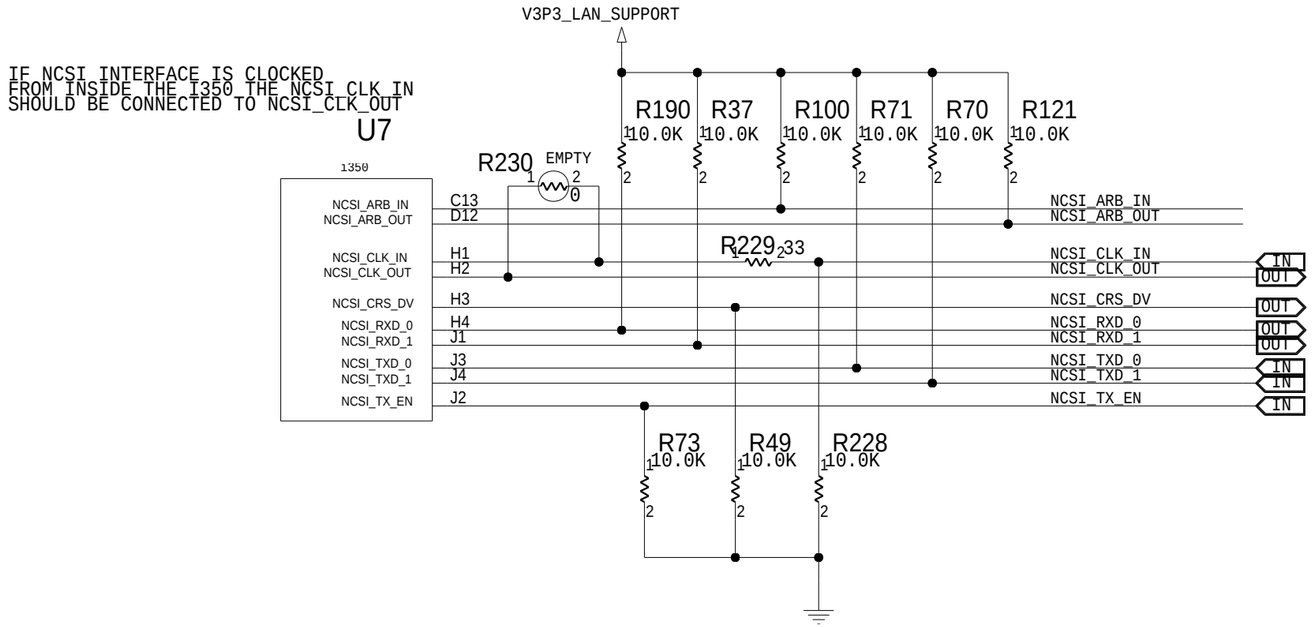
I350-NCSI

IF NCSI INTERFACE IS CLOCKED
FROM INSIDE THE I350 THE NCSI_CLK_IN
SHOULD BE CONNECTED TO NCSI_CLK_OUT



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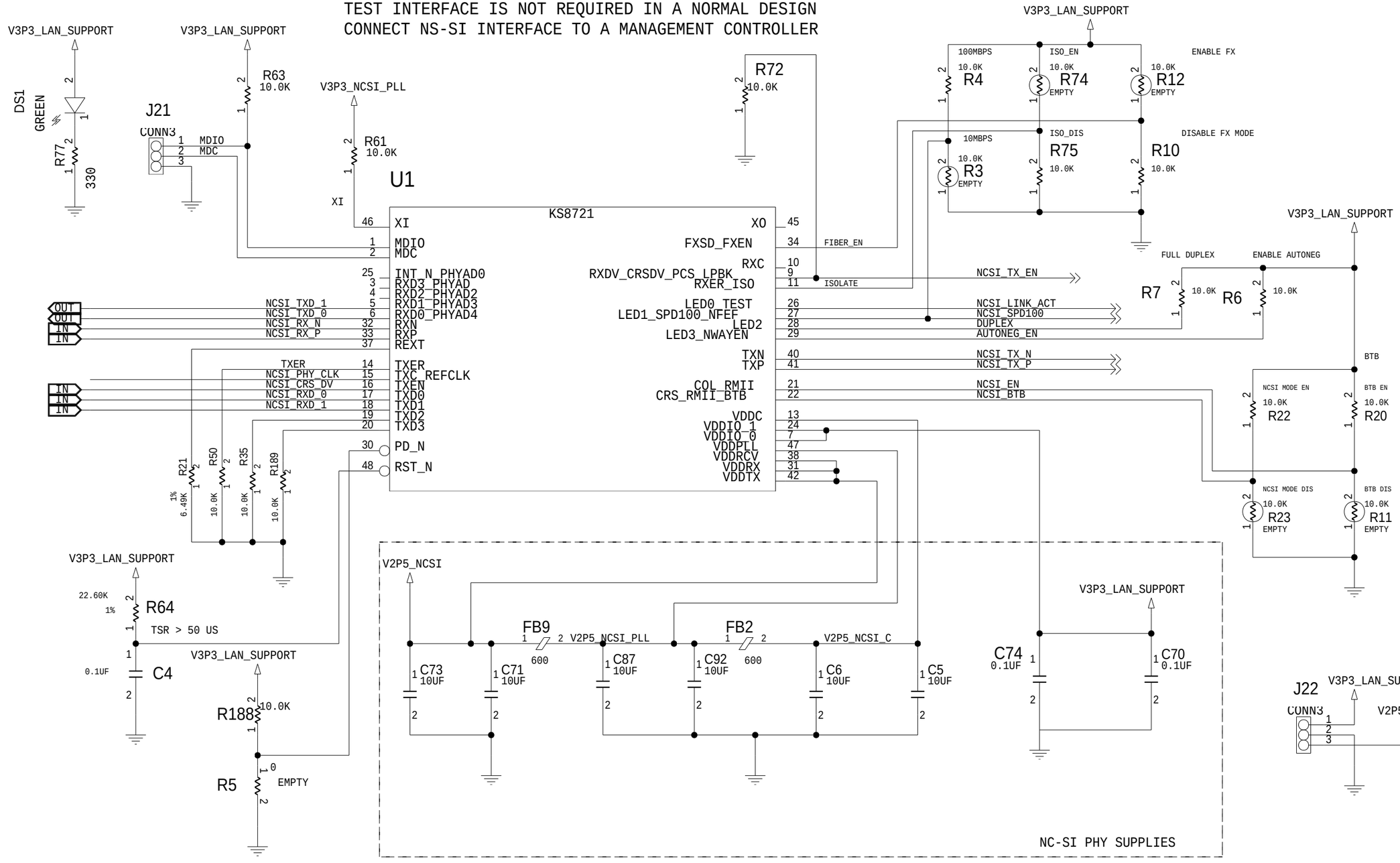
NC-SI TEST INTERFACE

TEST INTERFACE IS NOT REQUIRED IN A NORMAL DESIGN
CONNECT NS-SI INTERFACE TO A MANAGEMENT CONTROLLER



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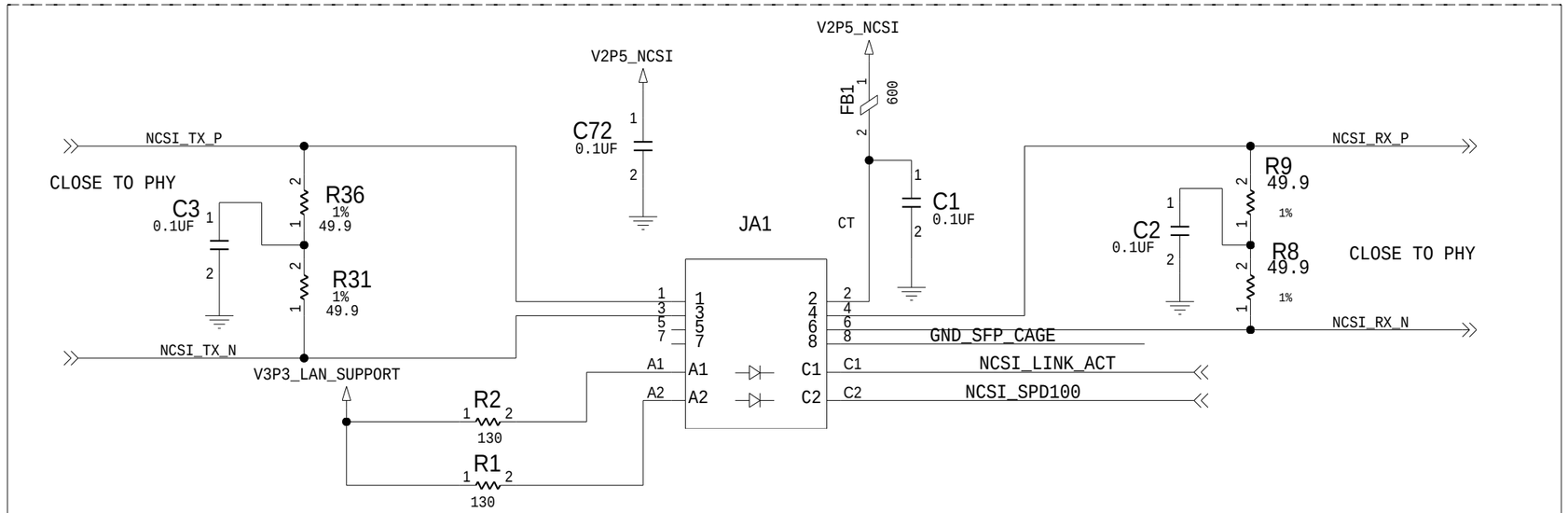
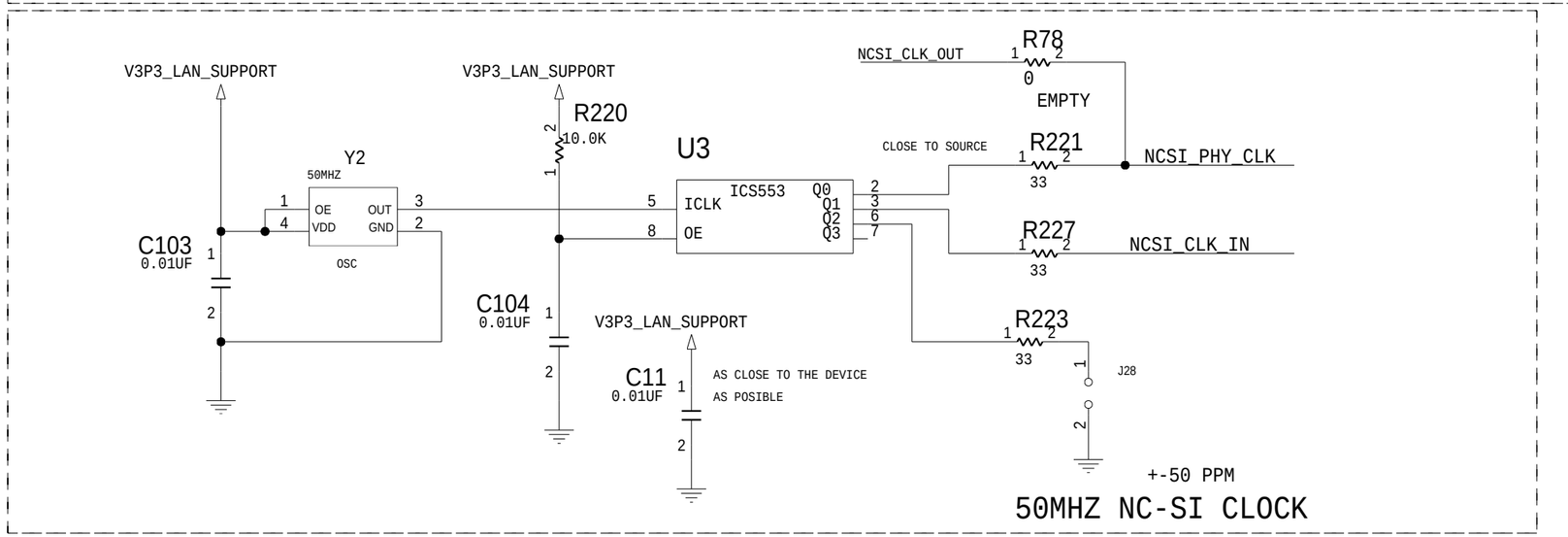
NC-SI TEST INTERFACE

TEST INTERFACE IS NOT REQUIRED IN A NORMAL DESIGN
CONNECT NS-SI INTERFACE TO A MANAGEMENT CONTROLLER





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