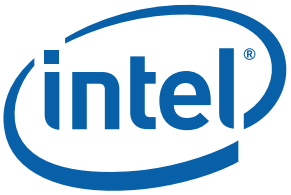

Intel® B460 and H410 Chipset Platform Controller Hub

Specification Update

April 2020

Revision *001*

Document Number: 621886-001

Contents

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Revision History

Revision Number	Description	Release Date
001	• Initial Release	April 2020

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Preface

This document is an update to the specifications contained in the Affected Documents table below. This document is a compilation of device and documentation errata. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents

Title	Document Number
Intel® 400 Series Chipset Family Platform Controller Hub Datasheet	621884 (Vol1) 621885 (Vol2)

Nomenclature

Errata are design defects or errors. Errata may cause the behavior of the PCH to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present in all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

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Summary Tables of Changes

The following tables indicate the errata, specification changes, specification clarifications, or documentation changes which apply to the product. Intel may fix some of the errata in a future stepping of the component and account for the other outstanding issues through documentation or specification changes as noted. These tables use the following notations:

Codes Used in Summary Tables

Status

Doc:	Document change or update will be implemented.
Plan Fix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed in Intel® hardware, firmware, or software.
No Fix:	There are no plans to fix this erratum.

Errata Summary Table

Erratum ID	Stepping	Errata
	A0	
1	No Fix	USB DbC or Device Mode Port When Resuming from S3, S4, S5, or G3 State
2	No Fix	PCIe* Root Port CLKREQ# Asserted Low to Clock Active Timing
3	No Fix	xHCI USB 2.0 ISOCH Device Missed Service Interval
4	No Fix	xHCI Short Packet Event Using Non-Event Data TRB
5	No Fix	For the steppings affected, refer to the Summary Tables of Changes.
6	No Fix	xHCI Host Controller Reset May Cause a System Hang
7	No Fix	SATA Enclosure Management LED Messaging
8	No Fix	Intel® Serial I/O Controller DMA LLP 4 GB Boundary Alignment

Specification Change

Number	Stepping	Specification Change
	A0	
		No specification changes in this revision of the Specification Update

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Errata

1. USB DbC or Device Mode Port When Resuming from S3, S4, S5, or G3 State

Problem: If a PCH USB Type-C* port is configured in Device Mode (or in DbC mode) and connected to an external USB 3.2 host controller, it may cause the USB port to go into a non-functional state in the following scenarios:

1. The PCH resumes from S3, S4, or S5 state, the port may remain in U2.
2. The port is connected to a USB 3.2 Gen 1x1 host controller when resuming from S3, S4, S5 or G3, the port may enter into Compliance Mode or an inactive state if Compliance mode is disabled.
3. The port is connected to a USB 3.2 Gen 2x1 host controller when resuming from S3, S4, S5 or G3, the port may enter an inactive state.

Implication: PCH USB Type-C port configured in Device Mode (or in DbC mode) may fail to enumerate or become unavailable.

Workaround: None identified.

Status: For the steppings affected, refer to the Summary Tables of Changes.

2. PCIe* Root Port CLKREQ# Asserted Low to Clock Active Timing

Problem: During L1 exit, the PCH PCIe* Root Ports may exceed the CLKREQ# asserted low to clock active maximum specification due to PCH PCIe clock un-gate path delays.

Implication: PCIe end point device L1 exit instabilities may be observed.

Note: PCIe end point devices that message LTR latency greater than or equal to 1 µs are not affected by this.

Workaround: None identified.

- Platforms not supporting S0ix with PCIe end point devices that do not support LTR may disable the associated PCH SRCCLKREQ# signal to keep the PCIe clock active during L1.
- Platforms supporting S0ix with PCIe end point devices that have LTR latencies less than 1 µs may disable the associated PCH SRCCLKREQ# signal to keep the PCIe clock active during L1.

Status: For the steppings affected, refer to the Summary Tables of Changes.

3. xHCI USB 2.0 ISOCH Device Missed Service Interval

Problem: When the xHCI controller is stressed with concurrent traffic across multiple USB ports, the xHCI controller may fail to service USB 2.0 Isochronous IN endpoints within the required service interval.

Implication: USB 2.0 isochronous devices connected to the xHCI controller may experience dropped packets.

Note: This issue has only been observed in a synthetic environment.

Workaround: None identified.

Status: For the steppings affected, refer to the Summary Tables of Changes.

4. xHCI Short Packet Event Using Non-Event Data TRB

Problem: The xHCI may generate an unexpected short packet event for the last transfer's Transfer Request Block (TRB) when using Non-Event Data TRB with multiples TRBs.

Implication: Transfer may fail due to the packet size error.

Note: This issue has only been observed in an synthetic environment. No known implication has been identified with commercial software.

Workaround: None identified.

Intel recommends software to use Data Event TRBs for short packet completion.

Status: For the steppings affected, refer to the Summary Tables of Changes.

5. eSPI SBLCL Register Bit Not Cleared by PLTRST#

Problem: The IOSF-SB eSPI Link Configuration Lock (SBLCL) bit (offset 4000h, bit 27 in eSPI PCR space) is reset by RSMRST# assertion instead of PLTRST# assertion.

Implication: If the SBLCL bit is set to 1, software will not be able to access the eSPI device Capabilities and Configuration register in the reserved address range (0h - 7FFh) until RSMRST# asserts.

Workaround: None identified.

If software needs to access the eSPI device reserved range 0h - 7FFh while SBLCL bit is set to 1, a RSMRST# assertion should be performed.

Status: For the steppings affected, refer to the Summary Tables of Changes.

6. xHCI Host Controller Reset May Cause a System Hang

Problem: The xHCI host controller may fail to response if either of the two actions are performed:

1. Accessing xHCI configuration space within 1 ms of setting the xHCI HCRST (Host Controller Reset) bit of the USB Command Register (xHC IBAR, offset 80h,Bit[1]), or
2. Setting the HCRST bit two times within 120 ms.

Implication: The system may hang.

Workaround: None identified.

Note: Software must not make any accesses to the xHCI Host Controller registers for 1 ms after setting the HCRST bit 1 of the USB Command Register (xHCI BAR + 80h) and must add a 120 ms delay in between consecutive xHCI host controller resets.

Status: For the steppings affected, refer to the Summary Tables of Changes.

7. SATA Enclosure Management LED Messaging

Problem: When sending a SATA enclosure LED message and all SATA ports are either idle or disabled, the PCH may not transmit the LED message due to an internal clock gating issue.

Implication: The LED status for SATA enclosure may be incorrect.

Workaround: None Identified.

Note: Enclosure Management SW can poll the Enclosure Management (EM_CTL) - Offset 20h bit 8 register for a 0 value immediately before writing LED messages.

Status: For the steppings affected, refer to the Summary Tables of Changes.

8. Intel® Serial I/O Controller DMA LLP 4 GB Boundary Alignment

Problem: If software assigns a 4 GB-aligned address to the Linked List Pointer (LLP_LOn = 0h) for Intel® Serial I/O Controller DMA engine, then the DMA engine interprets this as an empty link list and will not perform DMA transfers.

Implication: An Intel Serial IO controller (i.e., I2C, GSPI, or UART) may stop operating which may cause the system to hang.

Workaround: Driver software should not assign LLP to a 4 GB-aligned address.

Note: This issue has been addressed in the Intel Serial IO drivers in the following versions or later: For Microsoft* Windows* 10, I2C device driver rev 30.100.1724.2, SPI device driver rev 30.100.1725.1, and UART device driver rev 30.100.1725.1.

Status: For the steppings affected, refer to the Summary Tables of Changes.

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Specification Change

There are no Specification Changes in this revision of the Specification Update.

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