

2D Graphics FPGA IP

The 2D Graphics FPGA IP is a complete solution for adding 2D graphics capability to programmable SoCs.

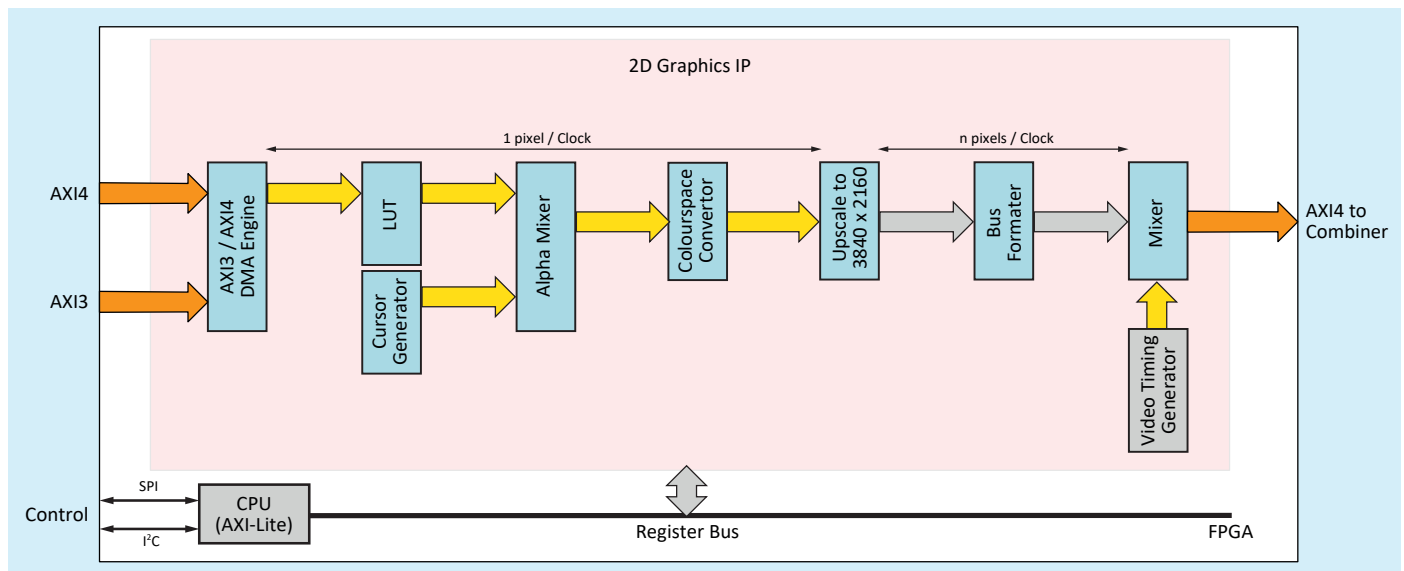


Figure 1. Functional block diagram of the 2D Graphics FPGA IP

Key Features

- Frame Buffer canvas up to 1920x1080 pixels
- Output up to 3840 x 2160
- Support for frame rates up to 120Hz
- Low latency output
- Choice of 16 bits (5:6:5 RGB) or 32 bits (8:8:8:8 RGBA) per pixel
- Configurable Output Colour Matrix
- Dedicated cursor firmware, offloading task of cursor generation from software
- Optional timing generator to allow stand-alone operation (Module output gen-locked to a reference signal via a timing generator)
- Use of AXI4-S for pixel interfaces allows blending of live video with content of Frame Buffer in Intel OSD (on-screen display)
- Implementation demonstrated in RTVE reference design.
- Software control of Output Colour Matrix
- Software control of firmware-accelerated cursor
- Linux Frame Buffer driver

Summary

The 2D Graphics FPGA IP is a complete solution for adding 2D graphics capability to programmable SoCs. This IP allows computer generated 2-dimensional graphics to be rendered as a video frame that can then be overlaid onto a live video stream.

The 2D Graphics IP uses three main AXI4 compliant interfaces:

- An AXI4-MM interface to connect to the SDRAM
- An AXI4-S interface for video output
- An AXI4-Lite interface to allow software control

Applications

The 2D Graphics FPGA IP can be used in a range of applications including:

- On-screen user interfaces
- Overlay of graphical elements, such as measurements, highlights and warnings on live images.
- Test Pattern Generation
- VR and AR Heads-up displays



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