SOLUTION BRIEF

Programmable Solutions
FPGA Video and Vision

SDI Gearbox/Converter FPGA IP

The SDI FPGA IP and other highly optimised FPGA IP cores are building blocks that are combined to provide SDI format gearbox and conversion functionality.

Summary

The SDI (Serial Digital Interface) FPGA IP and other highly optimised FPGA IP cores are building blocks that can be combined to provide SDI format gearbox and conversion functionality. Gearbox functionality allows any SDI video format of one link type, for example quad link 3G-SDI, to be converted to another link type with the same frame rate and color space, for example 12G-SDI. Conversion functionality allows the conversion of any SDI video link type, image size, frame rate or color space to be converted to any other.

Intel® provides a large range of complementary IP cores for video processing and connection. These IP cores can be used individually or in combination to provide FPGA solutions for applications in broadcast, AV, aerospace/defence, medical and automotive industries. Intel IP cores can be supplied as discrete blocks for inclusion in your own designs, as single chip solutions or Intel Design Services can provide a bespoke solution which can be tailored to your specific needs.

The following are some typical examples of the implementation of Intel's IP Cores for SDI format Gearbox and conversion.

Example of 4K60 2 Sample Interleave Gearbox

SMPTE SDI specifications define the use of 2 sample interleave (2SI) as the method of encoding video for 4K and UHD TV over quad 3G-SDI and single link 6G-SDI or 12G-SDI links.

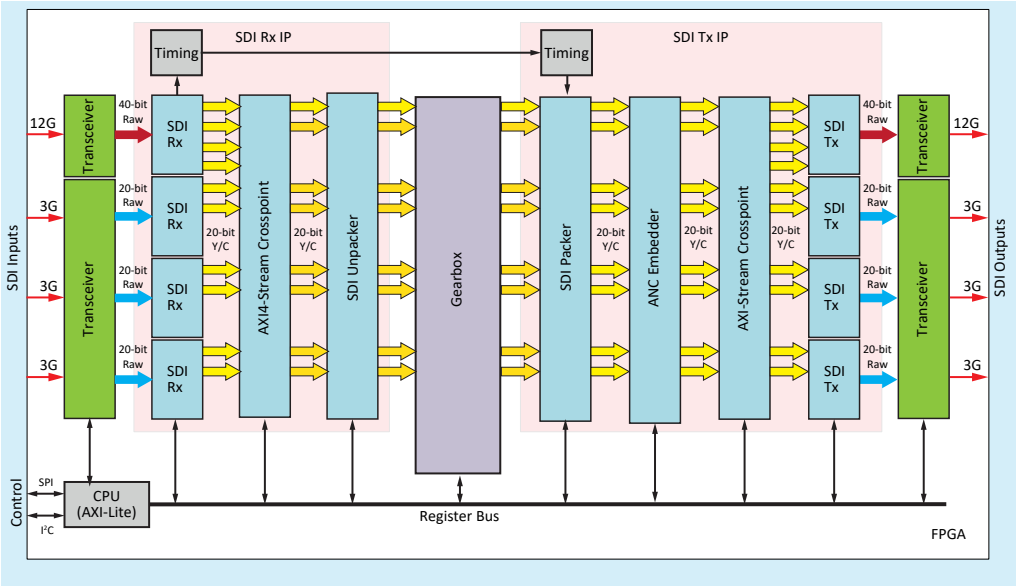

Figure 1. Functional block diagram of 4K60 2 Sample Interleave Gearbox FPGA IP

This diagram shows a typical implementation of Intel's SDI IP to support 2 sample interleave SDI format gearbox functionality.

Here the SDI Rx IP is connected to a Gearbox block and the output of the Gearbox block is connected to the SDI Tx IP.

The IP blocks are configured by an on-chip processor (for example ARM). This allows the selection of the individual links that make up the SDI video signal and the SMPTE virtual video streams that are contained within each link.

The Gearbox re-orders the input video and ancillary data to the chosen output video format.

The Intel GT (graphics technology) Cores simplify the connection of each SDI link's serial data steam into parallel data ready for processing by the other IP blocks

Example of 4K60 2SI + Square Division Gearbox

Early developers of 4K equipment adopted a square division approach to transferring 4K material over quad link 3G-SDI where each link is effectively a standard HD (1920x1080) image. Although square division was easier to adopt it is much harder to process and adds delay, hardware and cost.

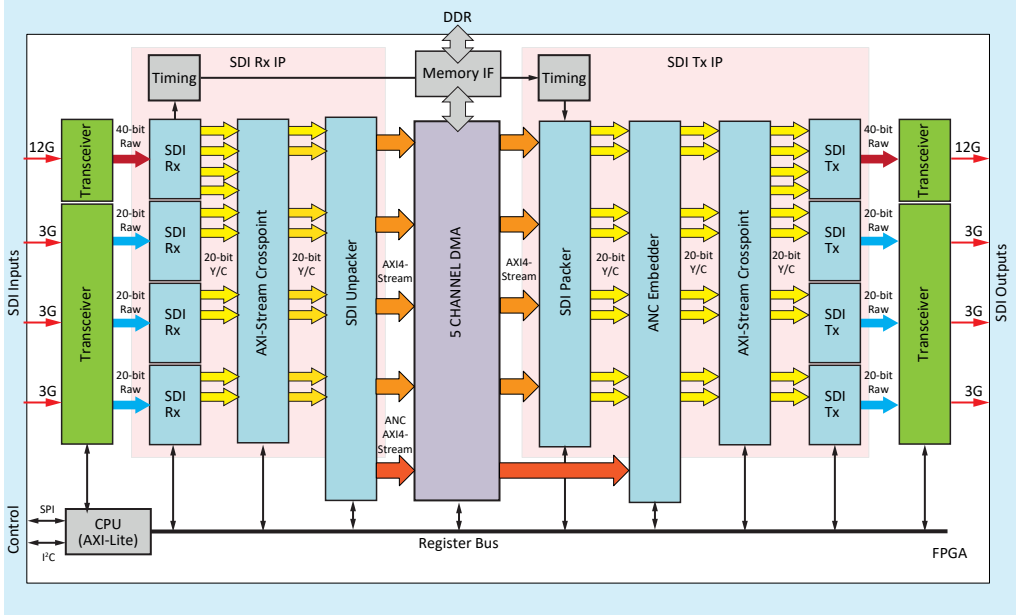

Figure 2. Functional block diagram of 4K60 2SI + Square Division Gearbox FPGA IP

This diagram shows a typical implementation of SDI IP to support both square division and 2 sample interleave SDI format gearbox functionality.

Here the SDI Rx IP is connected to a 5 channel DMA block that allows the pixel data to be reordered (in the example; from square division to 2 sample interleave). The output of the DMA block is connected to the SDI Tx IP.

The IP blocks are configured by an on-chip processor (for example; ARM or any AXI4-Lite CPU). This allows the selection of the individual links that make up the SDI video signal and the SMPTE virtual video streams that are contained within each link.

The memory interface controls the DMA access to externally connected DDR memory.

Example of SDI Cross Converter

Where conversion from one SDI video format (link type, image size, frame rate and color space) to another is required, the OSVP (Omnitek Scalable Video Processor) FPGA IP Core can be used with the SDI IP Cores to allow image size, frame rate and color space conversion.

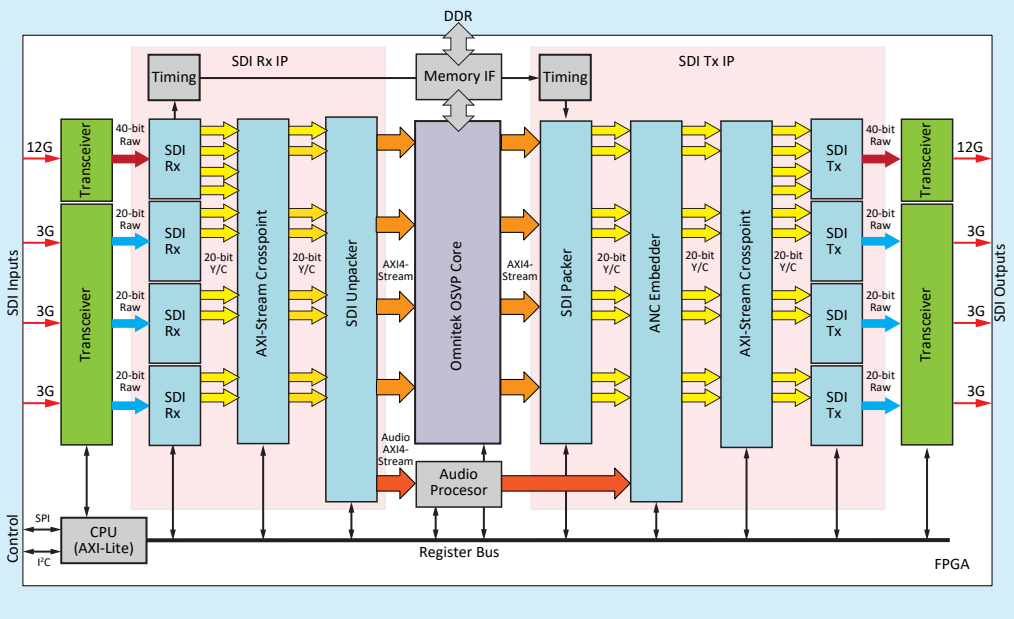

Figure 3. Functional block diagram of SDI Cross Converter FPGA IP

This diagram shows a typical implementation of the SDI IP and the OSVP IP Cores to provide video format conversion functionality.

Here the SDI Rx IP is connected to the OSVP IP Core which allows the input video image to be re-sized, the frame rate converted and the color space converted. The output of the OSVP IP Core is connected to the SDI Tx IP.

The memory interface controls the DMA access to externally connected DDR memory.

In all these examples the IP Blocks are controlled using an ARM processor or any AXI4-Lite CPU.

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