

Image Stitch FPGA IP

The Image Stitch FPGA IP is a highly configurable FPGA IP core for real time image stitching of up to 8 video streams into a single 4K/UHD video stream.

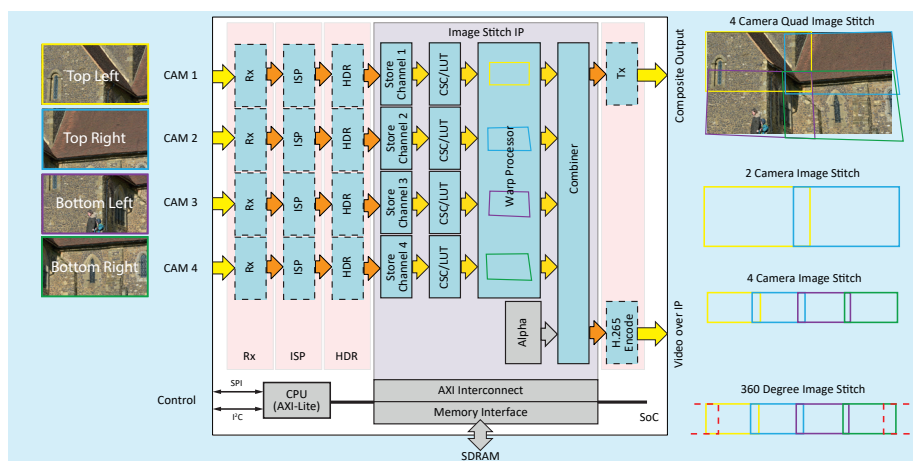


Figure 1. Image Stitch FPGA IP block diagram

Reference frames are captured at regular intervals from the live video streams and the CPU calculates the overlap and individual warps that need to be applied to the images to correctly stitch them together.

The Image Stitch FPGA IP can be used with the range of connectivity IP including SDI Rx, HDMI Rx, DisplayPort Rx, LVDS Rx, etc. and can be used with the ISP IP (to process the RAW sensor images) and HDR Tone-mapping IP (to improve image dynamic range and contrast).

Applications

The Image Stitch FPGA IP can be used in a range of applications including:

- 360° video capture and streaming
- Video conferencing systems requiring surround view
- Automotive surround view camera systems
- Surveillance systems
- Virtual Reality and Augmented Reality Headsets

Summary

The Image Stitch FPGA IP is a highly configurable and optimised FPGA IP core for real time image stitching of up to 8 video streams into a single 4K / UHD video stream.

The Image Stitch FPGA IP employs FPGA hardware to perform real time image stitching using image coordinates calculated using software running on the FPGA CPU.

Image Stitch FPGA IP Sub Blocks

The **Rx IP** block optionally provides SDI Rx, HDMI Rx, DisplayPort Rx, LVDS Rx or TTL Rx input connectivity to the Image Stitch IP.

Up to 8 channels of video from the Rx Connectivity IP are passed to the **Image Store** blocks. Here snapshots are taken at regular intervals and accessed by the Image Stitch software running on the CPU.

Video from the **Image Store** blocks are passed to the corresponding **CSC/LUT** blocks (Color Space Converter / Look-up Table blocks) where image colour correction is performed to match the video streams under control of the CPU.

The **Warp Processor** block manipulates the separate image streams using high level instructions from the CPU.

The **Combiner** block combines the image streams and blends them using the computer generated Alpha channel held in the Alpha block.

The **AXI-Stream Crosspoint** block routes a combined image stream to the appropriate Tx Connectivity IP output.

The **Tx IP** block optionally provides SDI Tx, HDMI Tx, DisplayPort Tx, LVDS Tx, TTL Tx or V-by-one Tx output connectivity.

Image streams are stored and manipulated in external SDRAM via the **AXI Interconnect** and **Memory Interface** blocks.

Key Features

- Automatic image geometry correction of up to 8 video streams
- Automatic white balance and colour correction
- Intelligent edge blending
- 4 quadrant image stitch, creating a 4K composite from 4 HD images
- 2-8 camera horizontal image stitch and 360o surround view
- 2-8 camera vertical image stitch
- Perspective or 360o video mapping
- Support for image sizes up to 4096 x 2160 at 60fps as 8, 10 and 12-bit, 4:2:0, 4:2:2 and 4:4:4.
- Composite output image up to 4096 x 2160 at 60fps as 8, 10 and 12-bit, 4:2:0, 4:2:2 and 4:4:4
- GUI control via web browser interface
- Efficient external memory interface
- 10-bit, RGB, 4:4:4 processing with 8, 10 and 12-bit, 4:2:0, 4:2:2 and 4:4:4 Rx/Tx interfaces

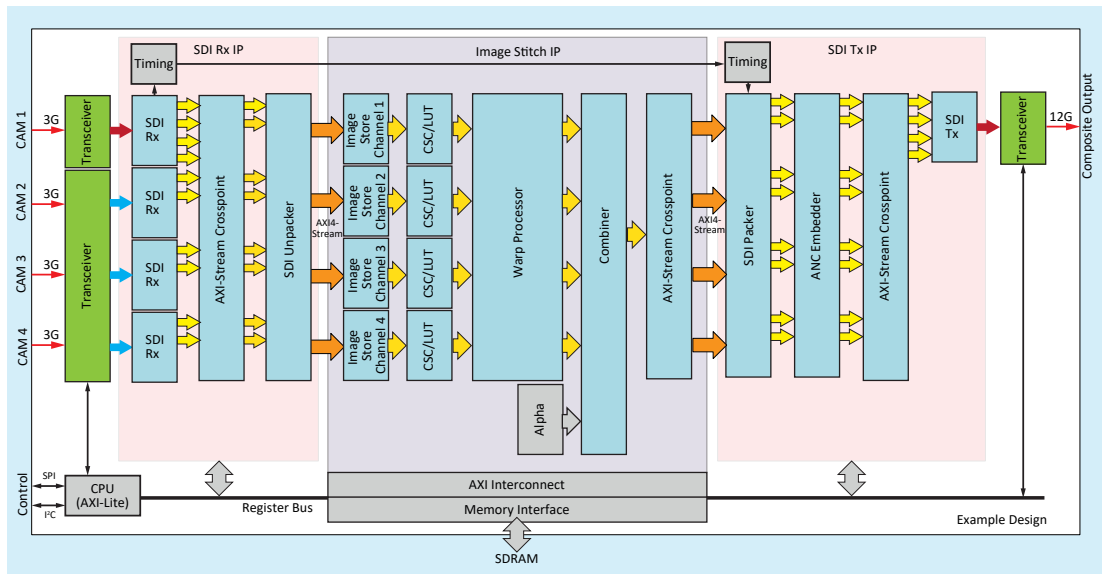
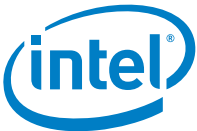


Figure 2. Block diagram



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