# Intel® 500 Series Chipset Family On-Package Platform Controller Hub (PCH)

## Specification Update

***November 2020***

***Revision 003***

Document Number: 630747-003

# Contents



§ §

# Revision History

| Revision | Description | Date |
|---|---|---|
| 001 | • Initial Release | August 2020 |
| 002 | • Added -<br>— Unexpected Shutdown with VCCIN_AUX Retention Mode Enabled<br>— Time-Sensitive Networking Incorrectly Advertised RX FIFO Size (for IoT Platforms only)<br>— xHCI Serial Bus Release Number Version | October 2020 |
| 003 | • Added -<br>— SX_EXIT_HOLDOFF# Not Functional with eSPI Enabled | November 2020 |

§ §

# Preface

This document is an update to the specifications contained in the Affected Documents table below. This document is a compilation of device and documentation errata, specification changes, and specification clarifications. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

## Affected Documents

| Title | Document Number |
|---|---|
| Intel® 500 Series Chipset Family On-Package Platform Controller Hub (PCH) Datasheet, Volume 1 of 2 | 631119 |
| Intel® 500 Series Chipset Family On-Package Platform Controller Hub (PCH) Datasheet, Volume 2 of 2 | 631120 |
| 11th Gen Intel® Core™ Processor Family for IoT Platforms - Datasheet Addendum | 632133 |

## Nomenclature

**Errata** are design defects or errors. Errata may cause the behavior of the PCH to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present in all devices.

**Specification Changes** are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

**Specification Clarifications** describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

§ §

# Summary Tables of Changes

The following tables indicate the errata, specification changes, specification clarifications, or documentation changes which apply to the product. Intel may fix some of the errata in a future stepping of the component and account for the other outstanding issues through documentation or specification changes as noted. These tables use the following notations:

## Codes Used in Summary Tables

### Stepping

| | |
|---|---|
| X: | Erratum exists in the stepping indicated. Specification Change that applies to the stepping indicated. |
| (No mark) or (Blank box): | This erratum is fixed or not applicable in listed stepping or Specification Change does not apply to listed stepping. |

### Status

| | |
|---|---|
| Doc: | Document change or update will be implemented. |
| Plan Fix: | This erratum may be fixed in a future stepping of the product. |
| Fixed: | This erratum has been previously fixed in Intel® hardware, firmware, or software. |
| No Fix: | There are no plans to fix this erratum. |

## Errata

| Erratum ID | Stepping | Errata |
|---|---|---|
| | B0 | |
| 1 | No Fix | USB DbC Or Device Mode Port When Resuming From S3, S4, S5, or G3 State |
| 2 | No Fix | xHCI Power Management Link Timer |
| 3 | No Fix | xHCI USB 2.0 ISOCH Device Missed Service Interval |
| 4 | No Fix | SPI SFDP Program Suspend And Program Resume Instruction Fields Not Used |
| 5 | No Fix | Intel® Trace Hub Pipe Line Empty |
| 6 | No Fix | xHCI Short Packet Event Using Non-Event Data TRB |
| 7 | No Fix | eSPI SBLCL Register Bit Not Cleared By PLTRST# |
| 8 | No Fix | xHCI Protocol Speed ID Count Field |
| 9 | No Fix | S0ix Entry When Connecting an USB-C* Power Adapter |
| 10 | No Fix | Unexpected Shutdown with VCCIN_AUX Retention Mode Enabled |
| 11 | No Fix | Time-Sensitive Networking Incorrectly Advertised RX FIFO Size (for IoT Platforms only) |
| 12 | No Fix | xHCI Serial Bus Release Number Version |

## Specification Changes

| Number | Stepping | Specification Changes |
|---|---|---|
| | B0 | |
| | | No specification changes in this revision of the Specification Update |

## Specification Clarification

| Number | Specification Clarification |
|---|---|
| 1 | SX_EXIT_HOLDOFF# Not Functional with eSPI Enabled |

§ §

# Errata

## 1. USB DbC Or Device Mode Port When Resuming From S3, S4, S5, or G3 State

Problem: If a PCH USB 3.2 Type-C port is configured in Device Mode (or in DbC mode) and connected to an external USB 3.2 host controller, it may cause the USB port to go into a non-functional state in the following scenarios:

1. The PCH resumes from S3, S4, or S5 state, the port may remain in U2.
2. The port is connected to a USB 3.2 Gen 1x1 host controller when resuming from S3, S4, S5, or G3, the port may enter into Compliance Mode or an inactive state if Compliance mode is disabled.
3. The port is connected to a USB 3.2 Gen 2x1 host controller when resuming from S3, S4, S5, or G3, the port may enter an inactive state.

Implication: PCH USB Type-C port configured in Device Mode (or in DbC mode) may fail to enumerate or become unavailable.

Workaround: None identified.

Status: For the steppings affected, refer the "Summary Tables of Changes".

## 2. xHCI Power Management Link Timer

Problem: The xHCI implements the Power Management Link Timer (PM LC Timer) Timeout value as 10 us instead of 4 us as defined by the USB 3.2 specification.

Implication: USB-IF xHCI CV TD 7.21 may report a failure. Intel has obtained a waiver for TD 7.21.

*Note:* No functional issues are expected.

Workaround: None identified.

Status: For the steppings affected, refer the "Summary Tables of Changes".

## 3. xHCI USB 2.0 ISOCH Device Missed Service Interval

Problem: When the xHCI controller is stressed with concurrent traffic across multiple USB ports, the xHCI controller may fail to service USB 2.0 Isochronous IN endpoints within the required service interval.

Implication: USB 2.0 isochronous devices connected to the xHCI controller may experience dropped packets.

*Note:* This issue has only been observed in a synthetic environment.

Workaround: None identified.

Status: For the steppings affected, refer the "Summary Tables of Changes".

## 4. SPI SFDP Program Suspend And Program Resume Instruction Fields Not Used

Problem: For flash device suspend/resume opcodes, the SPI controller does not use JEDEC SFDPs 13th DWORD bits [15:0], Program Suspend Instruction and Program Resume Instruction fields. The controller only uses bits [31:16], Suspend Instruction and Resume Instruction fields, to obtain the suspend/resume opcodes.

Implication: If the SPI flash requires bits [15:0] to be different than bits [31:16], then the suspend /resume feature is not functional. In this case, system behavior varies depending on what the suspend/resume instruction is and when it is generated.

*Note:* Major flash vendors have been using the same value for bits [31:16] and bits [15:0].

Workaround: None identified.

If a device requires bits [15:0] to be different than bits [31:16], then disable the device suspend / resume via the SPI Suspend / Resume Enable soft strap.

Status: For the steppings affected, refer the "Summary Tables of Changes".

## 5. Intel® Trace Hub Pipe Line Empty

Problem: The Intel® Trace Hub Pipe Line Empty bit (CSR_MTB_BAR, Offset D4h) for a given output port may be set while the Input Buffer Empty for the associated output port is not set. This will only happen when the captureDone signal is de-asserted by clearing the ForceCaptureDone bit (CSR_MTB_BAR, Offset D8h) is cleared or the StoreQual[0] signal is de-asserted by the Trigger Unit before the pipe line is empty, and the destination is either system memory or USB (DCI).

Implication: There may be valid trace data in the trace source input buffer which did not get sent to the destination (output port).

Workaround: None identified.

CaptureDone should be cleared or de-asserted after the pipe line is empty.

Status: For the steppings affected, refer the "Summary Tables of Changes".

## 6. xHCI Short Packet Event Using Non-Event Data TRB

Problem: The xHCI may generate an unexpected short packet event for the last transfer's Transfer Request Block (TRB) when using Non-Event Data TRB with multiples TRBs.

Implication: Transfer may fail due to the packet size error.

*Note:* This issue has only been observed in an synthetic environment. No known implication has been identified with commercial software.

Workaround: None identified.

Intel recommends software to use Data Event TRBs for short packet completion.

Status: For the steppings affected, refer the "Summary Tables of Changes".

## 7. eSPI SBLCL Register Bit Not Cleared By PLTRST#

Problem: The IOSF-SB eSPI Link Configuration Lock (SBLCL) bit (offset 4000h, bit 27 in eSPI PCR space) is reset by RSMRST# assertion instead of PLTRST# assertion.

Implication: If the SBLCL bit is set to 1, software will not be able to access the eSPI device Capabilities and Configuration register in the reserved address range (0h - 7FFh) until RSMRST# asserts.

Workaround: None identified.

If software needs to access the eSPI device reserved range 0h - 7FFh while SBLCL bit is set to 1, a RSMRST# assertion should be performed.

Status: For the steppings affected, refer to the "Summary Tables of Changes".

## 8. xHCI Protocol Speed ID Count Field

Problem: The xHCI Host Controller reports an incorrect Protocol Speed ID Count value for the USB 3.2 Supported Protocol Capability register - xHCI MMIO offset 8028 bits [31:28].

Implication: USB-IF xHCI CV TD 1.9 may report a failure.

*Note:* No functional impact is expected.

Workaround: None identified.

Status: For the steppings affected, refer the "Summary Tables of Changes".

## 9. S0ix Entry When Connecting an USB-C* Power Adapter

Problem: Connecting a USB-C* power adapter to a PCH USB port may cause a race condition that can prevent the system from entering S0ix. This issue only occurs on designs where the USB-C Power Delivery (PD) implements Out Of Band (OOB) messaging to communicate with the PCH for port mapping.

Implication: The system may fail to enter S0ix.

Workaround: None identified.

Status: For the steppings affected, refer the "Summary Tables of Changes".

## 10. Unexpected Shutdown with VCCIN_AUX Retention Mode Enabled

Problem: Due to a PMC logic bug, the FIVR may unexpectedly shutdown during C10 exit when retention mode is enabled for VCCIN_AUX.

Implication: The system may unexpectedly shutdown and requires a global reset cycle to recover.

Workaround: None identified. Due to this erratum, VCCIN_AUX retention mode is not supported and should be disabled. BIOS Reference Code Revision 3357.02 or later disables VCCIN_AUX retention mode by default.

Status: For the steppings affected, refer the "Summary Tables of Changes".

## 11. Time-Sensitive Networking Incorrectly Advertised RX FIFO Size (for IoT Platforms only)

Problem: The Time-Sensitive Networking (TSN) controller MTL Receive FIFO Size (RXFIFOSIZE) bits [4:0] in register MAC_HW_FEATURE1 (MMIO offset 120h) advertises 32 KB as the allowable RX FIFO size, while the implemented size is 24 KB.

Implication: The maximum aggregate size for MTL RX queues is 24 KB. If software allocation of RX queues exceeds this amount, then data attempted to be queued greater than 24 KB will be lost.

Workaround: None identified. Software should not allocate an aggregate size of more than 24 KB for MTL RX queues.

Status: For the steppings affected, refer the "Summary Tables of Changes".

## 12. xHCI Serial Bus Release Number Version

Problem: The xHCI Host Controller reports the value of 31h for the Serial Bus Release Number (SBRN) register (offset 60h), which does not meet the xHCI specification revision 1.2.

Implication: USB-IF xHCI CV TD 1.1 may report a failure. Intel has obtained a waiver for TD 1.1.

*Note:* There are no known functional failures due to this erratum.

Workaround: None identified.

Status: For the steppings affected, refer the "Summary Tables of Changes".

§ §

# Specification Changes

There are no specification changes in this revision of the Specification Update.

§ §

# Specification Clarification

## 1. SX_EXIT_HOLDOFF# Not Functional with eSPI Enabled

Add the following note to the Intel® 500 Series Chipset Family On-Package Platform Controller Hub (PCH) Datasheet, Volume 1 of 2 (#631119) in the SX_EXIT_HOLDOFF# Signal Description in the Power Management chapter Signal Description section:

"When eSPI is enabled, SX_EXIT_HOLDOFF# functionality is not available, and assertion of the signal will not impact Sx exit flows."

§ §