11th Generation Intel® Core™ Processor Family

Specification Update

Supporting 11th Generation Intel® Core™ Processor Families, Intel® Pentium® Processors, Intel® Celeron® Processors for UP3, UP3 IOT, and UP4 Platforms, formerly known as Tiger Lake

Revision 004

November 2020

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Contents

Revision History

Revision Number	Description	Revision Date
001	• Initial Revision	September 2020
002	• Added Errata: TGL016, TGL017	September 2020
003	• Added IOT UP3 Processor Line • Added Errata: TGL018, TGL019, TGL020	October 2020
004	• Added Errata: TGL021, TGL022, TGL023, TGL024, TGL025 • Updated Erratum: TGL014 • Added UP3 IOT and UP4 support	November 2020

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Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata, specification clarifications and changes. The document is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this updated document and are no longer published in other documents. This document may also contain information that has not been previously published.

Affected Documents

Document Title	Document Number
11th Generation Intel® Core™ Processor Datasheet, Volume 1 of 2	631121
11th Generation Intel® Core™ Processor Datasheet, Volume 2a of 2	631122

Related Documents

Document Title	Document Number/Location
AP-485, Intel® Processor Identification and the CPUID Instruction	http://www.intel.com/design/processor/applnots/241618.htm
Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 1: Basic Architecture Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2A: Instruction Set Reference Manual A-M Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2B: Instruction Set Reference Manual N-Z Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3A: System Programming Guide Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3B: System Programming Guide Intel® 64 and IA-32 Intel® Architecture Optimization Reference Manual	http://www.intel.com/products/processor/manuals/index.htm
Intel® 64 and IA-32 Architectures Software Developer's Manual Documentation Changes	http://www.intel.com/content/www/us/en/processors/architectures-software-developer-manuals.html
Intel® Virtualization Technology Specification for Directed I/O Architecture Specification	D51397-001
ACPI Specifications	www.acpi.info

Nomenclature

Errata – These are design defects or errors. Errata may cause the processor's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes – These are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Specification Clarifications – This describes a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes – This includes typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications, and documentation changes are removed from the specification update, when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

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Identification Information

Component Identification via Programming Interface

The processor stepping is identified by the following register contents:

Table 2-1. Processor Lines Component Identification

Samples	CPUID	Reserved [31:28]	Extended Family [27:20]	Extended Model [19:16]	Reserved [15:14]	Processor Type [13:12]	Family Code [11:8]	Model Number [7:4]	Stepping ID [3:0]
UP3/UP4	000806C1h	Reserved	0000000b	1000b	Reserved	00b	0110b	1100b	0001b

1. The Extended Family, Bits [27:20] are used in conjunction with the Family Code, specified in Bits[11:8], to indicate whether the processor belongs to the Celeron®, Pentium®, or Intel® Core™ processor family.
2. The Extended Model, Bits [19:16] in conjunction with the Model Number, specified in Bits [7:4], are used to identify the model of the processor within the processor's family.
3. The Family Code corresponds to Bits [11:8] of the EDX register after RESET, Bits [11:8] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the generation field of the Device ID register accessible through Boundary Scan.
4. The Model Number corresponds to Bits [7:4] of the EDX register after RESET, Bits [7:4] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the model field of the Device ID register accessible through Boundary Scan.
5. The Stepping ID in Bits [3:0] indicates the revision number of that model. Refer table above for the processor stepping ID number in the CPUID information.
6. When EAX is initialized to a value of '1', the CPUID instruction returns the Extended Family, Extended Model, Processor Type, Family Code, Model Number and Stepping ID value in the EAX register. The EDX processor signature value after reset is equivalent to the processor signature output value in the EAX register.

Cache and TLB descriptor parameters are provided in the EAX, EBX, ECX and EDX registers after the CPUID instruction is executed with a 2 in the EAX register.

Component Marking Information

Figure 2-1. Based on UP3-Processor Line Multi-Chip Package BGA Top-Side Markings

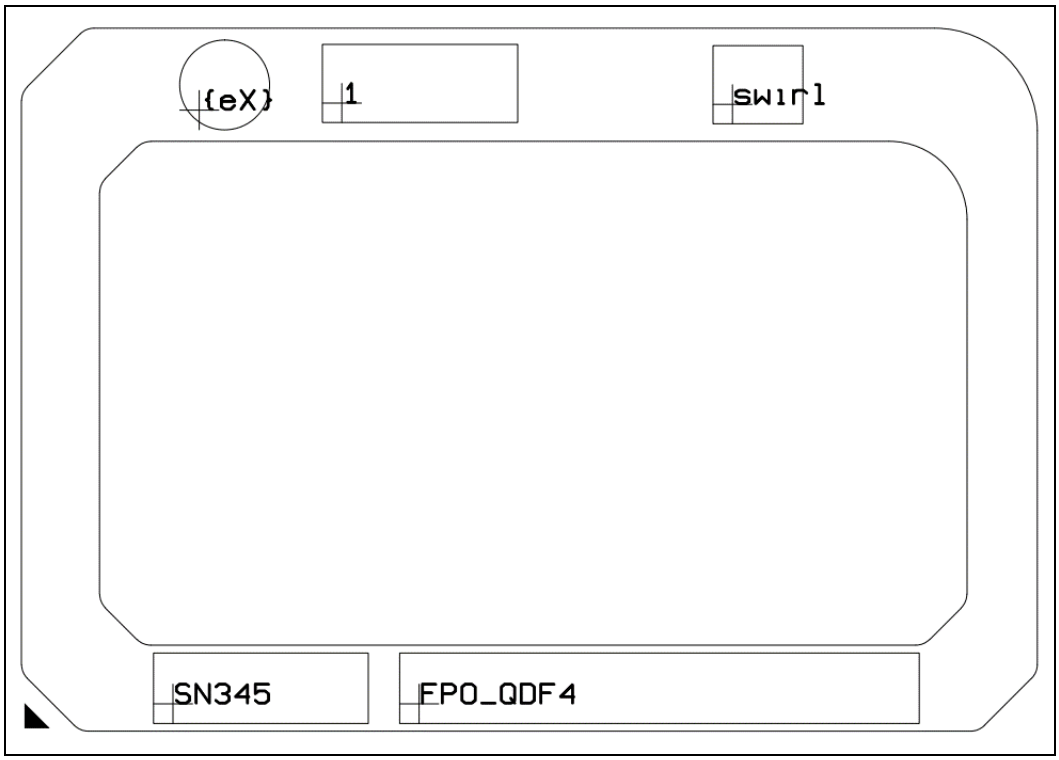
Pin Count: 1449 Package Size: 55.5 mm x 25 mm

Production (SSPEC):

- FPO: FPOxxxxx
- {eX}
- SWIR1: Intel® logo

Note: "1" is used to extract the unit visual ID (2D ID).

Figure 2-2. Processor Based on UP4 Processor Line Multi-Chip Package BGA Top-Side Markings



Pin Count: 1598 Package Size: 26.5 mm x 18.5 m

Production (SSPEC):

Intel logo
BRAND
PROC#
SPEC SPEED
{FPO} {eX}

Note: "1" is used to extract the unit visual ID (2D ID).

Note: Processor list can be found at:
https://ark.intel.com/content/www/us/en/ark/products/codename/88759/products-formerly-tiger-lake.html

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Summary Tables of Changes

The following tables indicate the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the listed processor stepping. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or Specification Changes as noted. These tables use the following notations:

Codes Used in Summary Table

Stepping	Description
(No mark) or (Blank Box)	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Status	Description
Doc	Document change or update that is implemented.
Planned Fix	This erratum may be fixed in a future stepping of the product.
Fixed	This erratum has been previously fixed in Intel® hardware, firmware, or software.
No Fix	There are no plans to fix this erratum.

Errata Summary Table

Erratum ID	Processor Line/ Stepping			Title
	UP3	IOT UP3	UP4	
TGL001	No Fix	No Fix	No Fix	X87 FDP Value May be Saved Incorrectly In Real-Address Mode or Virtual-8086 Mode
TGL002	No Fix	No Fix	No Fix	Debug Exceptions May Be Lost or Misreported When MOV SS or POP SS Instruction is Not Followed By a Write to SP
TGL003	No Fix	No Fix	No Fix	CPUID L2 Cache Information May Be Inaccurate
TGL004	No Fix	No Fix	No Fix	Placing Posted-Interrupt Descriptors Within The PRMRR May Result In a Processor Hang
TGL005	No Fix	No Fix	No Fix	Intel® PT CBR Packet May be Delayed or Dropped
TGL006	No Fix	No Fix	No Fix	Intel® PT TIP or FUP Packets May be Dropped Without OVF Packet
TGL007	No Fix	No Fix	No Fix	Overflow Flag in IA32_MC0_STATUS MSR May be Incorrectly Set
TGL008	No Fix	No Fix	No Fix	An Exception During a 32-bit Mode Task Switch With CET Enabled May Lead to an Incorrect TSS Busy Flag Value
TGL009	No Fix	No Fix	No Fix	Exit Qualification For EPT Violations Incorrectly Indicate On Instruction Fetches That The Guest-Physical Address Was Writeable
TGL010	No Fix	No Fix	No Fix	Processor May Generate Spurious Page Faults On Shadow Stack Pages
TGL011	No Fix	No Fix	No Fix	HDMI 1.4 Inter-Pair Skew Test May Fail
TGL012	No Fix	No Fix	No Fix	Intel® PT ToPA Tables Read From Non-Cacheable Memory During an Intel® TSX Transaction May Lead to Processor Hang
TGL013	No Fix	No Fix	No Fix	Performing an XACQUIRE to an Intel® PT ToPA Table May Lead to Processor Hang
TGL014	No Fix	No Fix	No Fix	PECI Frequency Limited to 32Kbps-1Mbps
TGL015	No Fix	No Fix	No Fix	PCIe Gen4 JTOL – Jitter Tolerance Compliance Test May Fail
TGL016	Fixed	Fixed	N/A	System May Fail To Exit Warm Reset or S3
TGL017	No Fix	No Fix	No Fix	Unable to Transmit Modified Compliance Test Pattern At 2.5 GT/S or 5.0 GT/s Link Speeds
TGL018	No Fix	No Fix	No Fix	MSR IA32_THERM_STATUS CURRENT_LIMIT_STATUS May Report Incorrect Value
TGL019	Fixed	Fixed	N/A	System May Hang During Package-C10 Exit
TGL020	Fixed	Fixed	N/A	Processor May Hang When PROCHOT# is Active
TGL021	No Fix	No Fix	No Fix	Processor May Hang if Warm Reset Triggers During BIOS Initializion
TGL022	Fixed	Fixed	Fixed	PCIe Link_Down May Occur After Exiting From Package C10 Cycle
TGL023	No Fix	No Fix	No Fix	Reported Package Power May Not be Accurate
TGL024	No Fix	No Fix	No Fix	USB TD65 PollingLFPS Duration Test Fail on Direct Port
TGL025	Fixed	Fixed	Fixed	Cache Configuration May be Incorrectly Initialized During Boot

Specification Changes

No.	Specification Changes
001	HDCP 2.2 not supported in certain modes for DP1.4a interface.

Specification Clarifications

No.	Specification Clarifications
	None for this revision of this specification update.

Documentation Changes

No.	Documentation Changes
	None for this revision of this specification update.

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Errata Details

TGL001	X87 FDP Value May be Saved Incorrectly In Real-Address Mode or Virtual-8086 Mode
Problem	Execution of the FSAVE, FNSAVE, FSTENV, or FNSTENV instructions in real-address mode or virtual-8086 mode may save an incorrect value for the x87 FDP (FPU data pointer). This erratum does not apply if the last non-control x87 instruction had an unmasked exception.
Implication	Software operating in real-address mode or virtual-8086 mode that depends on the FDP value for non-control x87 instructions without unmasked exceptions may not operate properly. Intel has not observed this erratum in any commercially available software.
Workaround	None identified. Software should use the FDP value saved by the listed instructions only when the most recent non-control x87 instruction incurred an unmasked exception.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL002	Debug Exceptions May Be Lost or Misreported When MOV SS or POP SS Instruction is Not Followed By a Write to SP
Problem	If a MOV SS or POP SS instruction generated a debug exception, and is not followed by an explicit write to the stack pointer (SP), the processor may fail to deliver the debug exception or, if it does, the DR6 register contents may not correctly reflect the causes of the debug exception.
Implication	Debugging software may fail to operate properly if a debug exception is lost or does not report complete information. Intel has not observed this erratum with any commercially available software.
Workaround	Software should explicitly write to the stack pointer immediately after executing MOV SS or POP SS.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL003	CPUID L2 Cache Information May Be Inaccurate
Problem	CPUID extended function 80000006H (EAX=80000006H) inaccurately reports information about the L2 cache in ECX. The function reports that the L2 cache size is 256K, although the cache size 512K.
Implication	Software that uses CPUID extended leaf 80000006H L2 cache information may operate incorrectly. Intel has not observed this erratum to impact the operation of any commercially available software.
Workaround	None identified. Software should ignore the L2 cache size information reported by CPUID extended leaf 80000006H for the affected processors.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL004	Placing Posted-Interrupt Descriptors Within The PRMRR May Result In a Processor Hang
Problem	Posted-interrupt processing is a virtualization feature for interrupts which requires configuring addresses in the posted-interrupt descriptor fields in the VMCS (Virtual Machine Control Structure). Configuring posted-interrupt descriptors addresses that are within the PRMRR (Processor Reserved Memory Range Register, defined by MSR 1F4H and MSR 1F5H) may result in a logical processor hang.
Implication	This erratum may result in a processor hang. Intel has not observed this erratum with any commercially available software.
Workaround	VMM (Virtual Machine Monitor) software should not use addresses within the PRMRR for posted-interrupt descriptors.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL005	Intel® PT CBR Packet May be Delayed or Dropped
Problem	Due to a complex set of microarchitectural conditions, the Intel® PT (Processor Trace) CBR (Core:Bus Ratio) packet generated on a frequency change may be dropped, without an OVF (Overflow) packet, or may be inserted into the trace late, after other packets (including possibly another CBR) that were generated after the frequency change completed.
Implication	An Intel® PT decoder may report an incorrect core:bus ratio to a portion of the trace, which may result in an incorrect wall clock time calculation.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL006	Intel® PT TIP or FUP Packets May be Dropped Without OVF Packet
Problem	The Intel® PT (Processor Trace) OVF (Overflow) packet may not be generated when only TIPs (Target IP Packets) and/or FUPs (Flow Update Packets) are lost due to internal buffer overflow.
Implication	A decoder error will result from the missing FUP and/or TIP packets.
Workaround	None identified. An Intel® PT decoder will be able to resume proper decode from the next FUP, TIP, or PSB (Packet Stream Boundary) packet. The incidence of error may be mitigated by setting IA32_RTIT_CTL. CYCEn[bit 1] (MSR 0570H) to 1, as an internal buffer overflow that loses a CYC packet will generate an OVF.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL007	Overflow Flag in IA32_MC0_STATUS MSR May be Incorrectly Set
Problem	Under complex micro-architectural conditions, a single internal parity error seen in IA32_MC0_STATUS MSR (401h) with MCACOD (bits 15:0) value of 5h and MSCOD (bits 31:16) value of 7h, may set the overflow flag (bit 62) in the same MSR.
Implication	Due to this erratum, the IA32_MC0_STATUS overflow flag may be set after a single parity error. Intel has not observed this erratum with any commercially available software.
Workaround	None identified.

Status	For the steppings affected, refer to the Summary Table of Changes.

TGL008	**An Exception During a 32-bit Mode Task Switch with CET Enabled may Lead to an Incorrect TSS Busy Flag Value**
Problem	Under complex micro-architectural conditions, in 32Bit mode, the processor may reset the busy (B) flag in the Task State Segment (TSS) descriptor when handling a general protection exception (#GP), a control protection exception (#CP), or a page fault exception (#PF) that happens during a task switch when Control-flow Enforcement Technology (CET) is enabled, indicated by CR4. CET (bit 23).
Implication	Due to this erratum, the TSS descriptor busy flag might be incorrectly written as "not busy" in the TSS descriptor. Intel has not observed this erratum with any commercially available software.
Workaround	Software should restore the busy flag in the TSS descriptor when handling #GP, #CP, or #PF exceptions when CET is enabled.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL009	**Exit Qualification For EPT Violations Incorrectly Indicate On Instruction Fetches That The Guest-Physical Address Was Writeable**
Problem	On EPT violations, bit 4 of the Exit Qualification indicates whether the guest-physical address was writeable. When EPT is configured as supervisory shadow-stack (both bit 60 in EPT paging-structure leaf entry and bit 0 in EPT paging-structure entries are set), non-executable (bit 2 in EPT paging-structure entries is cleared), and non-writeable (bit 1 in EPT paging-structure entries is cleared) a VMExit due to a guest instruction fetch to a supervisory page will incorrectly set bit 4 of the Exit Qualification. Bits 3, 5, and 6 of the Exit Qualification is not impacted by this erratum.
Implication	Due to this erratum, bit 4 of the Exit Qualification may be incorrectly set. Intel has not observed this erratum on any commercially available software.
Workaround	EPT handlers processing an EPT violation due to an instruction fetch access on a present page should ignore the value of bit 4 of the Exit Qualification.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL010	**Processor May Generate Spurious Page Faults On Shadow Stack Pages**
Problem	When operating in a virtualized environment, if shadow stack pages are mapped over an APIC page, the processor will generate spurious page faults on that shadow stack page whenever its linear to physical address translation is cached in the Translation Look-aside Buffer.
Implication	When this erratum occurs, the processor will generate a spurious page fault. Intel is not aware of any software that maps shadow stack pages over an APIC page.
Workaround	Software should avoid mapping shadow stack pages over the APIC page.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL011	HDMI 1.4 Inter-Pair Skew Test May Fail
Problem	Type-C Port (TCP) PHY may fail the HDMI 1. 4 ID7-6 Inter-pair Skew Test for specific thermal corner cases.
Implication	Due to this erratum, the HDMI 1. 4 Inter-pair Skew Test may fail. Intel has only observed this erratum in a synthetic test environment.
Workaround	None Identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL012	Intel® PT ToPA Tables Read From Non-Cacheable Memory During an Intel® TSX Transaction May Lead to Processor Hang
Problem	If an Intel® PT (Processor Trace) ToPA (Table of Physical Addresses) table is placed in UC (Uncacheable) or USWC (Uncacheable Speculative Write Combining) memory, and a ToPA output region is filled during an Intel® TSX (Transaction Synchronization) transaction, the resulting ToPA table read may cause a processor hang.
Implication	Placing Intel® PT ToPA tables in non-cacheable memory when Intel® TSX is in use may lead to a processor hang.
Workaround	None identified. Intel® PT ToPA tables should be located in WB memory if Intel® TSX is in use.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL013	Performing an XACQUIRE to an Intel® PT ToPA Table May Lead to Processor Hang
Problem	If an XACQUIRE lock is performed to the address of an Intel® PT (Processor Trace) ToPA (Table of Physical Addresses) table, and that table is later read by the CPU during the HLE (Hardware Lock Elision) transaction, the processor may hang.
Implication	Accessing ToPA tables with XACQUIRE may result in a processor hang.
Workaround	None identified. Software should not access ToPA tables using XACQUIRE. An OS or hypervisor may wish to ensure all application or guest writes to ToPA tables to take page faults or EPT violations.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL014	PECI Frequency Limited to 32Kbps-1Mbps
Problem	The PECI (Platform Environmental Control Interface) 3. 1 specification's operating frequency range is 2 Kbps to 2 Mbps. Due to this erratum, PECI may be unreliable when operated out of 3. 2Kbps-1Mbps range.
Implication	Platforms attempting to run PECI out of 3. 2Kbps-1Mbps range may not behave as expected.
Workaround	None identified. Platforms should limit PECI operating frequency to 3. 2Kbps-1Mbps range.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL015	PCIe Gen4 JTOL – Jitter Tolerance Compliance Test May Fail
Problem	The processor may not meet the PCI Express M. 2 Specification Revision 4. 0, Version 0. 9 receiver Jitter Tolerance (JTol) Minimum Receiver Path Sensitivity requirements when operating at 16.0 GT/s under high temperature conditions.
Implication	Due to this erratum, the processor may exceed receiver jitter tolerance limits when tested at high temperature conditions. Intel has not observed any impact to functional behavior or nominal PCIe compliance testing.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL016	System May Fail To Exit Warm Reset or S3
Problem	The processor may fail to access system memory if memory frequency changes between entry and exit of warm reset or S3.
Implication	When this erratum occurs the system may hang.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL017	Unable to Transmit Modified Compliance Test Pattern At 2.5 GT/S or 5.0 GT/s Link Speeds
Problem	The processor's PCIe port (Bus 0, Device 6, Function 0) does not transmit the Modified Compliance Test Pattern when in either 2. 5 GT/S or 5. 0 GT/s link speeds.
Implication	Due to this erratum, PCIe compliance testing may fail at 2. 5 GT/S or 5. 0 GT/s link speeds when enabling Modified Compliance Test Pattern.
Workaround	None Identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL018	MSR IA32_THERM_STATUS CURRENT_LIMIT_STATUS May Report Incorrect Value
Problem	During a thermal event, MSR IA32_THERM_STATUS (19Ch) CURRENT_LIMIT_STATUS bit 12 may not reflect the proper value.
Implication	Due to this erratum, software may not be able to determine the cause of the frequency limitation.
Workaround	None Identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL019	System May Hang During Package-C10 Exit
Problem	When exiting Package C10 the system may draw excessive current.
Implication	Due to this erratum, the system may hang.

Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL020	**Processor May Hang When PROCHOT# is Active**
Problem	When PROCHOT# is activated during BIOS initialization, the processor may hang with a machine check error reported in IA32_MCi_STATUS, with MCACOD (bits [15:0]) value of 0402H, and MSCOD (bits [31:16]) value of 0409H.
Implication	Due to this erratum, the processor may hang.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL021	**Processor May Hang if Warm Reset Triggers During BIOS Initialization**
Problem	Under complex micro-architectural conditions, when the processor receives a warm reset during BIOS initialization, the processor may hang with a machine check error reported in IA32_MCi_STATUS, with MCACOD (bits [15:0]) value of 0400H, and MSCOD (bits [31:16]) value of 0080H.
Implication	Due to this erratum, the processor may hang. Intel has only observed this erratum in a synthetic test environment.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL022	**PCIe Link_Down May Occur After Exiting From Package C10 Cycle**
Problem	After a Package C10 Exit event, the processor's PCIe link may fail to retrain.
Implication	When this erratum occurs, the PCIe link enters the Link Down state, which may lead to a system failure.
Workaround	It is possible for BIOS to include a workaround for this errata.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL023	**Reported Package Power May Not be Accurate**
Problem	MSR_PKG_ENERGY_STATUS (611H) bits[31:0] may not accurately reflect package power.
Implication	Due to this erratum, a higher than expected variation in the reported package power may be observed.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL024	USB TD65 Polling LFPS Duration Test Fail on Direct Port
Problem	The USB3 TD6.5 Compliance Polling LFPS Duration Test fails, because of Electrical Low Frequency Periodic Signalling (LFPS) common mode adjustment.
Implication	Due to this erratum, this compliance test will fail. Intel has not observed a compliance test failure on ports with a platform-level retimer. Intel has not observed any functional failures due to this erratum.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL025	Cache Configuration May be Incorrectly Initialized During Boot
Problem	The processor may fail to properly initialize internal cache configuration registers during boot.
Implication	Due to this erratum, the system may intermittently hang or exhibit unpredictable system behavior.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

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Specification Changes

ID	Affected Products/ Steps	Specification Change Title	Issue	Previous Text Reference	New Text	Affected Document
001	UP3 B1	HDCP 2.2 not supported in certain modes for DP1.4a interface.	While using DP1.4a output ports in MST (Multi transport mode) and Forward Error Correction (FEC) and utilizing HDCP2.2 for protected content, bitstream corruption can occur.	The processor supports both HDCP 2.3 and 1.4 content protection over wired displays (HDMI* and DisplayPort*).	The processor supports both HDCP 2.3 and 1.4 content protection over wired displays (HDMI* and DisplayPort*). HDCP 1.4 will be supported for DisplayPort wired displays while operated in multistream transports and FEC is enabled.	631121

Note: There are no Specification Clarifications or Document Changes for this revision of the specification update.

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