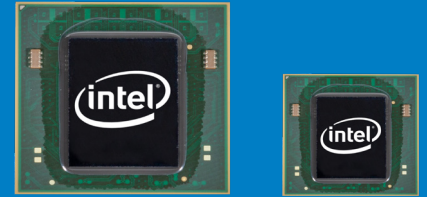


# Intel® Ethernet Controller X550



## Integrated single chip 10GBASE-T controller simplifies 10 Gigabit Ethernet (GbE) designs

### Key Features

- Single and dual-port 10GBASE-T controller with integrated MAC and PHY
  - 10GBASE-T, 1000BASE-T and 100BASE-TX modes
  - Supports NBASE-T technology (2.5 and 5.0GbE over CAT5e)
- IEEE 802.3az Energy Efficient Ethernet (EEE)<sup>1</sup>
- PCI Express (PCIe) 3.0 with up to 8.0 GT/s
- Network virtualization stateless offload: VxLAN and NVGRE.
- Intel® Ethernet Flow Director for hardware-based application traffic steering

### Overview

Intel continues its legacy of Ethernet leadership by introducing the next generation 10 Gb/s family of silicon to support the growing 10GBASE-T ecosystem.

The Intel® Ethernet Controller X550 family is the low cost single-chip 10GBASE-T controller of choice to broadly deploy 10GbE in platform designs. 10GBASE-T is the most flexible connectivity for all of your networking requirements.

Innovation continues with Intel's second generation integrated 10GBASE-T MAC+PHY, which drives down both cost and power, enabling the most cost-effective deployment of 10GbE in the data center. With 10GBASE-T, migration to 10GbE is dramatically simplified with backward compatibility with existing GbE network infrastructure.

## 10GBASE-T simplifies the transition from 1GbE to 10GbE

The X550 controller provides up to two integrated 10GBASE-T PHYs providing 10Gb/s of throughput that are also backwards compatible with legacy GbE switches and CAT6A cabling. Autonegotiation between 100Mb/s, 1GbE, and 10GbE speeds provide the backwards compatibility for a smooth transition and easy migration to 10GbE.

In addition, the X550 controller also supports NBASE-T technology. NBASE-T technology can increase network speeds of 2.5Gb/s or 5Gb/s using existing CAT5e/CAT6 cables at lengths up to 100 m.

Intel's NBASE-T firmware can be upgraded to support the IEEE 802.3bz specification<sup>1</sup>.

### Best Choice for Server Virtualization

Virtualization changes server resource deployment and management by running multiple applications and operating systems on a single physical server.

With Intel® Virtualization Technology for connectivity (VT-c), the X550 delivers outstanding I/O performance and Quality of Service (QoS) in virtualized data centers and cloud environments. I/O virtualization advances network connectivity used in today's servers to more efficient models. Flexible Port Partitioning (FPP), multiple Tx/Rx queues, Tx queue rate limiting, and on-controller QoS functionality, are useful for both virtual and non-virtual server deployments.

The X550 reduces I/O bottlenecks by providing intelligent offload of networking traffic per VM, enabling near-native performance and VM scalability. The host-based virtualization technologies include:

- VMDq for emulated path: NIC-based VM queue sorting enabling efficient hypervisor-based switching.
- SR-IOV for direct assignment: NIC-based isolation and switching for various virtual station instances enabling optimal CPU usage in virtualized environment.

### Network Virtualization

Network virtualization is the next big trend in creating an agile data center.

- VxLAN and NVGRE offloads: These stateless offloads preserve application performance for overlay networks. With these offloads, it is possible to distribute network traffic across CPU core.
- Preserves application performance in network virtualized environment.

## Flexible Port Partitioning (FPP)

FPP enables virtual Ethernet controllers that to used by a Linux host directly and/or assigned directly to virtual machines for hypervisor virtual switch bypass. FPP enables the assignment of up to 64 Linux host processes or virtual machines per port to virtual functions. An administrator can use FPP to control the partitioning of the bandwidth across multiple virtual functions. FPP can also provide balanced QoS by giving each assigned virtual function equal access to 10Gb/s of bandwidth.

### 10GbE performance at low cost and low power

10GBASE-T is a cost effective way to bring 10GbE to embedded, workstation, and server platforms, as LAN on Motherboard (LOM) or network add-in card. To reduce cost and power, the X550 controller is manufactured using a 28 nm process with an integrated MAC controller and up to two 10GBASE-T PHYs in a single-chip solution. Integration translates to lower power with reduced per-port power consumption, which can eliminate the need for active fan heatsinks.

The X550 controller provides bandwidth-intensive applications and virtualized data centers 10GbE network performance with cost effective network connectivity.

### Network manageability interfaces

The X550 controller provides OS2BMC, SMBus and DMTF-defined Network Controller Sideband Interface (NC-SI) for BMC manageability. In addition, it introduces support for Management Component Transport Protocol (MCTP), a new DMTF standard, enabling a BMC to gather information about Intel Ethernet Converged Network Adapters that can include the data rate, link speed, and error counts.

With low-power consumption, a small footprint and integrated serial PHYs, the controller is ideally suited for server blades, LOM, NIC, and mezzanine card implementations. The X550 also incorporates the manageability required by IT personnel for remote control and alerting. Communication to the Baseboard Management Controller (BMC) is available either through an onboard SMBus port or the DMTF-defined Network Controller Sideband Interface (NC-SI), providing a variety of management protocols, including IPMI, BMC passthrough, OS2BMC, and MCTP.

### Firmware Authentication

The X550 implements a signed firmware authenticated capability to verify the firmware and critical device settings with built-in detection of corruption. This is done at the time of firmware updates.

Features	Description
<b>External Interfaces</b>	
Intel® Ethernet Controller X550-AT Intel® Ethernet Controller X550-AT2 Intel® Ethernet Controller X550-BT2	<ul style="list-style-type: none"> <li>• PCIe interface 3.0 – 8.0GT/s, 5.0GT/s and 2.5GT/s; support for x1 and x4, links widths (lanes)</li> <li>• PCIe interface 3.0 – 8.0GT/s, 5.0GT/s and 2.5GT/s; support for x1 and x4, links widths (lanes)</li> <li>• PCIe interface 2.1 – 5.0GT/s and 2.5GT/s; support for x1, x4 and x8 links widths (lanes)</li> </ul>
Network Interfaces	<ul style="list-style-type: none"> <li>• IEEE 802.3 Ethernet interface for 10GBASE-T, 1000BASE-T, 100BASE-TX (IEEE 802.3an, 802.3ab, 802.3u)</li> <li>• NBASE-T technology support for 2.5GbE and 5.0GbE (pre-IEEE 802.3bz)</li> </ul>
<b>BOM Cost Reduction</b>	
Single Chip Design	<ul style="list-style-type: none"> <li>• Designed for passive heatsink thermal solutions</li> <li>• X550-AT and X550-AT2: Small packaging for easier board layout and design</li> <li>• X550-BT2: Footprint compatible with the Intel® Ethernet Controller X540 family</li> </ul>
Integrated Copper 10GBASE-T PHYs	<ul style="list-style-type: none"> <li>• Single chip with integrated PHYs for lower power and simplified component placement</li> </ul>
<b>External Features</b>	
NBASE-T technology support (IEEE 802.3bzready)	<ul style="list-style-type: none"> <li>• Provides 2.5GbE and 5.0GbE link speeds over CAT5e/CAT6 cabling deployments. Firmware upgradable to IEEE 802.3bz<sup>1</sup></li> </ul>
IEEE 1588 Protocol and IEEE 802.1AS Implementation	<ul style="list-style-type: none"> <li>• Per-packet timestamping and synchronization of time-sensitive applications</li> <li>• Distribute common time to media devices</li> </ul>
VLAN Support: • IEEE 801.1Q (VLAN) • IEEE 802.1ad (Double VLAN)	<ul style="list-style-type: none"> <li>• Provide data separation and security between network traffic</li> <li>• Double-tagging can be useful for Internet service providers, allowing the use of VLANs internally while mixing traffic from clients that are already VLAN-tagged</li> </ul>
Automatic Cross-over Detection Function (MDI/MDI-X)	<ul style="list-style-type: none"> <li>• The PHY automatically detects which Media-Dependent Interface (MDI) is required and configures itself accordingly</li> </ul>
<b>I/O Features for Multi-core Processor Systems</b>	
Intel® Flow Director	<ul style="list-style-type: none"> <li>• An advanced traffic steering capability that increases the number of transactions per second and reduces latency for cloud applications like Memcached</li> </ul>
MSI-X support	<ul style="list-style-type: none"> <li>• Minimizes overhead of interrupts</li> <li>• Load-balancing of interrupt handling between multiple cores/CPU's</li> <li>• Dynamic allocation of up to 64 vectors per port</li> </ul>
Multiple queues: 128 Tx and Rx Per Port	<ul style="list-style-type: none"> <li>• Queues provide QoS for virtualization, DCB, RSS, L2 EtherType, FCoE redirections, L3/L4/5-tuple filters, flow director, and TCP SYN filters</li> <li>• Network packet handling without waiting for buffer overflow providing efficient packet prioritizations</li> </ul>
TCP/UDP, IPv4 checksum offloads (Rx/Tx/largesend); extended Tx descriptors for more offload capabilities	<ul style="list-style-type: none"> <li>• Improve CPU usage</li> <li>• Checksum and segmentation capability to new standard packet type</li> </ul>
RSS for Windows environment scalable I/O for Linux environments (IPv4, IPv6, TCP/UDP)	<ul style="list-style-type: none"> <li>• Up to 32 flows per port</li> <li>• Improves the system performance related to handling of network data on multi-processor systems</li> </ul>
IPv6 support for IP/TCP and IP/UDP receive checksum offload	<ul style="list-style-type: none"> <li>• Improved CPU usage</li> </ul>
Tx TCP segmentation offload (TSO-IPv4, IPv6)	<ul style="list-style-type: none"> <li>• Large TCP I/O is segmented into small packets to increase throughput and reduce CPU overhead</li> <li>• Compatible with large-send offload</li> </ul>
Large FC Receive	<ul style="list-style-type: none"> <li>• Large FC receive includes two types of offloads that can save a data copy by posting the received FC payload directly to the kernel storage cache or the user application space</li> </ul>
Support for Packets Up To 15.5 KB (Jumbo Frames)	<ul style="list-style-type: none"> <li>• Enables higher and better throughput of data</li> </ul>
DMA Coalescing	<ul style="list-style-type: none"> <li>• Reduces platform power consumption by coalescing, aligning, and synchronizing DMA</li> <li>• Enables synchronizing power activity and power management of memory, CPU and RC internal circuitry</li> </ul>
Flow Director Filters: • Up to 32 KB - Two Signature Filters • Up to 8 KB - Two Perfect-match Filters	<ul style="list-style-type: none"> <li>• The flow director filters identify specific flows, or sets of flows, and route them to specific queues</li> <li>• These filters are an expansion of the L3/L4 5-tuple filters that provide up to 32 KB additional filters</li> </ul>
Receive Side Coalescing (RSC)	<ul style="list-style-type: none"> <li>• Merge multiple received frames from the same TCP/IP connection into a single structure</li> </ul>

Features	Description
<b>Virtualization Features</b>	
Multi-mode I/O Virtualization Operations	<ul style="list-style-type: none"> <li>Supports two modes of operation of virtualized environments: <ul style="list-style-type: none"> <li>Direct assignment of part of the port resources to different guest operating systems using the PCI SIG SR-IOV standard (also known as native mode or pass-through mode)</li> <li>Central management of the networking resources by hypervisor (also known as software switch acceleration mode)</li> </ul> </li> <li>A hybrid model, where some of the VMs are assigned a dedicated share of the port and the rest are serviced by a hypervisor is also supported</li> </ul>
VxLAN	<ul style="list-style-type: none"> <li>A framework for overlaying virtualized layer 2 networks over layer 3 networks. VxLAN enables users to create a logical network for your virtual machines across different networks</li> </ul>
NVGRE	<ul style="list-style-type: none"> <li>Network Virtualization using Generic Routing Encapsulation. The encapsulation of an Ethernet Layer 2 Frame in IP that enables the creation of virtualized Layer 2 subnets that can span physical Layer 3 IP networks</li> </ul>
Virtual Machine Device Queues (VMDq)	<ul style="list-style-type: none"> <li>Offloads data sorting from the hypervisor to silicon, improving data throughput and CPU usage</li> <li>QoS feature for Tx data by providing round-robin servicing and preventing head-of-line blocking</li> <li>Sorting based on MAC addresses and VLAN tags</li> </ul>
Next Generation VMDq	<ul style="list-style-type: none"> <li>Enhanced QoS feature by providing weighted round-robin servicing for the Tx data</li> <li>Provides loopback functionality; data transfers between the virtual machines within the same physical server do not go out to the wire and back in, improving throughput and CPU usage</li> <li>Supports replication of multicast and broadcast data</li> </ul>
64 Transmit (Tx) and Receive (Rx) Queue Pairs Per Port	<ul style="list-style-type: none"> <li>Supports VMware NetQueue and Microsoft VMQ</li> <li>MAC/VLAN filtering for pool selection and either DCB or RSS for the queue in pool selection</li> </ul>
Flexible Port Partitioning: 64 Virtual Functions Per Port	<ul style="list-style-type: none"> <li>Virtual Functions (VFs) appear as Ethernet Controllers in Linux Oses that can be assigned to VMs, Kernel processes or teamed using the Linux Bonding Drivers</li> </ul>
Support for PCI-SIG SR-IOV Specification	<ul style="list-style-type: none"> <li>Up to 64 virtual functions per port</li> </ul>
IEEE 802.1Q Virtual Local Area Network (VLAN) Support with VLAN Tag Insertion, Stripping and Packet Filtering for up to 4096 VLAN tags	<ul style="list-style-type: none"> <li>Ability to create multiple VLAN segments</li> <li>Filtering packets belonging to certain VLANs</li> </ul>
<b>Remote Boot Options</b>	
Preboot Execution Environment (PXE) Flash Interface Support	<ul style="list-style-type: none"> <li>Enables system boot via the EFI (32-bit and 64-bit)</li> <li>Flash interface for PXE 2.1 option ROM</li> </ul>
Intel Boot Agent software: Linux boot via PXE or BOOTP, Windows Deployment Services, or UEFI	<ul style="list-style-type: none"> <li>Allows networked computer to boot using a program code image supplied by a remote server</li> <li>Complies with the Preboot Execution Environment (PXE) Version 2.1 Specification</li> </ul>
<b>Security and Power Management</b>	
Receive packet filtering	<ul style="list-style-type: none"> <li>Determines which incoming packets are allowed to pass to the local machine based on L2, VLAN, or management policies</li> </ul>
Integrated IPsec security engines for offloads of up to 1024 Security Associations (SA) for each Tx and Rx	<ul style="list-style-type: none"> <li>Offloads handle a certain amount of the total number of IPsec flows on the controller in hardware</li> </ul>
IEEE 802.3az Energy Efficient Ethernet (EEE) <sup>1</sup>	<ul style="list-style-type: none"> <li>Power consumption by the PHY is reduced by during period of low link utilization to help reduce power consumption</li> </ul>
Secure flexible firmware architecture	<ul style="list-style-type: none"> <li>Secure NVM Update that protects the flash from external unauthorized software programming</li> <li>Supports dynamic firmware updating that enables firmware updates without the need for a system reboot</li> </ul>
Four Software Definable Pins (SDP) per port	<ul style="list-style-type: none"> <li>SDP pins per port can be used for miscellaneous hardware or software-controlled purposes</li> </ul>
LAN disable function	<ul style="list-style-type: none"> <li>Disabling just the PCIe function but keeping the LAN port that resides on it fully active for manageability purposes and BMC pass-through traffic</li> </ul>
Anti-spoofing for MAC and VLANs	<ul style="list-style-type: none"> <li>VM always uses a source Ethernet VLAN or MAC address on the transmit path that is part of the set of VLAN tags and Ethernet MAC addresses defined on the Rx path</li> </ul>
Full wake up support: <ul style="list-style-type: none"> <li>Advanced Power Management (APM) Support (Formerly Wake on LAN)</li> <li>Advanced Configuration and Power Interface (ACPI) Specification v2.0c</li> <li>Magic Packet Wake-up Enable with Unique MAC Address</li> </ul>	<ul style="list-style-type: none"> <li>APM - Designed to receive a broadcast or unicast packet with an explicit data pattern (Magic Packet) and assert a signal to wake up the system</li> <li>APCI - PCIe power management-based wake up that can generate system wake-up events from a number of sources</li> </ul>
Low power operation and power management	<ul style="list-style-type: none"> <li>Incorporates numerous features to maintain the lowest power possible including PCI Express Link and Network Interface power management</li> </ul>
Low power link up - link speed control	<ul style="list-style-type: none"> <li>Enables a link to come up at the lowest possible speed in cases where power is more important than performance</li> </ul>

Features	Description
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### Mechanical and Thermal

Intel® Ethernet Controller X550-AT	• 17 mm x 17 mm Flip-chip ball grid array (FC-BGA) package
Intel® Ethernet Controller X550-AT2	• 17 mm x 17 mm FC-BGA package
Intel® Ethernet Controller X550-BT2	• 25 mm x 25 mm FC-BGA package

Power:	
• X550-AT	• 9 W max, 7 W typical (10Gb/s active)
• X550-AT2	• 11 W max, 9 W typical (2 x 10Gb/s active)
• X550-BT2	• 11 W max, 9 W typical (2 x 10Gb/s active)

### Manageability Features

DMTF Network Controller Sideband Interface (NC-SI) pass-through	• Supports pass-through traffic between BMC and controller's LAN functions
Intel® System Management Bus (SMBus) Passthrough	• Enables BMC to configure the controller's filters and management related capabilities
Management Component Transport Protocol (MCTP) over SMBus or PCIe	• BMC communication between add-in devices within the platform • Allow reporting and controlling of all the information exposed in a LOM device via NC-SI, in NIC devices via MCTP over SMBus or PCIe
OS2MBC Traffic Support: <ul style="list-style-type: none"> <li>• Host-based application-to-BMC network communication patch</li> <li>• Private OS2MBC traffic flow</li> </ul>	• Transmission and reception of traffic internally to communicate between the OS and local BMC • Filtering method that enables server management software to communicate with a management controller via standard networking protocols such as TCP/IP instead of a chipset-specific interface • BMC might have its own private connection to the network controller and network flows are blocked
DMTF MCTP Protocol Over SMBus	• Enables reporting and controlling information via NC-SI using the MCTP protocol over SMBus
Firmware-based thermal management	• Can be programmed via the BMC to initiate thermal actions and report thermal occurrences
IEEE 802.3 Management Data Input/Output Interface (MDIO Interface or MII Management Interface)	• Enables the MAC and software to monitor and control the state of the PHY
MAC/PHY control status	• Enhanced control capabilities through PHY reset, link status, duplex indication, and MAC Dx power state
Watchdog timer	• The MAC and each PHY support a watchdog timer to detect a stuck microcontroller
Advanced Error Reporting (AER)	• Messaging support to communicate multiple types/severity of errors
Controller memory integrity protection	• Main internal memories are protected by Error Correcting Code (ECC) or parity bits
Vital Product Data (VPD) support	• Support for VPD memory area
Flexible MAC address	• MAC address used by a port can be replaced with a temporary MAC address in a way that is transparent to the software layer

### Product Order Code

Configuration	Ports	Package	Product Code	MM#	Product S Spec	Media Type
Intel® Ethernet Controller X550-AT	1	17 x 17 mm	ELX550AT	945964	S LLFT	Tray
Intel® Ethernet Controller X550-AT	1	17 x 17 mm	ELX550AT	945983	S LLFU	Tape & Reel
Intel® Ethernet Controller X550-AT2	2	17 x 17 mm	ELX550AT2	943736	S LL2E	Tray
Intel® Ethernet Controller X550-AT2	2	17 x 17 mm	ELX550AT2	943743	S LL2F	Tape & Reel
Intel® Ethernet Controller X550-BT2	2	25 x 25 mm	ELX550BT2	943742	S LL2G	Tray
Intel® Ethernet Controller X550-BT2	2	25 x 25 mm	ELX550BT2	943744	S LL2H	Tape & Reel

### Intel® Ethernet Accessories

Intel® Ethernet Optics and Cables are proven, reliable solutions for high-density Ethernet connections. Combine these accessories with Intel® Ethernet 700 Series and 500 Series Network Adapters for dependable interoperability and consistent performance across the network. Learn more at [intel.com/ethernet](http://intel.com/ethernet)

### Supported Operating Systems

The Feature Support Matrix for Intel® Ethernet Controllers includes a complete list of [supported network operating systems](#).

## Warranty

Standard Intel limited warranty, one year. See Intel terms and conditions of sale for more details.

## Product Information

For information about Intel® Ethernet Products and technologies, visit: [intel.com/ethernetproducts](https://www.intel.com/ethernetproducts)

## Customer Support

For customer support options in North America visit:  
[intel.com/content/www/us/en/support/contact-support.html](https://www.intel.com/content/www/us/en/support/contact-support.html)

1. Feature to be enabled in a post-launch firmware release.

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