



3rd Gen Intel[®] Xeon[®] Scalable Processors, Codename Ice Lake

Specification Update

August 2021



Intel technologies' features and benefits depend on system configuration and may require enabled hardware, software or service activation. Learn more at Intel.com, or from the OEM or retailer.

No computer system can be absolutely secure. Intel does not assume any liability for lost or stolen data or systems or any damages resulting from such losses.

You may not use or facilitate the use of this document in connection with any infringement or other legal analysis concerning Intel products described herein. You agree to grant Intel a non-exclusive, royalty-free license to any patent claim thereafter drafted which includes subject matter disclosed herein.

No license (express or implied, by estoppel or otherwise) to any intellectual property rights is granted by this document.

The products described may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Intel disclaims all express and implied warranties, including without limitation, the implied warranties of merchantability, fitness for a particular purpose, and non-infringement, as well as any warranty arising from course of performance, course of dealing, or usage in trade.

Tests document performance of components on a particular test, in specific systems. Differences in hardware, software, or configuration will affect actual performance. Consult other sources of information to evaluate performance as you consider your purchase. For more complete information about performance and benchmark results, visit <http://www.intel.com/performance>.

Cost reduction scenarios described are intended as examples of how a given Intel- based product, in the specified circumstances and configurations, may affect future costs and provide cost savings. Circumstances will vary. Intel does not guarantee any costs or cost reduction.

Results have been estimated or simulated using internal Intel analysis or architecture simulation or modeling, and provided to you for informational purposes. Any differences in your system hardware, software or configuration may affect your actual performance.

Performance varies by use, configuration and other factors. Learn more at www.intel.com/PerformanceIndex.

See backup for workloads and configurations. Results may vary.

For workloads and configurations visit www.intel.com/PerformanceIndex. Results may vary.

Intel does not control or audit third-party benchmark data or the web sites referenced in this document. You should visit the referenced web site and confirm whether referenced data are accurate.

Copies of documents which have an order number and are referenced in this document may be obtained by calling 1-800-548-4725 or by visiting www.intel.com/design/literature.htm.

Intel, the Intel logo and Xeon are trademarks of Intel Corporation or its subsidiaries.

*Other names and brands may be claimed as the property of others.

Copyright © 2021, Intel Corporation. All Rights Reserved.

Contents

Revision History	4
Preface	5
Identification Information	7
Component Marking Information	8
Summary Tables of Changes	9
Errata Summary Table	10
Errata Details	15
Specification Changes	35
Specification Clarifications	36
Documentation Changes	37



Revision History

Date	Revision	Description
August 2021	004	Added errata ICX82 , through ICX88 .
July 2021	003	Added errata ICX74 , through ICX81 . Updated ICX39 , and ICX58 .
June 2021	002	Added errata ICX47 , through ICX73 .
April 2021	001	Initial Release

Preface

This document is an update to the specifications contained in the [Related Documents](#) table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in [Nomenclature](#) are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Related Documents

Document Title	Document Number/ Location
<i>Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 1: Basic Architecture</i>	253665 ¹
<i>Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2A: Instruction Set Reference, A-M</i>	253666 ¹
<i>Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2B: Instruction Set Reference, N-Z</i>	253667 ¹
<i>Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3A: System Programming Guide, Part 1</i>	253668 ¹
<i>Intel® 64 and IA-32 Architectures Software Developer's Manual Volume 3B: System Programming Guide, Part 2</i>	253669 ¹
<i>ACPI Specifications</i>	www.acpi.info ²

1. Documents are available publicly at <https://www.intel.com/content/www/us/en/design/resource-design-center.html>.
2. Document available at www.uefi.org.



Nomenclature

Errata are design defects or errors. These may cause the 3rd Gen Intel® Xeon® Scalable Processors' behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

QDF Number A several digit code used to distinguish between engineering samples. These processors are used for qualification and early design validation. The functionality of these parts can range from mechanical only to fully functional. The NDA specification update has a processor identification information table that lists these QDF numbers and the corresponding product sample details.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Identification Information

Component Identification via Programming Interface

The 3rd Gen Intel® Xeon® Scalable Processors stepping can be identified by the following register contents:

Reserved	Extended Family ¹	Extended Model ²	Reserved	Processor Type ³	Family Code ⁴	Model Number ⁵	Stepping ID ⁶
31:28	27:20	19:16	15:13	12:12	11:8	7:4	3:0
	0000000b			0b			Varies per stepping

Note:

- The Extended Family, bits [27:20] are used in conjunction with the Family Code, specified in bits [11:8], to indicate whether the processor belongs to the Intel386™, Intel486™, Pentium®, Pentium® Pro, Pentium® 4, Intel® Core™ processor families, Intel® Core™ ix processor families, and Intel® Xeon® processor families.
- The Extended Model, bits [19:16] in conjunction with the Model Number, specified in bits [7:4], are used to identify the model of the processor within the processor's family.
- The Processor Type, specified in bit [12] indicates whether the processor is an original OEM processor, an Intel OverDrive processor, or a dual processor (capable of being used in a dual processor system).
- The Family Code corresponds to bits [11:8] of the EDX register after RESET, bits [11:8] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the generation field of the Device ID register accessible through Boundary Scan.
- The Model Number corresponds to bits [7:4] of the EDX register after RESET, bits [7:4] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the model field of the Device ID register accessible through Boundary Scan.
- The Stepping ID in bits [3:0] indicates the revision number of that model. See [Table 1](#) for the processor stepping ID number in the CPUID information.

When the EAX is set to a value of '1', the CPUID instruction returns the extended family, extended model, processor type, family code, model number, and stepping ID together referred to as the processor signature value in the EAX register. Note that after reset, the process will report the process signature value in both the EDX and EAX registers.

Cache and TLB descriptor parameters are provided in the EAX, EBX, ECX, and EDX registers after the CPUID instruction is executed with a 2 in the EAX register.

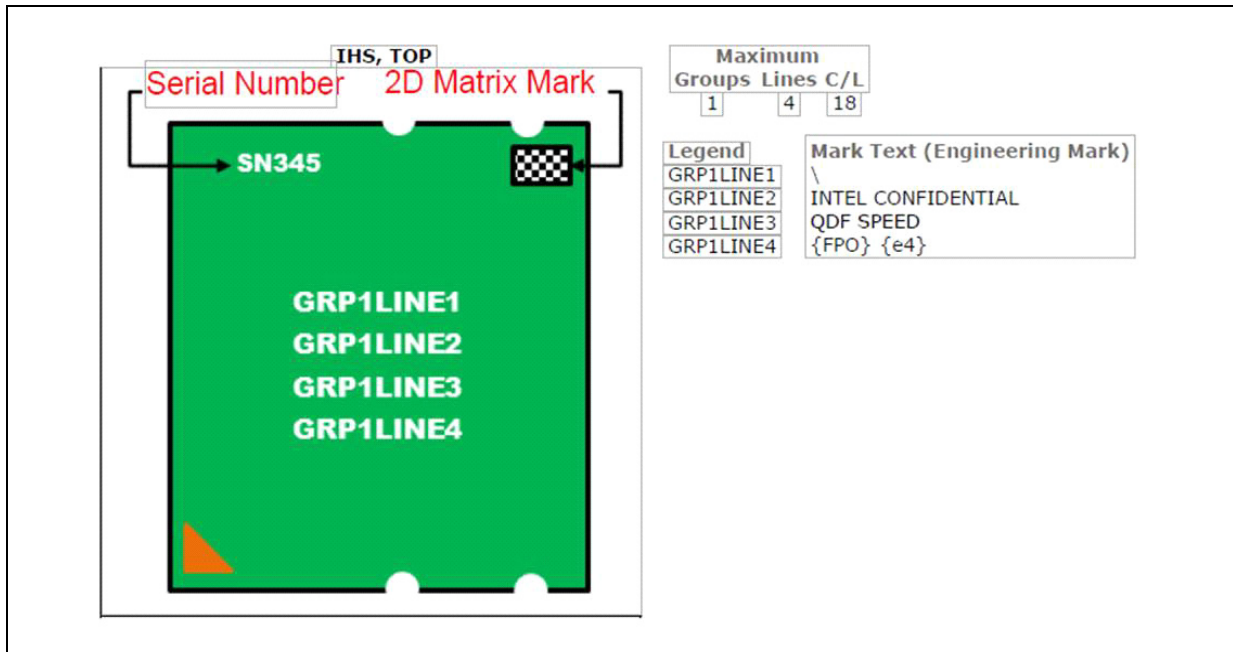
Table 1. Component Identification via Registers

Physical Chip	Stepping	Segment Wayness	CPUID	CAPID0(Segment)			CAPID0(Wayness)		CAPID4(Chop)		
				B:31, D:30, F:3, O:84h						B:31, D:30, F:3, O:94H	
				5	4	3	1	0	7	6	
XCC	D-2	Server, 1S	606A6	1	1	1	0	1	1	1	
	D-2	Server, 2S	606A6	1	1	1	1	0	1	1	
HCC	M-1	Server, 1S	606A6	1	1	1	0	1	1	0	
	M-1	Server, 2S	606A6	1	1	1	1	0	1	0	

Component Marking Information

The 3rd Gen Intel® Xeon® Scalable Processors can be identified by the following register markings.

Figure 1. Processor Preliminary Top Side Marking (Example)



For 3rd Gen Intel® Xeon® Scalable Processors SKUs, see <https://ark.intel.com/content/www/us/en/ark/products/series/204098/3rd-generation-intel-xeon-scalable-processors.html>.

Summary Tables of Changes

The following tables indicate the Specification Changes, Errata, Specification Clarifications, or Documentation Changes which apply to the 3rd Gen Intel® Xeon® Scalable Processors product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. These tables use the following notations:

Codes Used in Summary Tables

Stepping	Description
(No mark) or (Blank box)	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Status	Description
Doc	Document change or update will be implemented
Planned Fix	This erratum may be fixed in a future stepping of the product
Fixed	This erratum has been previously fixed in Intel® hardware, firmware or software
No Fix	There are no plan to fix this erratum



Errata Summary Table

Erratum ID	Processor Line / Steppings		Title
	HCC	XCC	
	M-1	D-2	
ICX1.	No Fix	No Fix	Memory Errors in a VLS Region on a Certain Device May Not be Properly Corrected
ICX2.	No Fix	No Fix	Wrong Page Access Semantics May be Reported When Intel® SGX ENCLU[EMODPE] Instruction Generates Page Fault (#PF) Exception
ICX3.	No Fix	No Fix	Writing Non-Zero Values to Read Only Fields in IA32_THERM_STATUS MSR May #GP
ICX4.	No Fix	No Fix	VMREAD/VMWRITE Instructions May Not Fail When Accessing an Unsupported Field in VMCS
ICX5.	No Fix	No Fix	VERR Instruction Inside VM-Entry May Cause DR6 to Contain Incorrect Values
ICX6.	No Fix	No Fix	Vector Masked Store Instructions May Cause Write Back of Cache Line Where Bytes Are Masked
ICX7.	No Fix	No Fix	VCVTPS2PH To Memory May Update MXCSR in The Case of a Fault on The Store
ICX8.	No Fix	No Fix	SMRAM State-Save Area Above the 4 GB Boundary May Cause Unpredictable System Behavior
ICX9.	No Fix	No Fix	Single Correctable Error Can be Logged Twice if Patrol Scrub Reads Address When Read Transaction is in Flight to Same Address
ICX10.	No Fix	No Fix	Processor May Hang if Warm Reset Triggers During BIOS Initialization
ICX11.	No Fix	No Fix	Placing Posted-Interrupt Descriptors Within The PRMRR May Result in a Processor Hang
ICX12.	No Fix	No Fix	Placing Page Table Information in The APIC-Access Page May Lead to Unexpected Page Faults While Performing Enclave Accesses
ICX13.	No Fix	No Fix	Performance Monitoring Load Latency Events May be Inaccurate For Gather Instructions
ICX14.	No Fix	No Fix	Performance Monitoring Counters May Undercount When Using CPL Filtering
ICX15.	No Fix	No Fix	PEBS Eventing IP Field May be Incorrect After Not-Taken Branch
ICX16.	No Fix	No Fix	Overlap Between APIC And SMRR2 Memory-Mapped Registers Will Not Signal a #GP
ICX17.	No Fix	No Fix	Overflow Flag in IA32_MC0_STATUS MSR May be Incorrectly Set
ICX18.	No Fix	No Fix	Intel SGX Enclave Accesses to The APIC-Access Page May Cause APIC-Access VM Exits
ICX19.	No Fix	No Fix	Intel® PT TIP or FUP Packets May be Dropped Without OVF Packet
ICX20.	No Fix	No Fix	Intel PT CBR Packet May be Delayed or Dropped

Errata Summary Table

Erratum ID	Processor Line / Steppings		Title
	HCC	XCC	
	M-1	D-2	
ICX21.	No Fix	No Fix	Incorrect FROM_IP Value For an RTM Abort in BTM or BTS May be Observed
ICX22.	No Fix	No Fix	Incorrect Branch Predicted Bit in BTS/BTM Branch Records
ICX23.	No Fix	No Fix	In eMCA2 Mode, When The Retirement Watchdog Timeout Occurs CATERR# May be Asserted
ICX24.	No Fix	No Fix	IA32_RTIT_STATUS.FilterEn Bit Might Reflect a Previous Value
ICX25.	No Fix	No Fix	IA32_MC1_STATUS MSR May Not Log Errors When IA32_MC1_CTL MSR is Set to Not Signal Errors
ICX26.	No Fix	No Fix	False MC1 Error Reported in The Shadow of a Internal Timer Error
ICX27.	No Fix	No Fix	Debug Exceptions May Be Lost or Misreported When MOV SS or POP SS Instruction is Not Followed by a Write to SP
ICX28.	No Fix	No Fix	CPUID TLB Information is Inaccurate
ICX29.	No Fix	No Fix	CPUID L2 Cache Information May be Inaccurate
ICX30.	No Fix	No Fix	Configuring The PRMR as Non-WB Might Lead to Incorrect VM-Exit Interruption Error Code
ICX31.	No Fix	No Fix	An Invalid Algorithm in The CRYPTO_ALG Field of The MKTME_KEY_PROGRAM_STRUCT Will Not Cause an INVALID_ENC_ALG Failure as Expected
ICX32.	No Fix	No Fix	A Spurious APIC Timer Interrupt May Occur After Timed MWAIT
ICX33.	No Fix	No Fix	#GP on Segment Selector Descriptor That Straddles Canonical Boundary May Not Provide Correct Exception Error Code
ICX34.	No Fix	No Fix	x87 FPU Exception (#MF) May be Signaled Earlier Than Expected
ICX35.	No Fix	No Fix	IERR Not Logged Correctly When Ubox Requested to Signal MSMI
ICX36.	No Fix	No Fix	PCIe* Surprise Link Down Events May Not be Reported
ICX37.	No Fix	No Fix	PCIe RPIO May Contain Incorrect Tag Value
ICX38.	No Fix	No Fix	Uncore MC Bank Registers Corrected Error Count Field May Not Have a Sticky Most Significant Bit
ICX39.	Fixed	Fixed	UPI Correctable Error May be Observed After Cold Resets And TCRH Events
ICX40.	No Fix	No Fix	Poisoned Locked Bus Transactions May Not Allow Warm Reset to Correctly Reset The Processor



Errata Summary Table

Erratum ID	Processor Line / Steppings		Title
	HCC	XCC	
	M-1	D-2	
ICX41.	Fixed	Fixed	TOR Timeout During WBINVD May Cause System Hang
ICX42.	No Fix	No Fix	Intel® PT VMEntry Indication Depends on The Incorrect VMCS Control Field
ICX43.	No Fix	No Fix	Intel PT Trace May Drop Second Byte of CYC Packet
ICX44.	No Fix	No Fix	Intel PT TIP.PGD May Not Have Target IP Payload
ICX45.	No Fix	No Fix	Intel PT PSB+ May be Lost
ICX46.	No Fix	No Fix	Intel Processor Trace PSB+ Packets May Contain Unexpected Packets
ICX47.	No Fix	No Fix	Spurious PCIe Link Parity Errors May be Logged
ICX48.	No Fix	No Fix	IBIST Receiver Error Overflow Register Field Cannot be Cleared by Software
ICX49.	No Fix	No Fix	MBM May Report Incorrect Bandwidth For Certain Access Strides
ICX50.	No Fix	No Fix	Correctable Errors May Set The Overflow Bit
ICX51.	No Fix	No Fix	Enabled Error May Not be Logged When Other Errors Are Disabled
ICX52.	No Fix	No Fix	Uncore MC Bank Registers Corrected Error Count Field May Not Have a Sticky Most Significant Bit
ICX53.	No Fix	No Fix	Machine Check Bank Status MSR May Not Set Overflow Bit When Multiple Uncorrectable Errors Occur
ICX54.	No Fix	No Fix	FERR Registers Are Not Getting Cleared When CHANERR Register is Being Cleared
ICX55.	No Fix	No Fix	IOMMU Translation Requests to Interrupt Range May Fail
ICX56.	No Fix	No Fix	Internal Firmware Errors May Not Set Error Enable Bit
ICX57.	No Fix	No Fix	UPI PH_PLS.SRstRcvdP Value May be Incorrect Following a UPI PHY Reset
ICX58.	No Fix	No Fix	Spurious Write Data Parity Errors May be Logged
ICX59.	Fixed	Fixed	PKG_MIN_PWR May be Incorrect
ICX60.	No Fix	No Fix	PN_POWER_OF_SKU May be Incorrect
ICX61.	No Fix	No Fix	PCIe Surprise Link Down Logging May be Unexpectedly Blocked

Errata Summary Table

Erratum ID	Processor Line / Steppings		Title
	HCC	XCC	
	M-1	D-2	
ICX62.	No Fix	No Fix	MBA May Incorrectly Throttle Threads When Hyperthreading is Enabled
ICX63.	No Fix	No Fix	MBA 2.0 May Cause MMIO Traffic to be Throttled
ICX64.	No Fix	No Fix	Cannot Inject Errors Into PCLS Bits
ICX65.	No Fix	No Fix	SNC2 And Hemisphere Mode do Not Work Correctly on Processors With 38 CHAs
ICX66.	No Fix	No Fix	CAP Error And ECC Error During ADC/ADDDC Sparing May Not be Corrected
ICX67.	Fixed	Fixed	Processor IERR Condition Followed by Warm Reset May Encounter Subsequent Fatal Error
ICX68.	No Fix	No Fix	NSR Field Attribute Does Not Comply With PCIe Base Specification 4.0
ICX69.	Fixed	Fixed	Intermittent Correctable Memory Errors May be Observed
ICX70.	Fixed	Fixed	Intel® UPI CRC Errors May be Detected During Power Management Transitions
ICX71.	No Fix	No Fix	Unmapped QDT DMA Reads May Result in Unpredictable System Behavior
ICX72.	No Fix	No Fix	Unexpected System Behavior May Occur During INVD Instruction Execution
ICX73.	No Fix	No Fix	Incorrect Intel® AVX2 And Intel® AVX-512 High Priority Frequencies May Be Reported
ICX74.	No Fix	No Fix	Configuring ADL May Prevent Package C-States Entry
ICX75.	Fixed	Fixed	DDR-T Interrupts During Warm Reset May Lead to a System Hang
ICX76.	Fixed	Fixed	Intermittent Intel UPI Test Failures May Be Observed During BSCAN
ICX77.	No Fix	No Fix	PCIe Rx Common Mode Impedance May be Too Low During Reset or Power-Down
ICX78.	No Fix	No Fix	Uncore Semaphore Capability May Not Generate a Semaphore Error Machine Check Exception
ICX79.	No Fix	No Fix	Uncore FIVR Fault May be Logged Incorrectly
ICX80.	No Fix	No Fix	Intel® SST-CP May Not be Dynamically Configurable
ICX81.	Fixed	Fixed	CHA Data Parity Error or Writeback LLC Miss May be Reported
ICX82.	Fixed	Fixed	WBINVD Delays May Lead to a Machine Check Exception
ICX83.	Fixed	Fixed	Mesh to Memory Transactions Timeout During Memory Stress Test
ICX84.	No Fix	No Fix	Certain Processor Units May Not Reach Intel® AVX-512 P1 All-cores Base Frequency
ICX85.	Fixed	Fixed	PCIe EB Error May Be Escalated to Receiver Errors



Errata Summary Table

Erratum ID	Processor Line / Steppings		Title
	HCC	XCC	
	M-1	D-2	
ICX86.	Planned Fix	Planned Fix	Disabling All Processor Cores on First Physical Row May Lead to an MCE
ICX87.	Fixed	Fixed	Unpredictable System Behavior May Occur Due to Memory Read Roundtrip Latency
ICX88.	No Fix	No Fix	A PECl Request May Receive an Incorrect Response

Specification Changes

Number	Specification Changes
1	None for this revision of this specification update.

Specification Clarifications

No.	Specification Clarifications
1	None for this revision of this specification update.

Documentation Changes

No.	Documentation Changes
1	None for this revision of the specification update.

Errata Details

ICX1. Memory Errors in a VLS Region on a Certain Device May Not be Properly Corrected

Problem: Under complex micro-architectural conditions, when Adaptive Data Correction (ADC) or Adaptive Double Device Data Correction (ADDDC) is enabled, and the system has spared out DRAM device 0, 1, 3, 4, 5, 8, 13, 15, or 16, and the system is in Virtual Lockstep (VLS) mode, then if a limited subset of multi-bit errors are detected on primary DRAM device 16 in the VLS region, those errors may not be properly corrected.

Implication: The system may experience unpredictable system behavior. Intel has only observed this behavior under synthetic testing conditions.

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX2. Wrong Page Access Semantics May be Reported When Intel® SGX ENCLU[EMODPE] Instruction Generates Page Fault (#PF) Exception

Problem: When Intel® Software Guard Extensions (Intel® SGX) extends an Enclave Page Cache (EPC) via the page permissions instruction (ENCLU[EMODPE]) and generates a Page Fault (#PF), even though the page permissions instruction access is a read access to the target page, the Page Fault Error Code (#PF's PFEC) will indicate that the fault occurred on a write (PFEC.W bit will be set) instead.

Implication: This erratum may impact debugging Intel SGX enclaves software. Intel has not observed this erratum with any commercially available software.

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX3. Writing Non-Zero Values to Read Only Fields in IA32_THERM_STATUS MSR May #GP

Problem: IA32_THERM_STATUS MSR (19CH) includes Read-Only (RO) fields as well as writable fields. Writing a non-zero value to any of the read-only fields may cause a #GP.

Implication: Due to this erratum, software that reads the IA32_THERM_STATUS MSR, modifies some of the writable fields, and attempts to write the MSR back may #GP.

Workaround: None identified.

Status: For the Steppings affected, refer to the [Summary Tables of Changes](#).

ICX4. VMREAD/VMWRITE Instructions May Not Fail When Accessing an Unsupported Field in VMCS

Problem: The execution of VMREAD or VMWRITE instructions should fail if the value of the instruction's register source operand corresponds to an unsupported field in the Virtual Machine Control Structure (VMCS). The correct operation is that the logical processor will set the Zero Flag (ZF), write 0CH into the VM-instruction error field and for VMREAD leave the instruction's destination unmodified. Due to this erratum, the instruction may instead clear the ZF, leave the VM-instruction error field unmodified and for VMREAD modify the contents of its destination.

Implication: Accessing an unsupported field in VMCS may fail to properly report an error. In addition, a VMREAD from an unsupported VMCS field may unexpectedly change its destination. Intel has not observed this erratum with any commercially available software.

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX5. VERR Instruction Inside VM-Entry May Cause DR6 to Contain Incorrect Values

Problem: Under complex micro-architectural conditions, a VERR instruction that follows a VM-entry with a guest-state area indicating MOV SS blocking (bit 1 in the Interruptibility state) and at least one of B3-B0 bits set (bits [3:0] in the pending debug exception) may lead to incorrect values in DR6

Implication: Due to this erratum, DR6 may contain incorrect values. Intel has not observed this erratum with any commercially available software.

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX6. Vector Masked Store Instructions May Cause Write Back of Cache Line Where Bytes Are Masked

Problem: Vector masked store instructions to Write-Back (WB) memory-type that cross cache lines may lead to CPU writing back cached data even for cache lines where all of the bytes are masked.

This can affect MMIO (Memory Mapped IO) or non-coherent agents in the following ways:

For MMIO range that is mapped as WB memory type, this erratum may lead to Machine Check Exception (MCE) due to writing back data into the MMIO space. This applies only to cross page vector masked stores where one of the pages is in MMIO range.

If the CPU cached data is stale, for example in the case of memory written directly by a non-coherent agent (agent that uses non-coherent writes), this erratum may lead to writing back stale cached data even if these bytes are masked.

Implication: CPU may generate writes into MMIO space which lead to MCE, or may write stale data into memory also written by non-coherent agents.

Workaround: It is recommended not to map MMIO range as WB. If WB is used for MMIO range, OS or VMM should not map such MMIO page adjacent to a regular WB page (adjacent on the linear address space, before or after the I/O page). Memory that may be written by non-coherent agents should be separated by at least 64 bytes from regular memory used for other purposes (on the linear address space).

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX7. VCVTPS2PH To Memory May Update MXCSR in The Case of a Fault on The Store

Problem: Execution of the VCVTPS2PH instruction with a memory destination may update the MXCSR exceptions flags (bits [5:0]) if the store to memory causes a fault (e.g., #PF) or VM exit. The value written to the MXCSR exceptions flags is what would have been written if there were no fault.

Implication: Software may see exceptions flags set in MXCSR, although the instruction has not successfully completed due to a fault on the memory operation. Intel has not observed this erratum to affect any commercially available software.

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX8. SMRAM State-Save Area Above the 4 GB Boundary May Cause Unpredictable System Behavior

Problem: If the BIOS uses the RSM instruction to load the SMBASE register with a value that would cause any part of the SMRAM state-save area to have an address above 4-GB, subsequent transitions into and out of System Management Mode (SMM) might save and restore processor state from incorrect addresses.

Implication: This erratum may cause unpredictable system behavior. Intel has not observed this erratum with any commercially available system.

Workaround: Ensure that the SMRAM state-save area is located entirely below the 4 GB address boundary.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX9. Single Correctable Error Can be Logged Twice if Patrol Scrub Reads Address When Read Transaction is in Flight to Same Address

Problem: When patrol scrubbing reads an address with a correctable ECC error, and at the same time a memory read transaction is in flight to that address, a single correctable error may be logged twice. These errors get logged in the RETRY_RD_ERR_LOG register BDF=(U0, 12, 0) offset 0x22C60 and in the MMIO ECC Correctable Error Counter Registers (22C18h-22C24h/26C18h-26C24h).

Implication: When this erratum occurs, an ECC error from one cache line could result in two correctable errors instead of one. Therefore, incorrectly increasing the overall correctable error count.

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX10. Processor May Hang if Warm Reset Triggers During BIOS Initialization

Problem: Under complex micro-architectural conditions, when the processor receives a warm reset during BIOS initialization, the processor may hang with a machine check error reported in IA32_MCI_STATUS, with MCACOD (bits [15:0]) value of 0400H, and MSCOD (bits [31:16]) value of 0080H.

Implication: Due to this erratum, the processor may hang. Intel has only observed this erratum in a synthetic test environment.

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX11. Placing Posted-Interrupt Descriptors Within The PRMRR May Result in a Processor Hang

Problem: Posted-interrupt processing is a virtualization feature for interrupts which requires configuring addresses in the posted-interrupt descriptor fields in the Virtual Machine Control Structure (VMCS). Configuring posted-interrupt descriptors addresses that are within the PRMRR (Processor Reserved Memory Range Register, defined by MSR 1F4H and MSR 1F5H) may result in a logical processor hang.

Implication: This erratum may result in a processor hang. Intel has not observed this erratum with any commercially available software.

Workaround: Virtual Machine Monitor (VMM) software should not use addresses within the PRMRR for posted-interrupt descriptors.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX12. Placing Page Table Information in The APIC-Access Page May Lead to Unexpected Page Faults While Performing Enclave Accesses

Problem: Guest-physical access using a guest-physical address that translates to an address on the APIC-access page (as identified by the APIC-access address field in the VMCS) should cause an APIC-access VM exit. This includes page table information accesses done as part of page translation (page walks). Due to this erratum placing page table information in the APIC-access page may result in a page fault instead of VM exit when the page translation is done as part of an enclave access.

Implication: Software that places page table information in the APIC access page may get page faults on executing enclave accesses, instead of exiting to the Virtual-Machine Monitor (VMM). Intel has not observed this erratum with any commercially available software.

Workaround: Software should not place page table information in the APIC access page.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX13. Performance Monitoring Load Latency Events May be Inaccurate For Gather Instructions

Problem: The performance monitoring events MEM_TRANS_RETIRED.LOAD_LATENCY_* (Event CDH; UMask 01H; any latency) count load instructions whose latency exceed a predefined threshold, where the loads are randomly selected using the load latency facility (an extension of PEBS). However due to this erratum, these events may count incorrectly for VGATHER*/VPGATHER* instructions

Implication: The Load Latency Performance Monitoring events may be inaccurate for Gather instructions.

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX14. Performance Monitoring Counters May Undercount When Using CPL Filtering

Problem: Performance Monitoring counters configured to count only OS or only USR events (by setting only one of bits 16 or 17 in IA32_PERFEVTSELx) may undercount for a short cycle period of typically less than 100 processor clock cycles after the processor transitions to a new CPL. Events affected may include those counting CPL transitions (by additionally setting the edge-detect bit 18 in IA32_PERFEVTSELx).

Implication: Due to this erratum, Performance Monitoring counters may report counts lower than expected.

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX15. PEBS Eventing IP Field May be Incorrect After Not-Taken Branch

Problem: When a Precise-Event-Based-Sampling (PEBS) record is logged immediately after a not-taken conditional branch (Jcc instruction), the Eventing IP field should contain the address of the first byte of the Jcc instruction. Due to this erratum, it may instead contain the address of the instruction preceding the Jcc instruction.

Implication: Performance monitoring software using PEBS may incorrectly attribute PEBS events that occur on a Jcc to the preceding instruction.

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX16. Overlap Between APIC And SMRR2 Memory-Mapped Registers Will Not Signal a #GP

Problem: Overlapped APIC and SMRR2 Memory-mapped configurations will not cause a General Protection (#GP) exception when configured

Implication: Due to this erratum, a #GP exception will not be triggered. Intel has not observed this erratum with any commercially available software or platform.

Workaround: None identified. Software should not overlap SMRR2 with APIC registers page.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX17. Overflow Flag in IA32_MC0_STATUS MSR May be Incorrectly Set

Problem: Under complex micro-architectural conditions, a single internal parity error seen in IA32_MC0_STATUS MSR (401h) with MCACOD (bits 15:0) value of 5h and MSCOD (bits 31:16) value of 7h, may set the overflow flag (bit 62) in the same MSR.

Implication: Due to this erratum, the IA32_MC0_STATUS overflow flag may be set after a single parity error. Intel has not observed this erratum with any commercially available software.

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX18. Intel SGX Enclave Accesses to The APIC-Access Page May Cause APIC-Access VM Exits

Problem: In VMX non-root operation, Intel SGX (Software Guard Extensions) enclave accesses to the APIC-access page may cause APIC-access VM exits instead of page faults.

Implication: A Virtual-Machine Monitor (VMM) may receive a VM exit due to an access that should have caused a page fault, which would be handled by the guest operating system (OS).

Workaround: A VMM avoids this erratum if it does not map any part of the Enclave Page Cache (EPC) to the guest's APIC-access address; an operating system avoids this erratum if it does not attempt indirect enclave accesses to the APIC.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX19. Intel® PT TIP or FUP Packets May be Dropped Without OVF Packet

Problem: The Intel® Processor Trace (Intel® PT) Overflow (OVF) packet may not be generated when only Target IP Packets (TIPs) and/or Flow Update Packets (FUPs) are lost due to internal buffer overflow.

Implication: A decoder error will result from the missing FUP and/or TIP packets.

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX20. Intel PT CBR Packet May be Delayed or Dropped

Problem: Due to a complex set of microarchitectural conditions, the Intel PT (Processor Trace) CBR (Core:Bus Ratio) packet generated on a frequency change may be dropped, without an Overflow (OVF) packet, or may be inserted into the trace late, after other packets (including possibly another CBR) that were generated after the frequency change completed.

Implication: An Intel PT decoder may report an incorrect core:bus ratio to a portion of the trace, which may result in an incorrect wall clock time calculation.

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX21. Incorrect FROM_IP Value For an RTM Abort in BTM or BTS May be Observed

Problem: During Restricted Transactional Memory (RTM) operation when branch tracing is enabled using Branch Trace Message (BTM) or Branch Trace Store (BTS), the incorrect EIP value (From_IP pointer) may be observed for an RTM abort.

Implication: Due to this erratum, the From_IP pointer may be the same as that of the immediately preceding taken branch.

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX22. Incorrect Branch Predicted Bit in BTS/BTM Branch Records

Problem: Branch Trace Store (BTS) and Branch Trace Message (BTM) send branch records to the Debug Store management area and system bus respectively. The Branch Predicted bit (bit 4 of eighth byte in BTS/BTM records) should report whether the most recent branch was predicted correctly. Due to this erratum, the Branch Predicted bit may be incorrect.

Implication: BTS and BTM cannot be used to determine the accuracy of branch prediction.

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX23. In eMCA2 Mode, When The Retirement Watchdog Timeout Occurs CATERR# May be Asserted

Problem: A Retirement Watchdog Timeout (MCACOD = 0x0400) in Enhanced MCA2 (eMCA2) mode will cause the CATERR# pin to be pulsed in addition to an MSMI# pin assertion. In addition, a Machine Check Abort (#MC) will be pended in the cores along with the MSMI.

Implication: Due to this erratum, systems that expect to only see MSMI# will also see CATERR# pulse when a Retirement Watchdog Timeout occurs. The CATERR# pulse can be safely ignored.

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX24. IA32_RTIT_STATUS.FilterEn Bit Might Reflect a Previous Value

Problem: Under complex micro-architectural conditions, reading the IA32_RTIT_STATUS.FilterEn bit (bit 0 in MSR 571h) after entering or exiting an RTIT region might reflect a previous value instead of the current one.

Implication: Due to this erratum, IA32_RTIT_STATUS.FilterEn bit might reflect a previous value. This erratum has not been seen in any commercially available software.

Workaround: Software should perform an LFENCE instruction prior to reading the IA32_RTIT_STATUS MSR to avoid this issue.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX25. IA32_MC1_STATUS MSR May Not Log Errors When IA32_MC1_CTL MSR is Set to Not Signal Errors

Problem: Under complex micro-architectural conditions, IA32_MC1_STATUS MSR (405H) may not log a poison error when the enable bit (bit 0) in the IA32_MC1_CTL MSR (281H) is cleared.

Implication: Due to this erratum, poison errors might not be logged in the MC1 bank. Intel has not observed this erratum in any commercially available software.

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX26. False MC1 Error Reported in The Shadow of a Internal Timer Error

Problem: After a internal timer error has been reported in MC3_STATUS MSR (0x40d) with MCACOD (bits [15:0]) value of 0400H, and MSCOD (bits [31:16]) value of 0080H, under complex micro-architectural conditions, a false error may be reported in MC1_STATUS MSR (0x405) with MCACOD 0x174 or MCACOD 0x124.

Implication: Due to this erratum, a false MCE may be reported in MC1_STATUS MSR. Intel has not observed this erratum in a synthetic test environment.

Workaround: Software should ignore the MC1 error when it appears with an internal timer error.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX27. Debug Exceptions May Be Lost or Misreported When MOV SS or POP SS Instruction is Not Followed by a Write to SP

Problem: If a MOV SS or POP SS instruction generated a debug exception, and is not followed by an explicit write to the Stack Pointer (SP), the processor may fail to deliver the debug exception or, if it does, the DR6 register contents may not correctly reflect the causes of the debug exception.

Implication: Debugging software may fail to operate properly if a debug exception is lost or does not report complete information. Intel has not observed this erratum with any commercially available software.

Workaround: Software should explicitly write to the stack pointer immediately after executing MOV SS or POP SS.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX28. CPUID TLB Information is Inaccurate

Problem: CPUID leaf 16 (EAX=16H) subleaf 1 (ECX=01H) TLB information inaccurately reports that the instructions' 1st-level TLB is 8-way and supports both 4K and 2M/4M pages, although it is split into 16 sets of 8 ways for 4K pages and 2 sets of 8 ways for 2M/4M pages.

Implication: Software that uses CPUID instructions 1st-level TLB information may operate incorrectly. Intel has not observed this erratum to impact the operation of any commercially available software.

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX29. CPUID L2 Cache Information May be Inaccurate

Problem: CPUID extended function 80000006H (EAX=80000006H) inaccurately reports information about the L2 cache in ECX. The function reports that the L2 cache size is 256K divided into 8 ways, while the actual L2 size and structure should be inferred from reading CPUID leaf 04H sub-leaf 02H.

Implication: Software that uses CPUID extended leaf 80000006H L2 cache information may operate incorrectly. Intel has not observed this erratum to impact the operation of any commercially available software.

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX30. Configuring The PRMRR as Non-WB Might Lead to Incorrect VM-Exit Interruption Error Code

Problem: Under complex micro-architectural conditions, while working with PRMRR configured to be non-WB (Write Back), an Asynchronous Enclave Exit (AEX) caused by a page fault (#PF) that is followed by a VM-exit might lead to an incorrect VM-exit interruption error Code.

Implication: Due to this erratum, the error code captured in the VM-exit interruption error code might be incorrect and not indicate a page fault. Intel has only observed this erratum in a synthetic test environment.

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX31. An Invalid Algorithm in The CRYPTO_ALG Field of The MKTME_KEY_PROGRAM_STRUCT Will Not Cause an INVALID_ENC_ALG Failure as Expected

Problem: The supported encryption algorithms are specified in TME_CAPABILITY MSR (981h). Using PCONFIG instruction to config an invalid algorithm in CRYPTO_ALGS field of the MKTME_KEY_PROGRAM_STRUCT (bits [23:8] in the KEYID_CTRL) will not cause an INVALID_ENC_ALG failure as expected.

Implication: Due to this erratum, the INVALID_CRYPT_ALG bit (bit 4) reported by PCONFIG instruction might be incorrect and memory encryption may not commence. Intel has not observed this erratum in any commercially available software.

Workaround: Software should only write to supported CRYPTO_ALG bits as enumerated in TME_CAPABILITY MSR (981h).

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX32. A Spurious APIC Timer Interrupt May Occur After Timed MWAIT

Problem: Due to this erratum, a Timed MWAIT that completes for a reason other than the Timestamp Counter reaching the target value may be followed by a spurious APIC timer interrupt. This erratum can occur only if the APIC timer is in TSC-deadline mode and only if the mask bit is clear in the LVT Timer Register.

Implication: Spurious APIC timer interrupts may occur when the APIC timer is in TSC-deadline mode.

Workaround: TSC-deadline timer interrupt service routines should detect and deal with spurious interrupts.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX33. #GP on Segment Selector Descriptor That Straddles Canonical Boundary May Not Provide Correct Exception Error Code

Problem: During a #GP (General Protection Exception), the processor pushes an error code on to the exception handler's stack. If the segment selector descriptor straddles the canonical boundary, the error code pushed onto the stack may be incorrect.

Implication: An incorrect error code may be pushed onto the stack. Intel has not observed this erratum with any commercially available software.

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX34. x87 FPU Exception (#MF) May be Signaled Earlier Than Expected

Problem: x87 instructions that trigger #MF normally service interrupts before the #MF. Due to this erratum, if an instruction that triggers #MF is executing when an Enhanced Intel SpeedStep® Technology transitions, an Intel® Turbo Boost Technology transitions, or a Thermal Monitor events occurs, the #MF may be taken before pending interrupts are serviced.

Implication: Software may observe #MF being signaled before pending interrupts are serviced.

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX35. IERR Not Logged Correctly When Ubox Requested to Signal MSMI

Problem: The Ubox can be programmed to signal a Machine Check System Management Interrupt (MSMI) when an IERR is received from the core. In this case, Ubox will signal both IERR and MSMI and log an error into MCERRLOGGINGREG (Bus: 30; Device: 0; Function: 0; Offset: A8h) but not into IERRLOGGINGREG (Bus: 30; Device: 0; Function: 0; Offset: A4h).

Implication: The source of a core 3-strike timeout IERR cannot be identified while decoding the IERRLOGGINGREG registers in each socket.

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX36. PCIe* Surprise Link Down Events May Not be Reported

Problem: When the processor's PCIe root port encounters conditions that should generate a Surprise Link Down (SLD) event, such as LinkUp = 0, the processor may fail to log or report an SLD event in the ERRUNCSTS register (Bus: 1-4; Device: 1; Function: 0; Offset 104h).

Implication: When this erratum occurs, software that relies upon SLD reporting will not behave as intended.

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX37. PCIe RPPIO May Contain Incorrect Tag Value

Problem: The PCIe Root Port Programmable Input Output (RPPIO) Header Log 1 (BDFO) tag field may contain a tag value that does not match that transmitted on the PCIe link.

Implication: When this erratum occurs, it may not be possible to associate transactions on the PCIe link with transaction data logged in RPPIO. Intel has not observed any functional implications due to this erratum.

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX38. Uncore MC Bank Registers Corrected Error Count Field May Not Have a Sticky Most Significant Bit

Problem: The corrected error count field in IA32_MC[4..28]_STATUS MSR may not contain a sticky most significant bit, and corrected error count may roll over to 0.

Implication: Due to this erratum, there is no indication that the corrected error count has rolled over.

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).



ICX39. UPI Correctable Error May be Observed After Cold Resets And TCRH Events

Problem: UPI correctable errors (IA32_MCi_STATUS.MSCOD [bits 31:16] 0x22/0x23/0x30, IA32_MCi_STATUS.MCACOD=0x0E0F [bits 15:0]) may be observed after cold resets and Train Cold Run Hot (TCRH) events.

Implication: Due to this erratum, UPI Correctable Errors may be logged and lead to a link width change.

Workaround: It may be possible for the BIOS to workaround this erratum.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX40. Poisoned Locked Bus Transactions May Not Allow Warm Reset to Correctly Reset The Processor

Problem: On a system with Intel SGX enabled, if the processor receives poisoned data in response to a locked bus transaction while some cores are in or resuming from a Core C6 state, the resulting warm reset may not correctly reset the processor.

Implication: Due to this erratum, the system may not properly reset without a Cold Reset.

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX41. TOR Timeout During WBINVD May Cause System Hang

Problem: Under complex microarchitectural conditions, a TOR Timeout Error Machine Check Exception (Machine Check banks 9, 10, and 11 [MSRs 0x425, 0x429, and 0x42D] with IA32_MCi_STATUS.MSCOD=0x000C [bits 31:16]) may occur during a WBINVD instruction.

Implication: Due to this erratum, a system hang may occur.

Workaround: It may be possible for the BIOS to workaround this erratum.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX42. Intel® PT VMEntry Indication Depends on The Incorrect VMCS Control Field

Problem: An Intel® Processor Trace PIP (Paging Information Packet), which includes indication of entry into non-root operation, will be generated on VMEntry as long as the "Conceal VMX in Intel PT" field (bit 19) in Secondary Execution Control register (IA32_VMX_PROCBASED_CTLSS2, MSR 048BH) is clear. This diverges from expected behavior, since this PIP should instead be generated only with a zero value of the "Conceal VMX entries from Intel PT" field (Bit 17) in the Entry Control register (IA32_VMX_ENTRY_CTLSS MSR 0484H)

Implication: An Intel PT trace may incorrectly expose entry to non-root operation.

Workaround: A VMM (virtual machine monitor) should always set both the "Conceal VMX entries from Intel PT" field in the Entry Control register and the "Conceal VMX in Intel PT" in the Secondary Execution Control register to the same value.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX43. Intel PT Trace May Drop Second Byte of CYC Packet

Problem: Due to a rare microarchitectural condition, the second byte of a 2-byte CYC (Cycle Count) packet may be dropped without an OVF (Overflow) packet.

Implication: A trace decoder may signal a decode error due to the lost trace byte.

Workaround: None identified. A mitigation is available for this erratum. If a decoder encounters a multi-byte CYC packet where the second byte has bit 0 (Ext) set to 1, it should assume that 4095 cycles have passed since the prior CYC packet, and it should ignore the first byte of the CYC and treat the second byte as the start of a new packet.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX44. Intel PT TIP.PGD May Not Have Target IP Payload

Problem: When Intel PT (Intel Processor Trace) is enabled and a direct unconditional branch clears IA32_RTIT_STATUS.FilterEn (MSR 571H, bit 0), due to this erratum, the resulting TIP.PGD (Target IP Packet, Packet Generation Disable) may not have an IP payload with the target IP.

Implication: It may not be possible to tell which instruction in the flow caused the TIP.PGD using only the information in trace packets when this erratum occurs.

Workaround: The Intel PT trace decoder can compare direct unconditional branch targets in the source with the FilterEn address range(s) to determine which branch cleared FilterEn.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX45. Intel PT PSB+ May be Lost

Problem: Intel PT (Processor Trace) generates a PSB+ (Packet Stream Boundary+) set of packets periodically, based on the number of trace bytes written out. If the threshold for a PSB+ is reached while Intel PT is being disabled by clearing IA32_RTIT_CTL.TraceEn[0] (MSR 0570H) either during a VM-exit or after generating fewer than 8 bytes of trace since TraceEn was last set, that PSB+ may be lost.

Implication: An Intel PT decoder that is scanning for a PSB+ at which to begin decode may have to skip over more trace output bytes before finding one.

Workaround: Software processing the trace at runtime can detect that a PSB+ was dropped by checking that IA32_RTIT_STATUS.PacketByteCnt[48:32] (MSR 0571H) has recently crossed the PSB threshold, while scanning the trace to check that the expected PSB+ was not inserted. When a dropped PSB+ is detected, software can force a PSB+ to be inserted the next time Intel PT is enabled by clearing PacketByteCnt.70H) to 1, as an internal buffer overflow that loses a CYC packet will generate an OVF.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX46. Intel Processor Trace PSB+ Packets May Contain Unexpected Packets

Problem: Some Intel Processor Trace packets should be issued only between TIP.PGE (Target IP Packet.Packet Generation Enable) and TIP.PGD (Target IP Packet.Packet Generation Disable) packets. Due to this erratum, when a TIP.PGE packet is generated it may be preceded by a PSB+ (Packet Stream Boundary) that incorrectly includes FUP (Flow Update Packet) and MODE.Exec packets.

Implication: Due to this erratum, FUP and MODE.Exec may be generated unexpectedly.

Workaround: Decoders should ignore FUP and MODE.Exec packets that are not between TIP.PGE and TIP.PGD packets.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX47. Spurious PCIe Link Parity Errors May be Logged

Problem: The processor may log a spurious parity error into (Local Data Parity Mismatch Status registers (Bus: 1,2,3,4; Device: 2; Function: 0; Bits 15:0) G4LDPMSTS (Offset 420H), G4FRDPMSTS (Offset 424H) and G4SRDPMSTS (Offset 428H)) upon exiting Link L1 power states.

Implication: Due to this erratum, PCIe lanes may report spurious data parity mismatches. Intel has not observed any functional implications for this erratum.

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX48. IBIST Receiver Error Overflow Register Field Cannot be Cleared by Software

Problem: The receiver error overflow field of the IBIST Error Recovery and Receive Detection Status registers, IBSTERRRCRVSTS[0-3].RXERRCNTTOVRFLOW [Bus: 4-1; Device: 5; Function:0; Offsets: 624h, 62Eh, 634h, 63Ch; Bit 15] cannot be cleared by writing a "1" to clear this bit. A cold reset is required to clear this bit.

Implication: Due to this erratum, software may encounter inaccurate overflow logging.

Workaround: IBIST tests should use a cold reset between tests to clear the error overflow bit.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX49. MBM May Report Incorrect Bandwidth For Certain Access Strides

Problem: Memory Bandwidth Monitoring (MBM) samples the total memory traffic and upscales the results when reporting bandwidth. MBM may report zero to twice the actual memory bandwidth consumed for workloads that primarily access cache lines sequentially with physical address strides that are a multiples of 4 KB.

Implication: Due to this erratum, MBM may report inaccurate bandwidth for workloads that primarily access cache lines sequentially with physical address strides that are a multiples of 4 KB. Actual memory bandwidth is unaffected by this erratum.

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX50. Correctable Errors May Set The Overflow Bit

Problem: Machine Check Architecture (MCA) rules were updated to not set the overflow bit (bit 62) of IA32_MCi_STATUS due to Correctable Errors (CE). The overflow bit of IA32_MC[9-11]_STATUS MSRs (425H, 429H, 42D) may be incorrectly set if the first error is a correctable error and the second error is a non-correctable error.

Implication: Due to this erratum, a corrected error may cause the overflow bit to be set.

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX51. Enabled Error May Not be Logged When Other Errors Are Disabled

Problem: During the same cycle, a higher priority Uncorrected (UC) error or Software Recoverable Action Optional (SRAO) error which is disabled, may be logged rather than an enabled lower priority UC or SRAO error (for memory controller machine check banks 12-26).

Implication: Due to this erratum, software may not observe the enabled error. Intel has not observed this erratum in any commercially available software.

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX52. Uncore MC Bank Registers Corrected Error Count Field May Not Have a Sticky Most Significant Bit

Problem: The corrected error count field in IA32_MC[4..28]_STATUS MSR may not contain a sticky most significant bit, and corrected error count may roll over to 0.

Implication: Due to this erratum, there is no indication that the corrected error count has rolled over.

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX53. Machine Check Bank Status MSR May Not Set Overflow Bit When Multiple Uncorrectable Errors Occur

Problem: The IA32_MC4_STATUS (Offset: 411h) OVER field (bit 62) may not be set if multiple uncorrectable error types occur during the same cycle or if a single uncorrectable error type occurs over multiple cycles.

Implication: Due to this erratum, identification of multiple uncorrectable errors may not be possible.

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX54. FERR Registers Are Not Getting Cleared When CHANERR Register is Being Cleared

Problem: The per-channel FERR_(CHANERR/DMACOUNT/INTDMACOUNT/CHANSTS/DESC_CTRL/CADDR/NADDR) (Bus: 0; Device: 1; Function: 7-0 (CBDMA); Offsets: 180h, 184h, 186h, 188h, 190h, 198h, 1A0h) registers (FERR registers) do not get cleared when the corresponding per-channel CHANERR (Bus: 0; Device: 1; Function: 7-0 (CBDMA); Offset: A8h) register gets cleared.

Implication: Due to this erratum, the value in the stale FERR registers may be incorrect if its read when CHANERR==0.

Workaround: Software should not read the per-channel FERR registers unless the corresponding CHANERR register contains non-zero data.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX55. IOMMU Translation Requests to Interrupt Range May Fail

Problem: The Intel® Virtualization Technology (Intel® VT) for Directed I/O (Intel® VT-d) Architecture Specification specifies that DMA remapping hardware (IOMMU) should return a successful response with U=1 to a Translation Request with address in the interrupt range (0xFEExxxxx).

Implication: Due to this erratum, the DMA remapping hardware provides a response of Completer Abort. Intel has only observed this erratum in a synthetic testing environment.

Workaround: None identified. Devices should always use Untranslated Request when using address from the MSI register of the device.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX56. Internal Firmware Errors May Not Set Error Enable Bit

Problem: The processor does not set the error enable (EN) bit of the IA32_MC6_STATUS MSR (419h; bit 60) when certain internal firmware errors are detected. IA32_MC6_STATUS MSR field MCACOD (bits 15:0) are correctly set to 406h.

Implication: Software that relies on the EN bit may not operate properly. This type of error is always signaled and will result in system shutdown.

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).



ICX57. UPI PH_PLS.SRstRcvdP Value May be Incorrect Following a UPI PHY Reset

Problem: The value in the UPI register S_RST_RCVD_P (KTIREUT_PH_PLS Bus 30; Device 2; Function 2; Offset 160h; Bit 14) is reset and cleared instead of taking the value in S_RST_RCVD (KTI_REUT_PH_CLS Bus 30; Device 2; Function 2; Offset 164h; Bit 14) following a UPI PHY reset.

Implication: Due to this erratum, software relying on KTIREUT_PH_PLS following a UPI reset may contain inaccurate logging details.

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX58. Spurious Write Data Parity Errors May be Logged

Problem: In 2S systems, a spurious Write Data Parity Error (MSCOD = 0x002, MCACOD=0x0405) may be logged in the memory controller machine check bank status register (Bank 13, 14, 17, 18, 21, 22, 25, 26 and MSRs 0x435, 0x439, 0x449, 0x455, 0x459, 0x465 and 0x569). The same errors will be logged in the associated shadow registers at MMIO offset 23440h from the MEM[0-7]_BAR registers (Bus 30, Device 0, Function 1, Offsets D8h, DCh, E0h, E4h, E8h, ECh, F0h, and F4h).

Implication: When poison is enabled (MCG_CONTAIN.POISON_ENABLE = 1 (MSR 178h, bit 0), a spurious Write Data Parity Error may be logged and will be signaled as a UCNA error, but there will be no poison data in memory. Software that relies on UCNA error reporting may take unnecessary actions. When poison is not enabled, the spurious Write Data Parity Error may result in a fatal machine check exception.

Workaround: It is possible for BIOS to contain a workaround for this erratum.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX59. PKG_MIN_PWR May be Incorrect

Problem: Certain processors may report an incorrect value in the PKG_MIN_PWR field (Bits 30:16) of the PACKAGE_POWER_SKU_CFG register (Bus: 31; Device 30; Function 0; Offset 80h).

Implication: Software that utilizes PKG_MIN_PWR to budget processor or platform power may not behave as intended.

Workaround: It is possible for BIOS to contain a workaround for this erratum.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX60. PN_POWER_OF_SKU May be Incorrect

Problem: Certain processors may report an incorrect value in the PN_POWER_OF_SKU field (Bits 14:0) of the POWER_LIMIT_MISC_INFO_CFG register (Bus: 31; Device 30; Function 5; Offset E0h).

Implication: Software that utilizes PN_POWER_OF_SKU to budget processor or platform power may not behave as intended.

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX61. PCIe Surprise Link Down Logging May be Unexpectedly Blocked

Problem: In the absence of a power controller, software is still allowed to set the Power Controller Control (PCC) bit to a value of 1 in SLOTCTL (Bus 1,2,3,4; Device 2; Function 0; Offset 58h; bit 10). This action blocks logging of Surprise Link Down (SLD) errors regardless of the state of the Power Controller Present (PCP) bit in SLOTCAP (Bus 1,2,3,4; Device 2; Function 0; Offset 54h bit 1). In the event of a PCIe slot losing power, associated SLD errors should only be blocked if the PCP is set.

Implication: Software that relies upon SLD status may not operate as expected. Intel has not observed this erratum in any commercially available software.

Workaround: Software should check that the SLOTCTL.PCP bit is set before writing the PCC bit in SLOTCTL.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX62. MBA May Incorrectly Throttle Threads When Hyperthreading is Enabled

Problem: When one logical processor is idle, the Memory Bandwidth Allocation (MBA) feature may select an incorrect MBA throttling value to apply to the core. An idle logical processor may behave as though the CLOS field in its associated IA32_PQR_ASSOC MSR (0xC8F) is set to the CLOS of the last active thread. When this occurs, the MBA throttling value associated with CLOS of the last active thread on the unused logical processor may be incorrectly applied to the physically co-located active logical processor.

Implication: An idle logical processor is interpreted to have the CLOS that the last active thread sets in its IA32_PQR_ASSOC MSR, which affects the calculation for the actual throttling applied to the physical core. When this erratum occurs, the MBA throttling value associated with a given core may be incorrect. This erratum does not affect use cases when both threads on a physical core are assigned the same CLOS.

Workaround: It is possible for BIOS to contain a partial mitigation for this erratum.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX63. MBA 2.0 May Cause MMIO Traffic to be Throttled

Problem: Memory Bandwidth Allocation (MBA) 2.0 may throttle Memory Mapped IO (MMIO) traffic even though this traffic does not consume memory bandwidth.

Implication: Due to this erratum, write throughput to MMIO, particularly using Write Combining memory types, may be adversely impacted.

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX64. Cannot Inject Errors Into PCLS Bits

Problem: The DRAM cache line error injection does not inject into Partial Cache Line Sparing (PCLS) bits. After an error injection, the bits covered by PCLS will not be flipped which may change the expected behavior on subsequent reads of the DRAM cache line.

Implication: Due to this erratum, software injecting errors in cache lines may not see the expected errors on reads to those cache lines. The severity of the error may be incorrect or there may be no error.

Workaround: None identified. Software should avoid injecting errors into the PCLS regions.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX65. SNC2 And Hemisphere Mode do Not Work Correctly on Processors With 38 CHAs

Problem: Sub-NUMA Clustering 2 (SNC2) and Hemisphere Mode (HM) do not work correctly on processors with 38 Caching and Home Agents (CHA).

Implication: On processors with 38 CHAs, if SNC2 or HM is enabled, the processor may exhibit unpredictable system behavior.

Workaround: It is possible for a BIOS code change to workaround this erratum.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX66. CAP Error And ECC Error During ADC/ADDDC Sparing May Not be Corrected

Problem: Under complex microarchitectural conditions, during Adaptive Data Correction/Adaptive Double Device Data Correction (ADC/ADDDC) sparing, a correctable Command/Address Parity (CAP) error and a correctable ECC error occurring simultaneously on the last address of the spare copy may not be properly corrected.

Implication: Due to this erratum, correctable CAP errors and correctable ECC errors may not be properly corrected resulting in an uncorrected error or unpredictable system behavior. This erratum has only been observed in a synthetic test environment.

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX67. Processor IERR Condition Followed by Warm Reset May Encounter Subsequent Fatal Error

Problem: Certain fatal error conditions that result in IERR assertion may fail to properly recover following a warm reset.

Implication: When this erratum occurs, the processor may require a global reset to boot the system.

Workaround: It is possible for a BIOS code change to contain a workaround for this erratum.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX68. NSR Field Attribute Does Not Comply With PCIe Base Specification 4.0

Problem: The access type of the No Soft Reset bit (bit 3) of the Power Management Control Status Register (PMCSR) (Bus: 1-4; Device: 5; Function: 0; Offset: 84h) is Read/Write/Locked; however, the PCIe Base Specification version 4.0 specifies this bit to be Read Only.

Implication: Due to this erratum, software that relies on the NSR bit may behave unexpectedly.

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX69. Intermittent Correctable Memory Errors May be Observed

Problem: The processor may observe intermittent correctable memory errors with non-homogeneous DRAM configurations.

Implication: Due to this erratum, intermittent correctable memory errors may be observed.

Workaround: It may be possible for a BIOS code change to workaround this erratum.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX70. Intel® UPI CRC Errors May be Detected During Power Management Transitions

Problem: Correctable CRC errors may be detected in machine check banks MC5_STATUS, MC7_STATUS, or MC8_STATUS (MSRs 415h, 41Dh, or 421h) with MSCOD = 0x30 or 0x23 and MCACOD = 0x0E0F when the Intel® Ultra Path Interconnect (Intel® UPI) link is entering or exiting L0p or L1 power management states.

Implication: Due to this erratum, correctable CRC errors may be detected during power state transitions.

Workaround: It is possible for the BIOS to contain a workaround for this erratum.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX71. Unmapped QDT DMA Reads May Result in Unpredictable System Behavior

Problem: Intel® Quick Data Technology (QDT) DMA reads to addresses that are not mapped in the IOMMU or reads to peer agents that result in read completion errors. An Unsupported Request/Completer Abort may result in unpredictable system behavior.

Implication: Due to this erratum, the system may exhibit unpredictable system behavior. Intel has not observed this erratum to impact any commercially available software.

Workaround: None identified. Software should not program the QDT controller with any source addresses that may receive completion errors.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX72. Unexpected System Behavior May Occur During INVD Instruction Execution

Problem: During the execution of an INVD instruction, if there is a partial cacheline write from the I/O subsystem in progress, the processor may generate an unexpected machine check exception or other unexpected system behavior.

Implication: When this erratum occurs, the processor may experience unexpected system behavior. Intel has only observed this erratum in a synthetic test environment.

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX73. Incorrect Intel® AVX2 And Intel® AVX-512 High Priority Frequencies May Be Reported

Problem: The processor may incorrectly report High Priority Intel® Advanced Vector Extensions 2 (Intel® AVX2) and Intel® Advanced Vector Extensions 512 (Intel® AVX-512) frequencies higher than the corresponding SSE frequency.

Implication: Due to this erratum, software that reads High Priority Intel AVX2 and Intel AVX-512 frequencies may report an incorrect value. The processor's Intel AVX2 and Intel AVX-512 frequencies will not exceed the corresponding SSE frequency.

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX74. Configuring ADL May Prevent Package C-States Entry

Problem: If the Agent Debug Logic (ADL) is configured after Package C-states are enabled, it is possible for future Package C-states (deeper than Package C0) to be blocked.

Implication: Due to this erratum, Package C-states deeper than Package C0 may not be achieved, leading to higher than anticipated platform power consumption.

Workaround: None Identified. It is possible for software to contain code to enable ADL prior to enabling deeper Package C-states.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX75. DDR-T Interrupts During Warm Reset May Lead to a System Hang

Problem: If a DDR-T interrupt occurs during warm reset it may not get serviced, which may lead to a system hang.

Implication: Due to this erratum, a system hang may occur.

Workaround: It is possible for the BIOS to contain a workaround for this erratum.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX76. Intermittent Intel UPI Test Failures May Be Observed During BSCAN

Problem: Sending a Boundary Scan (BSCAN) external test pattern from an Intel UPI transmitter may encounter intermittent failures where the pattern is not correctly received by the Intel UPI receiver on the remote socket.

Implication: A BSCAN pattern from an Intel UPI transmitter may not be observed correctly at an Intel UPI receiver.

Workaround:

Workaround: It is possible for the BIOS to contain a workaround for this erratum.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX77. PCIe Rx Common Mode Impedance May be Too Low During Reset or Power-Down

Problem: A PCIe receiver may exhibit impedance of approximately 2 k Ω - 3 k Ω at reset and 1 k Ω at power-down compared to expected impedance above 20 k Ω (ZRX-HIGH-IMP-DC-POS).

Implication: The processor does not meet the *PCI Express Base Specification*, Revision 4.0 receiver impedance greater than 20 k Ω . Intel has not observed any functional impact due to this erratum.

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX78. Uncore Semaphore Capability May Not Generate a Semaphore Error Machine Check Exception

Problem: This processor's semaphore capability (LOCALAQUSEMP[1:0] and SYSTEMAQUSEMP[1:0] [Bus 30, Device 0, Function 2, Offsets 0x184, 0x190, 0x18C, 0x188]) does not generate a Semaphore Error machine check exception (MCACOD = 0x0407, MSCOD = 0x800E) if the semaphore's tail pointer passes its head pointer.

Implication: Due to this erratum, the system may exhibit unpredictable system behavior instead of a machine check exception

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX79. Uncore FIVR Fault May be Logged Incorrectly

Problem: If an Uncore FIVR fault occurs prior to the first BIOS Microcode Update (MCU) load, it may be reported in machine check bank IA32_MC4_STATUS (MSR 411h) as an MCA_DISPATCHER_RUN_BUSY_TIMEOUT (MSCOD=0xB0, MCACOD=0x402) instead of an MCA_FIVR_PD_HARDERR (MSCOD=0x56, MCACOD=0x402).

Implication: Due to this erratum, an incorrect FIVR fault error may be logged.

Workaround: None identified.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX80. Intel® SST-CP May Not be Dynamically Configurable

Problem: The processor supports both the WRITE_PCU_MISC_CONFIG and WRITE_PM_CONFIG mailbox commands. If the WRITE_PCU_MISC_CONFIG mailbox command is used to enable Intel® Speed Select Technology - Core Power (Intel® SST-CP), then the WRITE_PM_CONFIG mailbox command cannot be used to disable it.

Implication: Due to this erratum, Intel SST-CP may not be dynamically disabled as expected.

Workaround: Software should use only the WRITE_PM_CONFIG mailbox command to dynamically configure Intel SST-CP.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX81. CHA Data Parity Error or Writeback LLC Miss May be Reported

Problem: A processor with a reported junction temperature above 75 °C and an uncore frequency > 2 GHz, a fatal Machine Check Exception (MCE) may be observed on Cache Home Agent (CHA) Machine Check Banks (Banks 9, 10, and 11) MCI_STATUS MSRs (425h, 429h, or 42Dh) due to CHA data parity errors (MCACOD = 405h and MSCOD = Ah) or a Writeback LLC miss (MCACOD = 1146h and MSCOD = Bh).

Implication: Due to this erratum, a fatal MCE may be observed.

Workaround: It is possible for the BIOS to contain a workaround for this erratum.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX82. WBINVD Delays May Lead to a Machine Check Exception

Problem: Executing a WBINVD instruction during IO traffic and lock instructions may result in an Internal Timer Error Machine Check (IA32_MCI_STATUS.MCACOD=80h; bits [31:16], IA32_MCI_STATUS.MCACOD=400h; bits [15:0]).

Implication: An Internal Timer Error Machine Check may be reported during a WBINVD instruction.

Workaround: It may be possible for BIOS to contain code to work around this issue.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX83. Mesh to Memory Transactions Timeout During Memory Stress Test

Problem: When the processor is utilizing Intel® Optane™ persistent memory in Memory Mode, under complex microarchitectural conditions when running memory stress testing a soft hang may occur.

Implication: Due to this erratum, a system hang may occur with a Timeout Error Machine Check reported in MCI_STATUS of machine check banks 12, 16, 20, or 24 (MSRs 431h, 441h, 451h, 461h with MSCOD (bits[31:16]) value of 0009h and MCACOD (bits[15:0]) value of 0400h).

Workaround: It may be possible for BIOS to contain a workaround for this erratum.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX84. Certain Processor Units May Not Reach Intel® AVX-512 P1 All-cores Base Frequency

Problem: Certain processor units may not reach specified base all-cores active Intel® AVX-512 frequency when running benchmarks with high utilization of Intel® AVX-512 instructions.

Implication: Due to this erratum, impacted processors may run at a lower base all-cores active Intel® AVX512 P1 core frequency.

Workaround: It may be possible for BIOS to contain a partial workaround for this erratum.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX85. PCIe EB Error May Be Escalated to Receiver Errors

Problem: During PCIe configuration and recovery, logging of Elastic Buffer (EB) errors are not masked as per PCIe 4.0 Spec Sec 4.2.6 and are escalated to receiver errors in the PCIe Correctable Error Status Register (ERRCORSTS) (Bus: [4-1]; Device: 2; Function: 0; Offset: 110h).

Implication: Due to this erratum, an incorrect receiver error may be reported.

Workaround: It may be possible for a BIOS code change to contain a workaround for this erratum.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX86. Disabling All Processor Cores on First Physical Row May Lead to an MCE

Problem: When the cores on the first physical row (cores 0-3 and 19-22 for XCC family processors; cores 0-2 and 13-15 for HCC family processors) are disabled in BIOS, a Machine Check Exception (MCE) failure may be logged during reset in Machine Check Banks (Banks 9, 10, and 11) MCI_STATUS MSR's (425h, 429h, or 42Dh).

Implication: Due to this erratum, a fatal MCE may occur and the system may fail to boot.

Workaround: None identified. Re-enabling the cores followed by a cold reset will recover the system.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX87. Unpredictable System Behavior May Occur Due to Memory Read Roundtrip Latency

Problem: During DDR4 read operations with data scrambling enabled, setting any of the values in the RT_rank fields in DDRCRINTFROUNDTRIP0_CH1 register (Offset: 13F30h) RT_RANK(0-3) (bits 27:0) or DDRCRINTFROUNDTRIP1_CH1 register (Offset: 13F34h) RT_RANK(4-7) (bits 27:0) to a value greater or equal to 5Ch may lead to unpredictable system behavior.

Implication: When this erratum occurs, the system may exhibit unpredictable behavior.

Workaround: It may be possible for a BIOS code change to contain a workaround for this erratum.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

ICX88. A PECCI Request May Receive an Incorrect Response

Problem: An additional request issued on the PECCI interface prior to the previous request completing may lead to the initial response being used as the response for the second request.

Implication: Due to this erratum, PECCI requests may not receive the correct response.

Workaround: None identified. The device needs to wait for the response before issuing another request.

Status: For the steppings affected, refer to the [Summary Tables of Changes](#).

Specification Changes

There are no specification changes in this specification update revision.



Specification Clarifications

There are no specification clarifications in this specification update revision.

Documentation Changes

There are no documentation changes in this specification update revision.