# Stratix 10 TX SI Development Kit Power Tree

FPGA Power UP Sequencing:

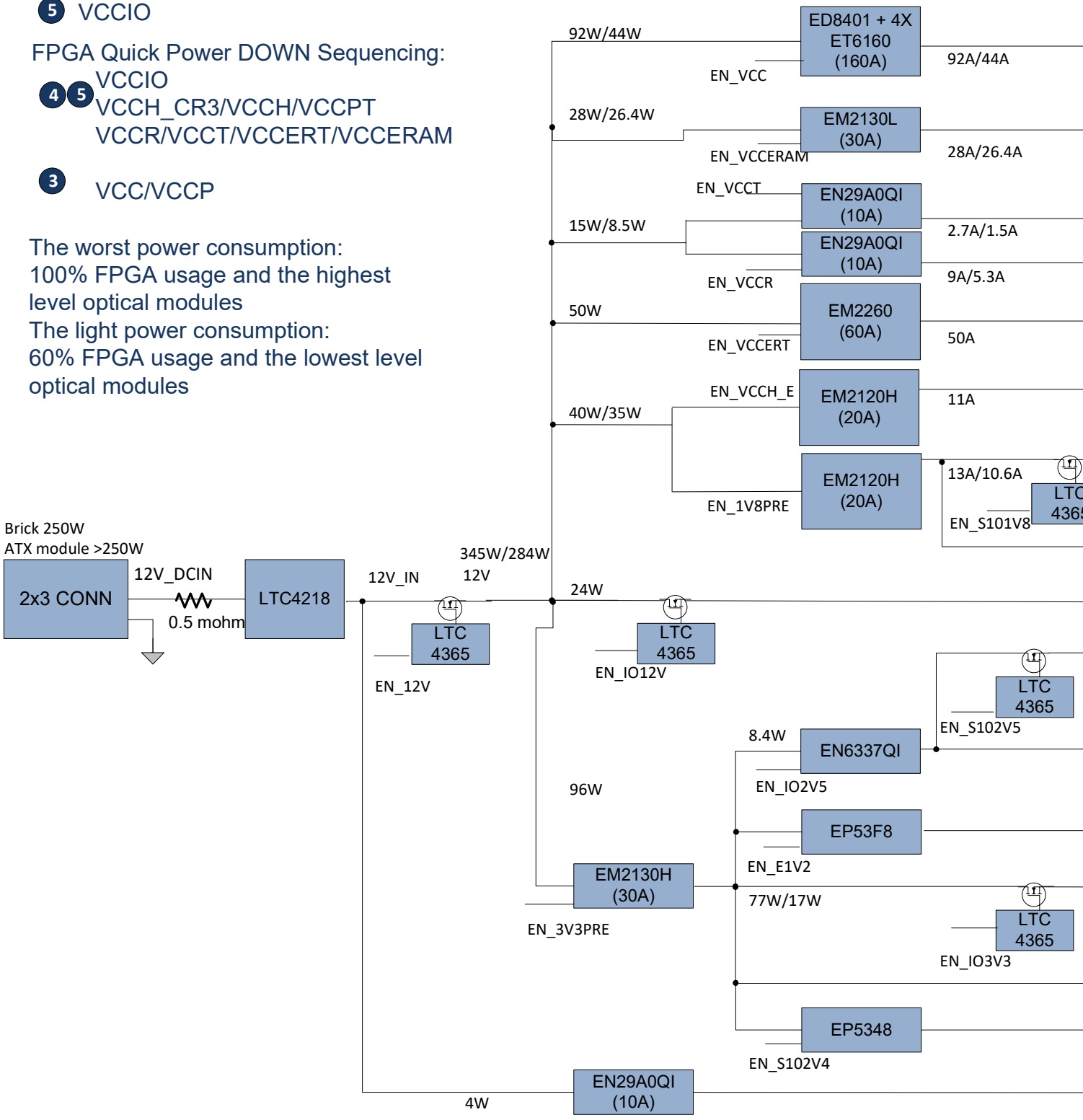
3 VCC/VCCP/VCCERAM
VCCR/VCCT/VCCERT
4 VCCH_CR3/VCCH/VCCPT
5 VCCIO

FPGA Quick Power DOWN Sequencing:

4 5 VCCIO
VCCH_CR3/VCCH/VCCPT
VCCR/VCCT/VCCERT/VCCERAM

3 VCC/VCCP

The worst power consumption:
100% FPGA usage and the highest level optical modules
The light power consumption:
60% FPGA usage and the lowest level optical modules



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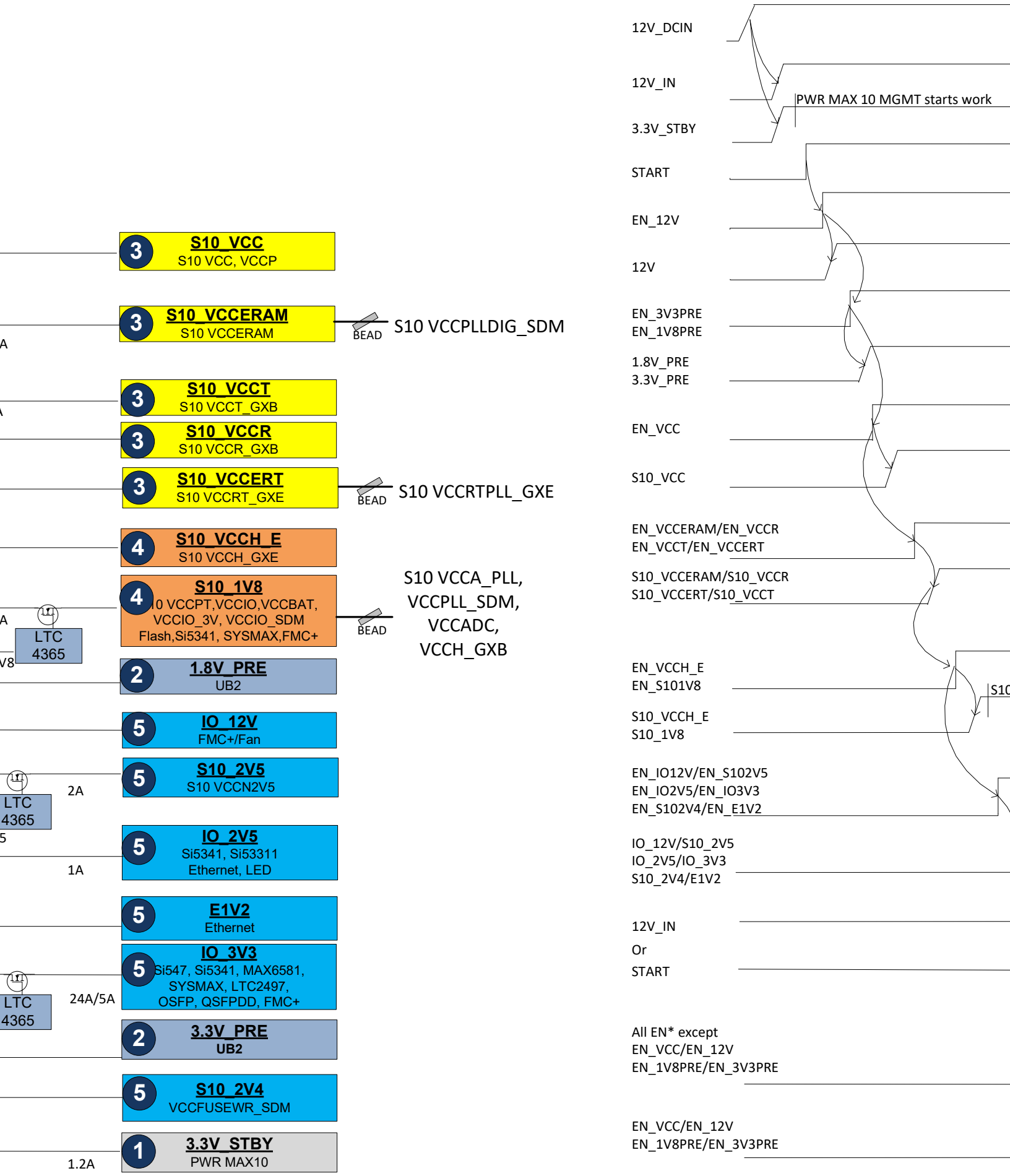

## Power Up/Down Sequence

ts work