Carrier Ethernet Switches | 26-52 Gbps Transport Switch | TPX3103

Altera's TPX3103 provides a Carrier Ethernet Switch solution, which supports all combinations of Ethernet and MPLS packet transport switching protocols.

TPX3103 solutions are based on SoftSilicon® technology which guarantees that the evolution of features and protocols can be supported and also makes it possible to adapt to specific interface requirements.

Family Key Features

- Integrated Packet Processor and Traffic Manager
- Up to 52 Gbps packet switch solution
- True deterministic packet switching performance

– the switch capacity is independent on the amount and combinations of look-ups

- Supports E(VP)-LINE / -LAN / -TREE services based on Ethernet and MPLS pseudowire technologies
- Hardware based ETH and MPLS OAM support for sub 50 ms protection switching
- Advanced traffic management with per flow policing
- Equipment protection through redundant dual-device solution with graceful degradation to half bandwidth
- Up to 24 built-in triple-speed Ethernet SGMII MAC interfaces
- Up to 2 built-in 10 GbE XGMII Ethernet interfaces
- SPI-4.2 interface supporting multiple transport technologies
- Supports deep packet buffers through storage in external memory
- Handles all look-ups without additional TCAM
- High-level driver software designed for quick and easy integration

Transport Switching

Packet switching solutions for transport networks is based on layer 2 Ethernet and MPLS switching protocols complemented with traffic management and OAM support in order to resemble the traditional carrier class attributes of SONET/SDH networks as close as possible.

Support of all these requirements calls for a solution that not only meet stringent carrier class requirements, but is also flexible enough to allow changes in standards and new technologies to be easily accommodated.

The TPX3103 series provides just that. It fully supports all of the above technologies and protocols while also providing a carrier class, integrated packet processor and traffic management solution.

Designed according to MEF, ITU-T, IEEE and IETF specifications, TPX3103 provides key features that enable the deployment of true Carrier Class packet networks, such as redundancy, protection, OAM support, fault & service management and advanced Quality of Service (QoS) features.

The TPX3103 is ideal for both linecard and standalone applications. The SPI-4.2 interface and the ability to switch across a large number of logical interface makes it ideal for MSSP and P-OTS applications in conjunction with Ethernet over SONET / SDH / OTN mappers.

Complete Support and Flexibility

TPX3103 is based on SoftSilicon® technology providing flexibility not only in which features and protocols are supported, but also which interfaces should be provided. For example, a 10 Gbps Ethernet interface can be exchanged with a SPI-4.2 interface to support Ethernet over SONET/SDH or WDM/OTN.

Three speed grade variants of the TPX3103 are available:

- 26 Gbps, 32.0 Mpps,
- 22 Gbps, 27.0 Mpps,
- 20 Gbps, 24.5 Mpps

Deterministic Performance

The TPX3103 provides guaranteed, deterministic packet processing performance. Every packet is guaranteed to be processed within the same, fixed number of clock cycles no matter the number and combinations of Ethernet, MPLS and pseudo-wire look-ups to be performed.

Carrier Class Features

The design includes hardware based ETH and MPLS OAM and protection features. The TPX3103 implements hardware based sub 50 ms protection switching for hundreds of VLAN flows or MPLS tunnels.

In a packet network with switching between high and low capacity pipes you will inevitably have burst of packets. In order to assure that packets are not lost it is important to have large enough external packet memory that can buffer these bursts as supported by TPX3103.

TPX3103 has a unique capacity scaling / redundancy solution that allows two devices to be coupled together to provide double capacity in any aspect. By using this capability a 52 Gbps switch can implemented in two chips. In the event of a failure in one of the devices, the solution can continue at 26 Gbps switching capacity provided by the remaining device until the problem is resolved. Using link aggregation and TPX3103 advanced traffic management it is thus possible to ensure that priority services are not disrupted by such failures.

Functional Description

The block diagram below shows the most important internal functional blocks of TPX3103 along with the necessary ancillary components. Packets are received from left (ingress) and are processed from left to right through the TPX3103 and are finally transmitted from the port module to the right (egress).

TPX3103 | 52 Gbps Transport Switch | Carrier Ethernet Switches

Specifications

Capacity

- 20-26 Gbps bandwidth, 24.5-32 Mpps packet rate for single TPX3103
- 40-52 Gbps bandwidth, 49-64 Mpps packet rate for dual TPX3103
- Switching between 256 logical ports
- Jumbo frames up to 10Kbyte

L2/VLAN and L2/VSI switching

- L2 switching using VLAN or Virtual Switch Instances (VSI)
- 8K Virtual Switch Instances
- Up to 576K (packet flows, CoS)
- Up to 128K L2 addresses
- Link aggregation with 8K groups
- Wire speed L2 multicast handling

MPLS Packet Switching

- Three MPLS push/pops per packet
- 8K MPLS lookup entries provided
- Wire speed MPLS multicast handling

Provider Backbone Transport (PBT)

- MAC-in-MAC based on IEEE 802.1ah and 802.1Qay
- Up to 2048 PBT tunnels (e.g. 1024 working and 1024 protection tunnels)
- Up to 1024 I-TAG service entries

OAM support

- ETH OAM based on Y.1731, 802.1ag
- MPLS OAM based G.8114, Y.1711
- 3.3msec OAM packets interval
- HW based check of CCM / CV for up to 1K remote MEPs
- HW based Loss and Delay perform
- HW based protection switching

Policing and Traffic Management

- Up to 64K policing buckets, both single and dual leaky bucket modes
- Ingress or egress policing
- Output queue system with 8 queues for each of the 256 logical ports
- WRED support with 4 levels
- Strict priority weighted round robin and guaranteed bandwidth scheduling
- Leaky bucket output shaping per output queue and per logical port

Traffic Statistics

- Ingress octet and packet counts for up to two VLAN-, MPLS- and/or PBT tunnel lookups
- Egress octet or packet counts for each Tx update entry
- Police octet or packet counts per color for each police bucket entry

The Port module is responsible for combining the incoming packet flows from the different physical ports to one flow, which then is forwarded to the packet processor. From the packet processor's perspective all so-called logical ports, whether physical Ethernet ports, channels on the SPI-4.2 packet interface or th CPU ports, look the same and get the same treatment. The port module supports up to 256 logical ports.

The TPX3103 has a packet processor for handling the headers of the packets and a traffic manager for storage and scheduling of packets.

The packet processor looks at the header of the packet and uses this information to determine how to forward, police and en-queu the packet.

The traffic manager stores incoming packets i external packet buffer memory and determines in which order to send packets to the different output ports. Replication of packets in connection with multicasting is also done by the traffic manager.

The OAM block handles special Ethernet and MPLS OAM packets like Connectivity Check Messages (CCM). The OAM block performs certain timing critical function internally (such as periodically transmission of CCM with down to 3.3 msec intervals) while other non time critical functions are performed in conjunction with the CPU (software).

The CPU interface block is handling DMA access into the CPU memory (for packets like BPDU's and OAM packets) as well as register read/write operations into the TPX3103.

The C2C controller handles the internal communication between two TPX3103 devices in case of dual chip operation.

TPX3103 has the unique capability of operating in a dual-chip mode, in which the solution operates as a single 40-52G switch with switching capability from any-to-any port. Remark, in this mode all features, be it link aggregation, policing, traffic management etc., work across interfaces on both devices just as if it was one single device and full connectivity between all parts is ensured.

Only one CPU needs to be connected to the two TPX3103's and this CPU has access to any register and resource in the combined device. It is also viable to connect a CPU to both of the TPX3103 devices.

The dual chip of operation enables implementation of equipment failure protection with graceful degradation of the capacity in case of a removal of a module.

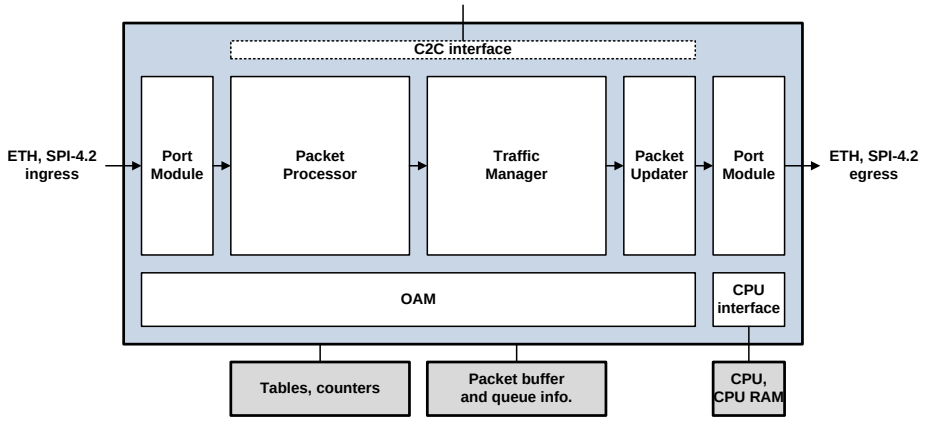
Driver Software

API software is provided for easy integration with and maintenance of application layer software. The software can be compiled to any OS.

Reference Platform

The Longmorn reference platform implements an entire stand-alone transport switch consisting of the TPX3103 transport switch with GE and 10GE interfaces plus a SPI-4.2 interface to a TPX192 EoS mapper.

Longmorn comes complete with application layer SW, MIBs and SNMP interface and a PC based element manager application.



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