White Paper

Enabling Improved Image Format Conversion with FPGAs

FPGAs offer a competitive alternative to format-conversion ASSPs, which do not focus on the broadcast market. Altera's video framework makes it easy to build cost-effective customizable format conversion functions in FPGAs with time-to-market advantages.

Introduction

Broadcast infrastructure systems—such as servers, switchers, head-end encoders, and specialty studio displays—support a multitude of input image formats, and commonly require images to be converted to high definition (HD) or a different resolution before they can be stored, encoded, or displayed. While specialized ASSPs have addressed this market with varying degrees of success, the challenge has been to address the extremely diverse and application-specific requirements of broadcast equipment vendors with a single chip. For example, overall delay is very important in switcher applications, latency is a key factor for displays and video-conferencing systems, and image quality is a high priority for post-production equipment. In addition to these specific application needs, the devices must also support a multitude of frame rates, resolutions, and formats.

Furthermore, because the design cycles for this type of equipment are relatively short, designers do not have the luxury of waiting for the long respin cycles of ASSPs when requirements change. As a result, many ASSP vendors with excellent video technologies have failed to get market traction in this space and have been absorbed by consumer electronics chip companies, providing video processing expertise to consumer-specific markets. For example, Gennum (VXP), Genesis, Silicon Optix, and Let It Wave have been acquired by Sigma Designs, ST Micro, IDT, and Zoran, respectively.

During this ASSP industry consolidation and retargeting, the video processing capability in FPGAs has increased, creating an ideal platform for custom image format conversion applications. To support the accelerating image format conversion to FPGAs, Altera has developed a 1080p video design framework, described in this white paper, that makes it easy for system designers to develop a custom image format conversion signal chain. The image format conversion reference design discussed can be used as a starting point and modified to develop custom video processing applications. This design is hardware-verified and is available to qualified customers.

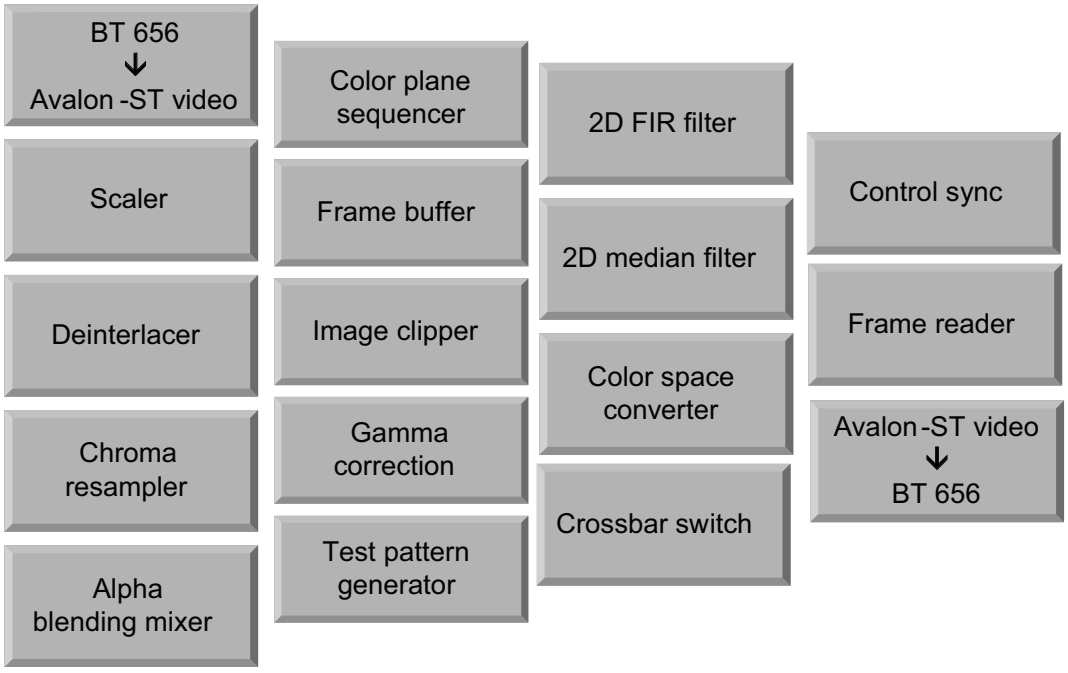
Video Design Framework

The Altera® video design framework is a collection of tools and building-block video functions designed to speed the development and implementation of your custom image format conversion design. It consists of the following components:

- Building-block video intellectual property (IP) cores
- Format conversion reference designs that showcase FPGA capabilities and provide a starting point for design
- Open-source, low-overhead video interface that allows you to mix-and-match custom or off-the shelf IP blocks
- System-level design tools for integrating processors and memory subsystems
- Various video development kits for rapid design prototyping

Altera has developed a variety of building blocks for video processing, called the Video and Image Processing (VIP) Suite (see Figure 1). Of the many functions available in this suite, the scaling and deinterlacing functions are implemented extensively in image format conversion designs. Altera's VIP Suite features both a sophisticated polyphase scaling engine and a deinterlacing function that can be configured to implement motion-adaptive deinterlacing. Other functions such as chroma resampling, color space conversion and frame rate conversion—all of which are part of the VIP Suite—are also used frequently. These video functions can be combined together to create any custom image format conversion design.

Figure 1. Video Image Processing (VIP) Suite



This video design framework provides the functionality previously supplied by ASSPs, with the added advantages of the ability to customize and update your design (see Table 1).

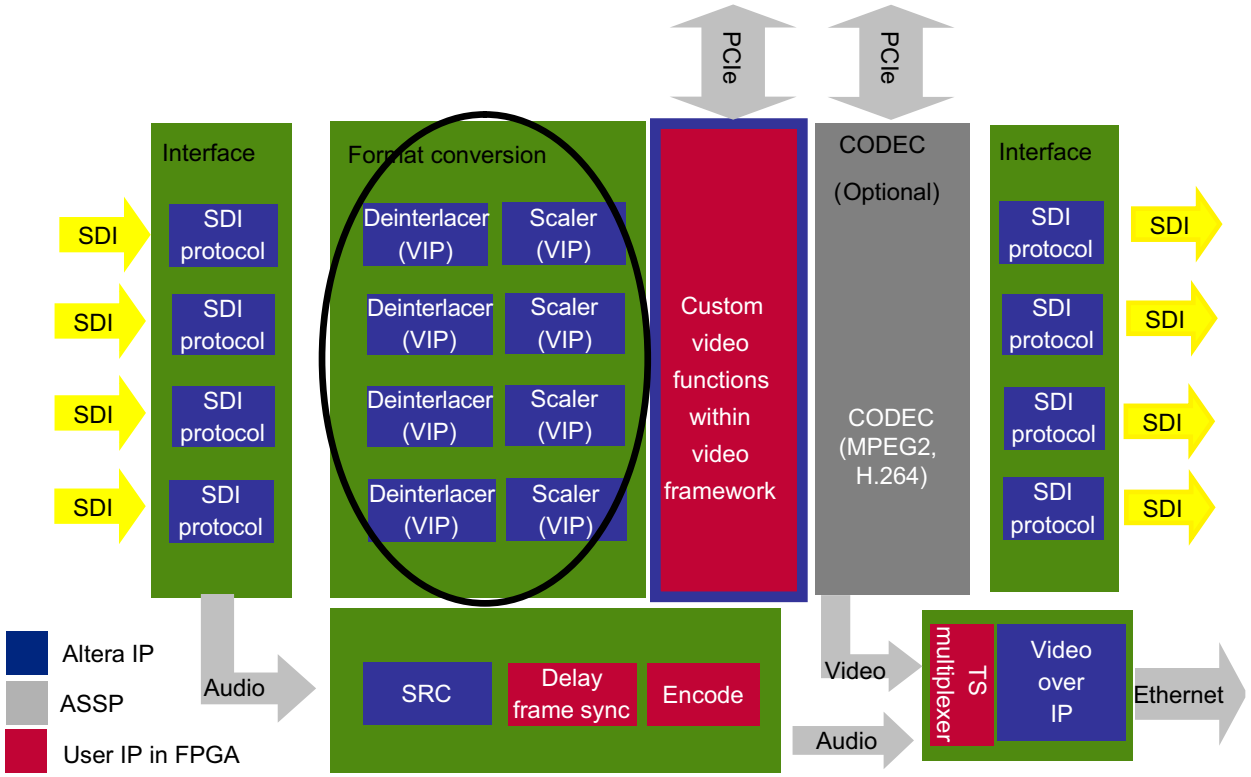
Table 1. Altera Video Design Framework Compared to Broadcast ASSPs

Video Functions	Altera Video Design Framework	Broadcast ASSPs
Motion-adaptive deinterlacing	✓	✓
Polyphase scaling	✓	✓
Video mixing	✓	✓
Building block IP—chroma resampler, color space converter, etc.	✓	✓
Genlock support	✓	✓
Noise reduction	✓ (from Algolith)	✓
DDR2/3 memory controller *(2)*	✓ (Unified memory architecture using multiport front-end arbiter)	✓ (No memory sharing and limited support for external memory types)
Integrated SERDES for SDI and PCIe Gen1 and Gen2	✓	
On-chip processor	✓	✓
Update design using software	✓	
Update design using IP parameters in hardware	✓	
Add custom hardware to the design	✓	
Switch function	✓	
AFD support	✓	

Image Format Conversion Designs

Almost all studio systems—including servers, switchers, head-end encoders, and boards such as the one shown in Figure 2—use custom image-format conversion, an application ideal for programmable FPGA architecture.

Figure 2. Functional Block Diagram of a Typical Studio System



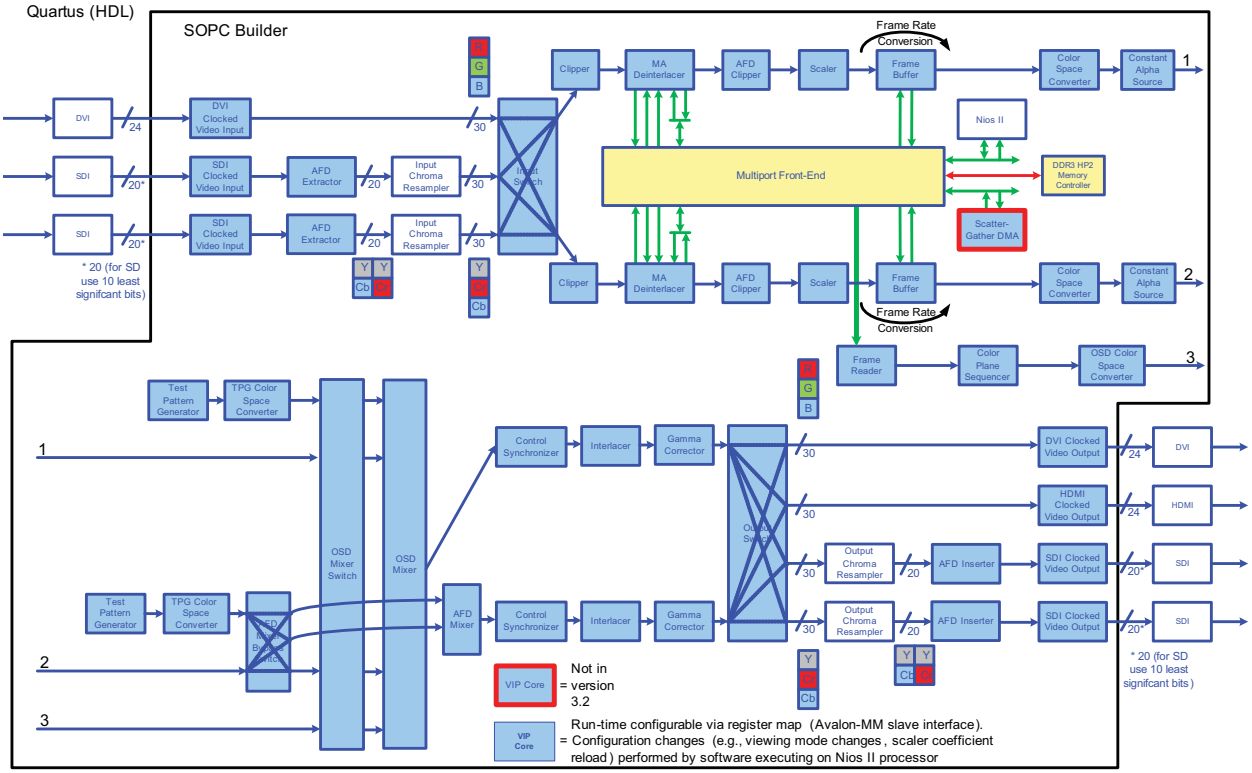
The Altera video series of reference designs deliver high-quality up-, down-, and crossconversion of standard-definition (SD), HD, and 3-Gbps video streams in interlaced or progressive format. The reference designs are highly software and hardware configurable, enabling rapid system configuration and design.

The V1 reference design features two SDI inputs (SD, HD, or 3G) to one DVI output (480p60, 720p60, or 1080p60), with one high-quality channel (MA deinterlacer, 12x12 tap scaler) and one lower quality channel (weave deinterlacer, nearest neighbor scaler).

The V2 reference design features two fully independent high-quality SDI channels capable of coping with resolutions up to 1080p60.

Altera's latest reference design, UDX3 (up-/down-/crossconversion), combines the functionality of V1 and V2. UDX3 is configurable (in software) to support multiview (with on-screen display (OSD)) or up-/down-/crossconversion, and supports two fully independent, high-quality SDI or DVI channels capable of coping with resolutions up to 1080p60. As shown in Figure 3, the design can be demonstrated using a Stratix® IV GX PCI Express (PCIe) board, a HSMC dual 3G SDI Rx/Tx daughtercard and a Bitec HSMC DVI I/O daughtercard.

Figure 3. Altera's Image Format Conversion Design Built With the Video Design Framework



The UDX3 reference design includes the following features:

- Two run-time selectable inputs from:
  - Two triple-rate SDI inputs—SD, HD or 3G, interlaced or progressive, any resolution and frame rate up to 1080p60
  - One DVI input—Interlaced or progressive, any resolution and frame rate up to 1080p60
- Two run-time selectable outputs from:
  - Two triple-rate SDI outputs—SD, HD, or 3G, interlaced or progressive, any resolution and frame rate up to 1080p60
  - One HDMI output—interlaced or progressive, any resolution and frame rate up to 1080p60
  - One DVI output—interlaced or progressive, any resolution and frame rate up to 1080p60
- Two high-quality up-/down-/crossconversion video-processing paths with:
  - Motion-adaptive deinterlacer
  - Scaler (6x6 tap)
  - Interlacer
  - Two field latency for interlaced input
  - Two frame latency for progressive input (one frame in deinterlacer, one frame in frame buffer)
  - Run-time controllable frame rate conversion
  - Genlock
- Mixer present on one video processing path—Allows multiview with OSD
  - New frame-reader block to allow streaming of OSD from a frame buffer in memory
- Software controlled—No recompile needed when changing input or output format, resolution, or frame rate
  - Software loads from flash memory along with SOF and OSD logos
- Active format descriptor (AFD) extraction and insertion—Dynamic clipping, scaling, and padding to support 4:3-to-16:9 format conversion based on an AFD code
- Unified memory architecture—Uses a multiport front-end arbiter to allow CPU, OSD, and video processing to use one 64-bit DDR3 memory (V1 and V2 use two separate memories)
- New switch block allows run-time reconfiguring of video processing path

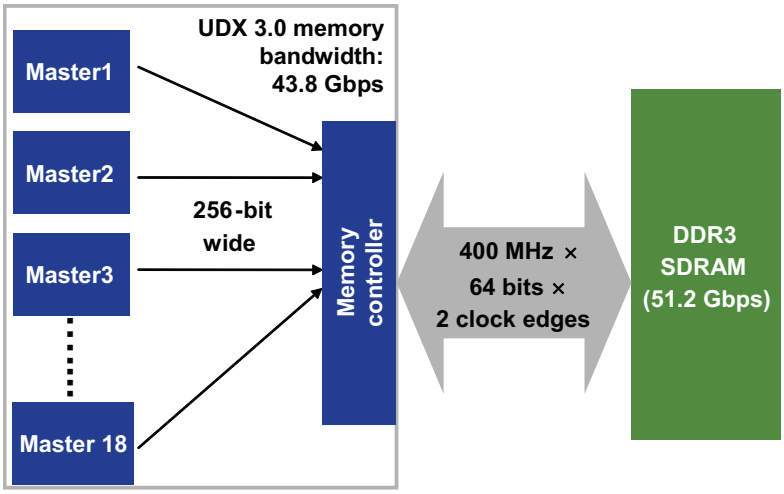
For more information, request the UDX3 reference design from a local Altera sales representative and refer to the reference design documentation.

Multiport Front Memory Controller Allows Unified Memory Architecture

The format conversion functions typically are memory hungry because they must cache multiple frames of video for manipulation. At the same time, the data per frame significantly increases as the data moves from SD to HD to full HD, hence the need for an efficient memory arbiter and controller to get the most from the external memory available in the system. Having an efficient memory controller with high performance interfaces can reduce the external memory requirements costs and hence the system costs.

The UDX reference design accesses Altera's DDR3 SDRAM High-Performance Memory Controller MegaCore function for external memory access. Figure 4 shows the external memory bandwidth requirements of the UDX reference design. There are two channels of video in the design and MA deinterlacers (five masters), frame buffers (two masters), a Nios® II embedded processor (two masters), and DMA controller (two masters). With two channels of video this results in an 18-master system.

Figure 4. External Memory Bandwidth Requirements of the UDX3 Reference Design



As shown in Table 2, the total external bandwidth required is 43.8 Gbps. The Stratix IV GX board 64-bit DDR3 SDRAM provides a maximum theoretical bandwidth of

$$400 \text{ MHz} \times 64 \text{ bits} \times 2 \text{ clock edges} = 51.2 \text{ Gbps}$$

which results in a memory access efficiency requirement of approximately 86%. By increasing the frame rate of the OSD, the maximum memory access efficiency that can be achieved is >90%.

Table 2. UDX Reference Design System External Memory Bandwidth Breakdown

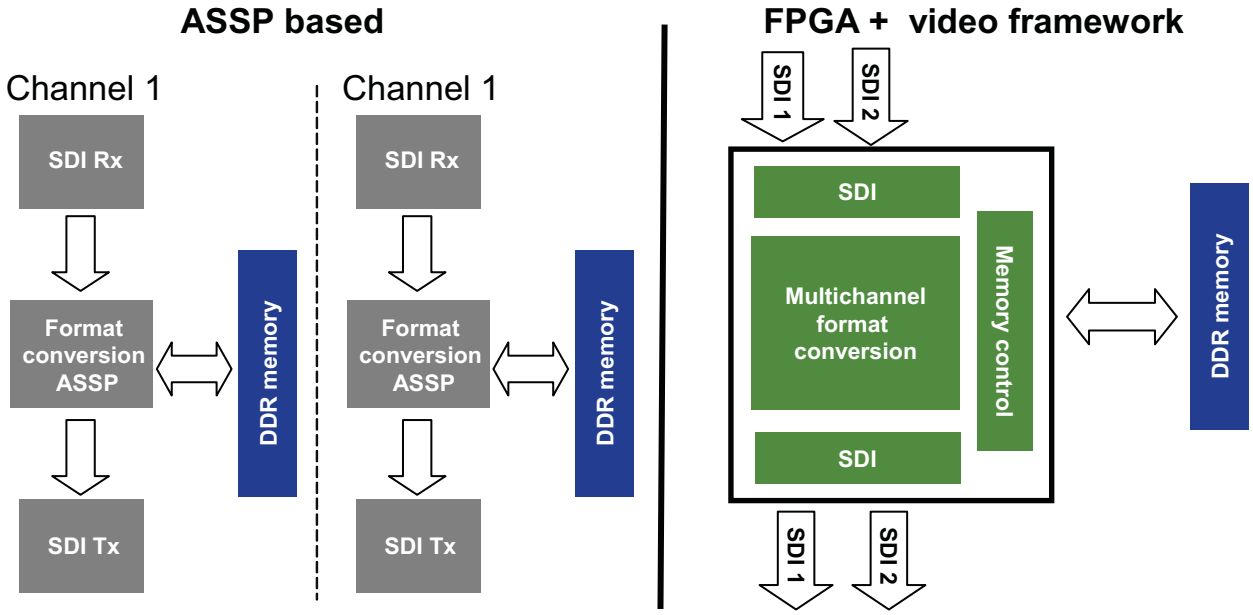
Function	Bandwidth
MA deinterlacer (channel 1)	11.228 Gbps
MA deinterlacer (channel 2)	11.228 Gbps
Frame buffer (channel 1)	7.963 Gbps
Frame buffer (channel 2)	7.963 Gbps
OSD frame reader	3.981 Gbps
OSD DMA controller	0.926 Gbps
Nios II embedded processor	0.5 Gbps
Total	**43.789 Gbps**

To achieve the required memory access efficiency of ≥ 90 %, a multiport front-end arbiter is used to access the DDR3 high-performance memory controller. The multiport front-end arbiter sits between the 18 masters and the single slave of the memory controller, and arbitrates between the master accesses. By grouping the 18 masters sensibly, using the default round-robin arbitration scheme of SOPC Builder, the number of ports on the multiport front can be reduced to 15.

For further details on the multiport front-end memory subsystem, request the UDX3 reference design from a local Altera sales representative and refer to the reference design documentation.

As shown in Figure 5 (left), ASSPs have inherent disadvantages for broadcast application, because they typically are designed for single-channel, high-volume consumer applications with very limited external memory support. They usually do not scale well; as more channels lead to more components on the board, the board quickly gets ugly. In addition, systems designers are forced to use very limited memory types, such DDR1 or DDR2, which are seldom the latest or the most-cost effective. Lastly, as the memory cannot be shared between channels, it can result in a very inefficient and costly memory subsystem.

Figure 5. Multichannel Format Conversion



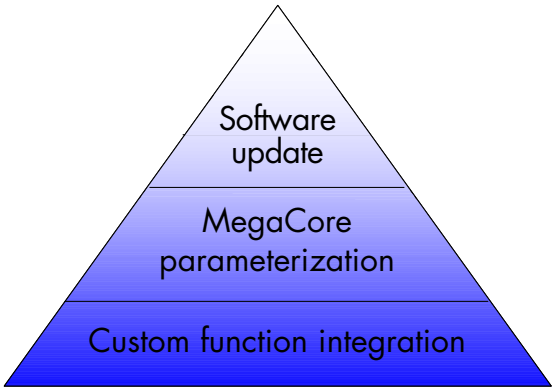
In contrast, FPGAs typically support various external memory types such as DDR, DDR2, DDR3, and RLDRAM, and use the video framework and peripherals such as a multiport front-end memory controller. The format conversion (Figure 5 (right)) can be easily scaled and customized for various applications.

There are also various other features specific to broadcast that ASSPs do not support, such as extracting and embedding data in vertical and horizontal blanking intervals such as audio and active format descriptors. Studios have been demanding support for AFD from equipment manufactures because it significantly enhances the end user's viewing experience and lowers cost by removing the need for parallel workflows and broadcasts for SD and HD. Altera provides AFD and audio embed and extract functions, and allows users to easily integrate these functions in their format conversion system

Customizing Your Image Format Conversion Designs

Altera's video framework is designed from the ground up to enable user customization. The framework allows three levels of customization with various degrees of flexibility, as illustrated in Figure 6. This level of customization is unprecedented in the FPGA domain and is not possible when designing with ASSPs.

Figure 6. Different Levels of Customization Available With the Altera Video Framework



Designs developed using Altera's video framework can be updated in real time using two innovative technologies:

- *Packet format streaming interface*—Designed to transfer both video and control packets from one functional block to another
- *Algorithmic function block configuration*—Can be configured as a memory-mapped component with functionality that can be updated in real time by writing to the right control register

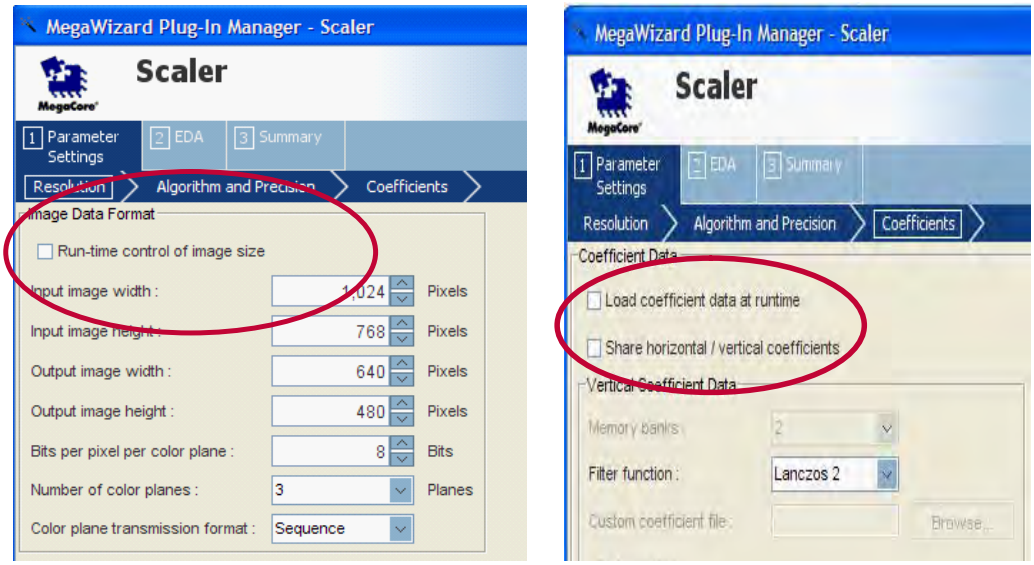
The Avalon® Streaming (Avalon-ST) video interface, Altera's new low-overhead protocol, offers a packet-oriented method to send video and control data. Control packets are used to send dynamic parameters that describe the format of the video frames traveling on the stream. These parameters apply to the next video data packet to arrive, or when specified at compile time, they apply to the first video data packet received after a reset. (Table 3 shows how the control data packets provide information about the next frame.) Embedding control data packets in a stream of video data allows a video processing pipeline to reconfigure itself to new data as that data arrives.

Table 3. Control Packets Allow for Dynamic Updates of the Video Stream Format

Control Parameters			Next Frame
Frame Width	**Frame Height**	**Interlacing**	
640	480	Progressive	• Progressive • Frame size 640x480 pixels
1920	540	Field 0, Sync 1	• Interlaced • First field to arrive is f0 • Sync on f1 • Size 1920x540 field/1920x1080 frame
720	288	Field 1, Sync 1	• Interlaced • First field to arrive is f1 • Sync on f1 (must have buffered f0) • Size 1920x540 field/1920x1080 frame

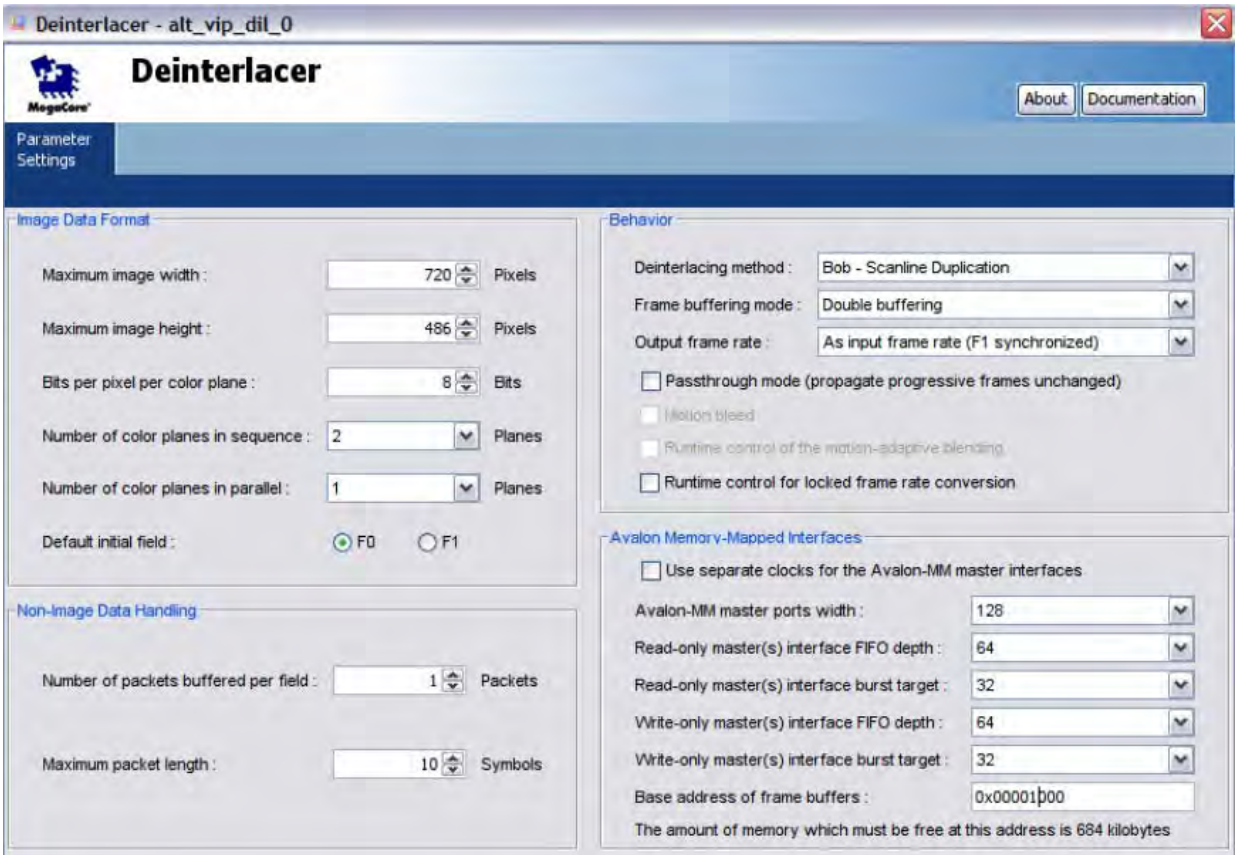
In addition to enabling run-time updates via the streaming interface, most video function blocks developed by Altera feature a run-time update capability. This means that these blocks use a memory-mapped slave interface that allows a state machine or an on-chip processor to update their behavior. Each slave interface provides access to a set of control registers. These control registers can be updated while the function is running using, for example, an on-chip processor. At the beginning of a new frame, the updated control data is loaded in the IP functional block. This process allows you to update image sizes and scaling coefficients, and to change the scaling ratio—even from downscaling to upscaling—while the system is running. Figure 7 shows how run-time control is enabled for the polyphase scaling engine available in the Altera video framework.

Figure 7. Updating the Scaling Function



To further customize your design, you can change parameters for the MegaCore functions. All video functions developed by Altera are completely parameterizable. As shown in Figure 8, the deinterlacer function allows you to select not only the deinterlacing algorithm, but also options such as default field, pass-through mode, the number of frames buffered in external memory, output frame rate, and control for motion bleed.

Figure 8. Completely Parameterizable Hardware Function Blocks

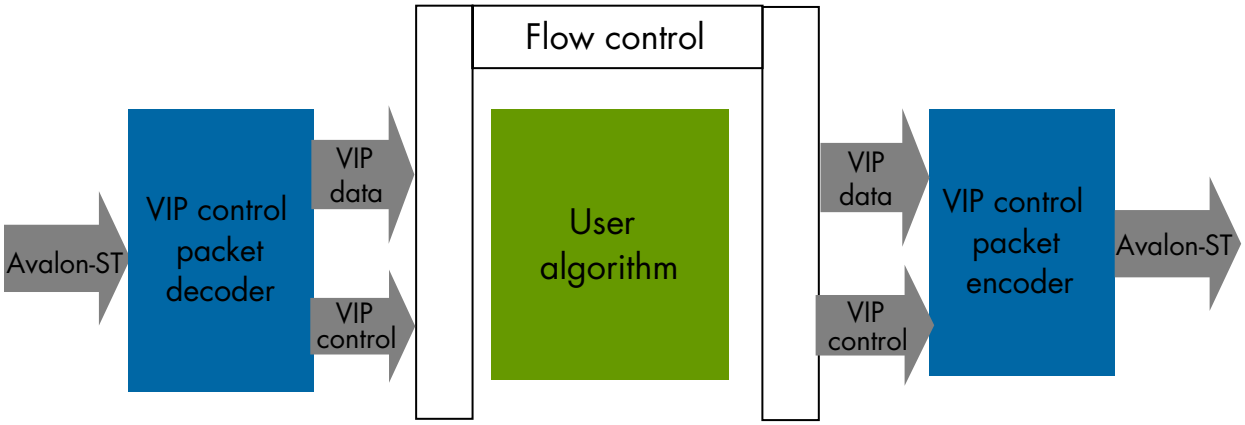


The open plug-and-play specifications of the Avalon-ST and Avalon Memory-Mapped (Avalon-MM) interface standards mean that you can start with one of the image format conversion designs and replace an Altera block with your own custom block. Many designers have custom algorithms that are optimized for their application or that are constantly evolving. To enable easy integration of custom algorithms, Altera provides an HDL template with an Avalon-ST interface wrapper. This wrapper consists of the following modules:

- *VIP Control Packet Decoder*—Decodes the VIP control packets from the data stream and sends the decoded data (width, height, interlaced) as separate signals to the algorithm.
- *VIP Control Packet Encoder*—Encodes the VIP control packets based on the received width, height, and interlaced information and inserts them into the data stream.
- *VIP Flow Control Wrapper*—Wraps around the user algorithm and deals with the flow control conversion from Avalon-ST to and from a simple read/write interface.
- *User algorithm core*—The HDL template comes with a simple design example in the user algorithm module. This block can be replaced with your own algorithm.

A high-level block diagram of the HDL template is shown in Figure 9.

Figure 9. Avalon Streaming HDL Template



Algolith, Altera's IP partner and an expert in video IP, has taken advantage of the HDL template to offer their cores for evaluation. Starting with the Altera reference design for image format conversion, Algolith replaced the Altera's deinterlacer function with their proprietary motion-adaptive deinterlacer and made it available for users to evaluate in hardware. Similarly Algolith has built reference designs using the Altera video design framework that enables customers to evaluate their noise-reduction IP.

Conclusion

Altera's video design framework provides all the key functionality required by broadcast infrastructure systems to implement image format conversion. With the Altera video design framework and the image format conversion reference design, FPGA designers now have access to feature sets previously only found in broadcast ASSPs, with the added advantage of flexibility and hardware customization.

Further Information

- Request the UDX3 reference design froma local Altera sales representative:
  www.altera.com/corporate/contact/con-index.html
- *AN 581: High Definition (HD) Video Reference Design (V2)*:
  www.altera.com/literature/an/an581.pdf
- *Video and Image Processing Suite User Guide*:
  www.altera.com/literature/ug/ug_vip.pdf
- Format Conversion Reference Design (UDX3):
  www.altera.com/support/refdesigns/sys-sol/broadcast/ref-format-conversion-udx3.html
- Algolith Inc
  www.algolith.com
- *AN 559: High-Definition (HD) Video Reference Design:*
  www.altera.com/literature/an/an559.pdf

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