White Paper

Video Processing on FPGAs for Military Electro-Optical/Infrared Applications

This white paper explores Altera's low-power FPGA platform and the video design solutions that address the military's complex, power-budget-constrained EO/IR design challenges and significantly increase designer productivity.

Introduction

Many of today's electro-optical/infrared (EO/IR) systems require high-complexity, real-time video processing within a constrained power budget. The latest low-power, low-cost FPGA families—with their inherently parallel digital signal processing (DSP) blocks, an abundance of embedded memory blocks, large number of registers, and high-speed memory interfaces—are ideal for developing the next generation of night vision, thermal imaging, head-mounted and avionics displays, and other such EO/IR systems. However, video processing on FPGAs also has challenges, such as implementing efficient external-frame buffer interfaces, interfacing different video function blocks, integrating signal processing to the on-chip processor, as well as the lengthy debug and prototyping cycles.

Using FPGAs for Video Processing

Today's low-cost and low-power FPGAs feature a host of silicon features that enable high-performance signal processing, including abundant multipliers, fast fabric performance, and large amounts of on-chip memory. Such FPGAs are well suited to implement low-power and high-quality image processing, which are required for new EO/IR systems. Altera's Cyclone® III FPGAs are a good example of an FPGA platform that combines the multiplier, memory, and logic resources required for complex video and image processing with the frugal power consumption that is important for many EO/IR systems. Table 1 shows some of the silicon features that enable high-performance video processing.

Table 1. Cyclone III Silicon Features Required for High-Performance Video Processing

Features	Benefits
18x18 multipliers	Up to 288 (maximum performance of 260 MHz)
Memory	Up to 432 blocks of 9K RAM, over 4 Mbits of on-chip RAM
Logic	Up to 120K logic elements (LEs)

Built on the TSMC 65-nm low-power process technology, Cyclone III FPGAs have additional silicon and software optimizations to offer extremely low power consumption. While power consumption is very design- and f_{MAX}-dependant, the typical power consumption of a mid-range Cyclone III FPGA (with over 50,000 LEs) is lower than 1W, as shown in Figure 1. The static power consumption is less than one-tenth of this number (i.e., less than 100 mW).

Figure 1. Typical Power Consumed by Cyclone III FPGAs for a Range of Density and Performance

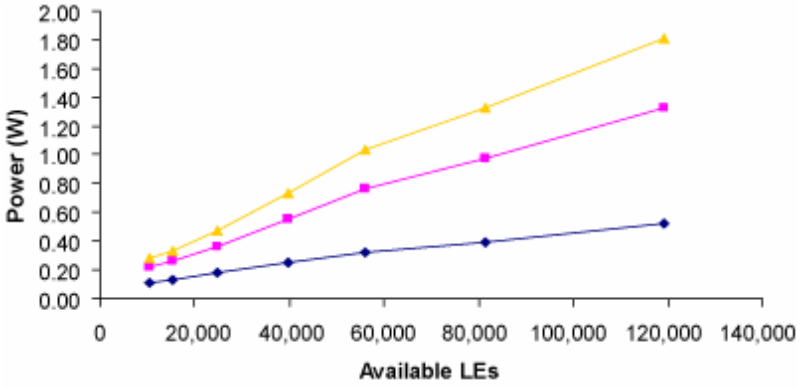
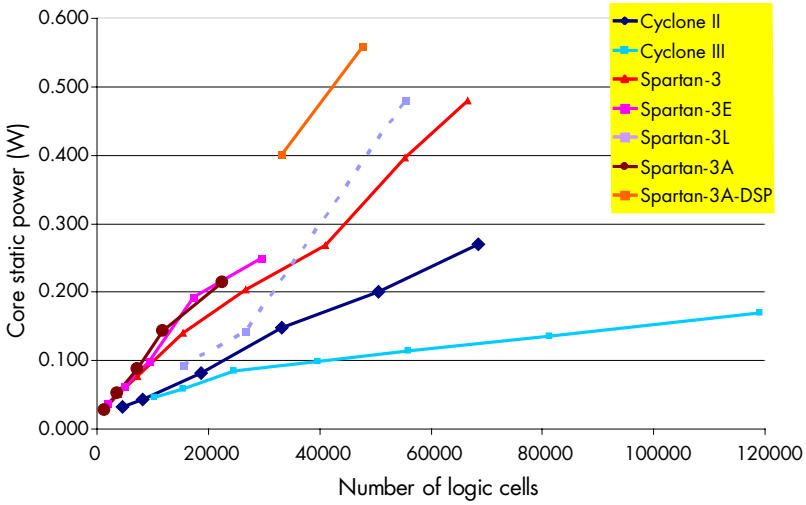


Figure 2 graphs the core static power consumption for various low-cost FPGAs.

Figure 2. Comparison of Low-Cost FPGA Static Power Consumption



Notes:

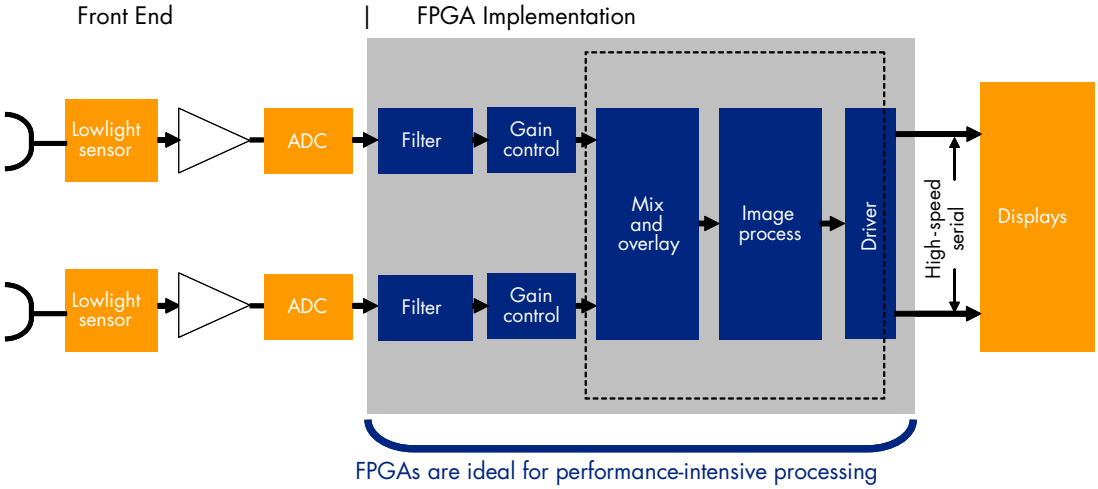
(1) Tj = 85°C (Tj could not be set for 1000L and 2000L)

(2) Spartan-3 and Spartan-3L results from Xilinx Web Power, Spartan-3E results from XPE

Accelerating FPGA Video Designs for EO/IR Systems

A typical EO/IR system has sensor processing at the front end and complex image processing at the back end, as shown in Figure 3.

Figure 3. Block Diagram of a Generic EO/IR Sensor-Processing Signal Chain



To implement the back-end processing in an FPGA, the designer must create:

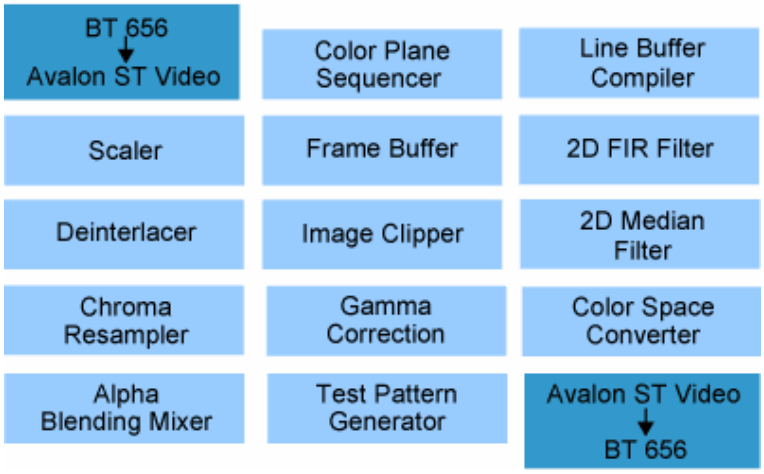
- Video blocks to implement specific functions, including image processing, such as scaling and color space conversion
- Streaming interface to connect different blocks
- Embedded processors
- Other functions, such as external DDR memory controllers
- System-level design tool to tie all functions together

The Altera® video design framework brings together all the software tools and building block intellectual property (IP) to jumpstart video design development, thereby significantly improving productivity when developing video and image processing applications.

Building Block Video Functionality

Altera's Video and Image Processing (VIP) Suite of IP cores (Figure 4)provides functionality ranging in complexity from a color space converter to a polyphase scaler and motion-adaptive de-interlacer. All of these blocks have standard video interfaces that allow for easy plug-and-play capability, work with the standard BT-656 video format, and allow for rapid prototyping of the system. Having this library of pre-tested and verified common video functions available allows the designer to focus on proprietary functions.

Figure 4. VIP Suite of IP Cores



Altera and partner companies have built a collection of reference designs using the VIP Suite and some custom cores to provide a starting point for designs. For example, the DSP Video Processing Reference Design, which is optimized for the low-power Cyclone III platform, is available for immediate download..

Open Interface Standard

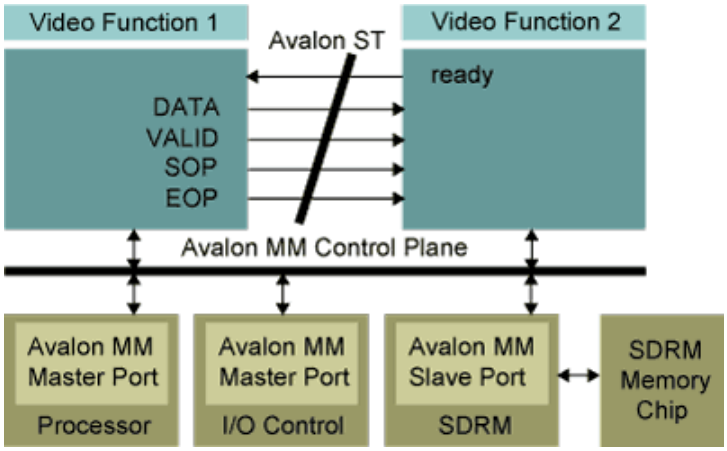
A video signal chain is created by connecting multiple blocks with differing interface characteristics, each built by a different team. A great deal of effort is expended in getting the interfaces to talk with each other in a coherent manner. In addition, some functions may need to be controlled by the on-chip processor. The interface between the processor and a given function often is custom designed and may be different for each function block. The design and debug of such an interface is outside the scope of the key value-add algorithmic designs developed by the video system designers.

What is needed is a standard interface protocol that can be used to connect the different blocks and control the functional block operation using the on-chip processor. The key characteristics of such an interface are that it should be open (non-proprietary) and have a low overhead (in terms of logic and performance). One such standard is the Altera's Avalon® Streaming (Avalon-ST) video protocol, which is a packet-oriented method of sending video and control data from one video-processing block to another. The key feature of this protocol is that it is open and the specification is freely downloadable via the Internet. While using this specification does not in any way commit the designer to using Altera FPGAs, all Altera VIP Suite and video reference designs use this interface.

The Avalon-ST video protocol defines how any type of video data can be broken into packets of video data and packets of control data. A video data packet has two sets of parameters: static parameters that cannot vary at run time, such as bits per color plane and sequence of the color plane, and dynamic parameters that can be changed at run time, such as frame size, field size, and interlace format.

Often it is necessary to control the behavior of a video function by using control logic such as an embedded processor. Altera has defined a standard slave interface—Avalon Memory Mapped (Avalon-MM)—that allows a video block and an on-chip processor to communicate. This interface allows two-way communication where the processor can program the video function, and the function can raise interrupts to notify the processor of exceptional events. Figure 5 shows how different video functions can be connected to each other and to an embedded processor using this protocol.

Figure 5. Video System Using Both Avalon-ST and Avalon-MM Interfaces



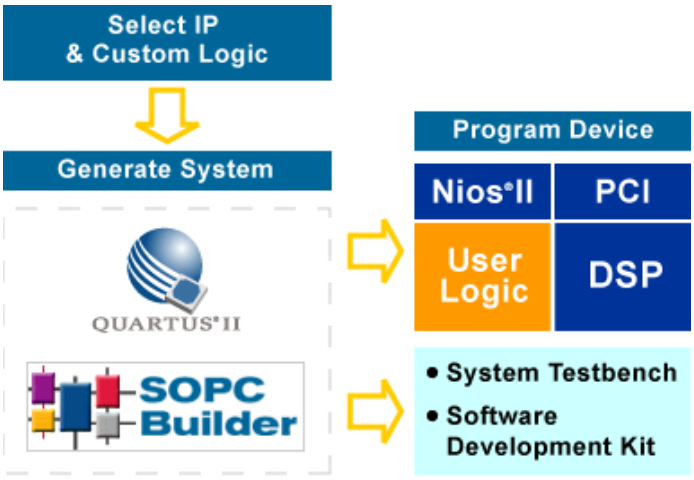
More information on the Avalon-ST and Avalon-MM protocol is available in the "Interfaces" section of the *Video and Image Processing Suite User Guide*.

System-Level Design Tools

Video systems generally include an embedded processor and a memory subsystem to manage the video frames in the external memory. Connecting these elements with the video signal chain requires processor instantiation, DDR memory interface, and system-arbitration logic design.

Altera's SOPC Builder tool greatly simplifies embedded system design with its library of elements such as soft processors (Nios® II embedded processor), interfaces, memory, bridge, and DSP IP cores. It also features a connectivity GUI and generator to wire up arbitrated and streaming bus systems automatically. Figure 6 shows a design flow where SOPC Builder is used to generate a system on the FPGA.

Figure 6. Design Flow Using SOPC Builder to Generate a System



Prototyping the Design

Video is very time consuming to simulate in software, so debug and verification are performed in hardware with actual video signals and displays. Different video applications use different physical interfaces (i.e., composite, DVI, SDI, HDMI, etc.) to transport video in and out of the chip.

Altera and partners offer video development kits for the Cyclone III platform that support different video I/O formats, including composite, S-video, DVI, analog VGA, and SDI. One such is Bitec Inc's complete video development kit based on the Cyclone III EP3C120 FPGA. This video kit comes with a complete set of daughtercards for interfacing with various video sources and displays, and a suite of reference designs built using the Altera video framework that will help designers start developing EO/IR systems.

Conclusion

As newer military EO/IR systems demand performance video processing combined with low-power consumption, FPGAs are becoming the implementation platform of choice. FPGA vendors have responded by developing a suite of IP, design tools, and development kits that help rapid design, development, and prototyping of such systems. Altera, in particular, has a combination of IP, reference designs, development kits, and system-level design tools that come together in a video design framework to significantly increase productivity and shorten time to market.

Further Information

- IP MegaStore™: www.altera.com/products/ip/dsp/ipm-index.jsp
- Altera's Video and Image Processing MegaCore® Functions: www.altera.com/products/ip/dsp/image_video_processing/m-alt-vipsuite.html
- DSP Video Processing Reference Design: www.altera.com/technology/dsp/ref_design/dsp-video.html
- *Video and Image Processing Suite User Guide*: www.altera.com/literature/ug/ug_vip.pdf
- Bitec's Cyclone III Video Development Kit: www.bitec.ltd.uk/ciii_video_dev_kit.html

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