

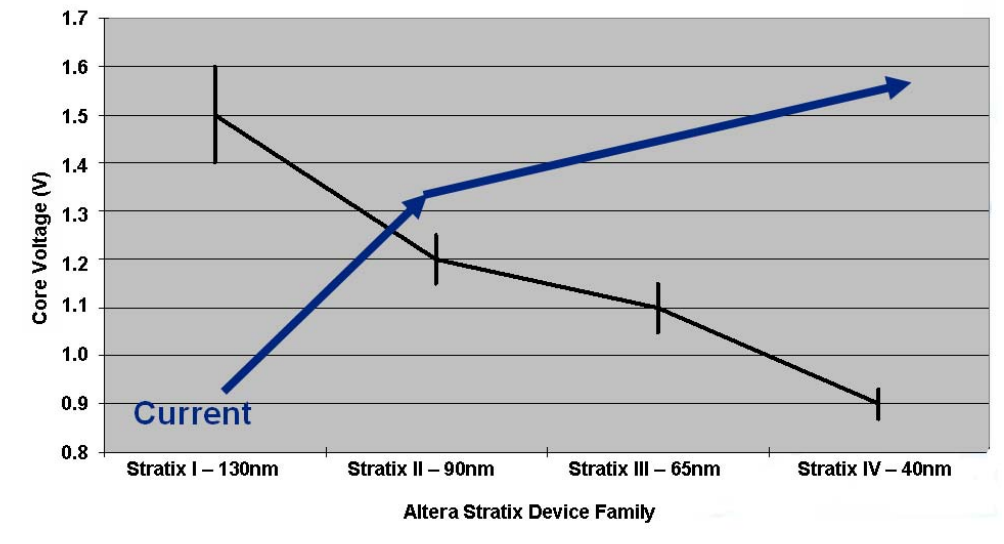
This application note provides an overview of the various components that make up a power delivery network. It also describes the role of the PCB cutoff frequency ($F_{EFFECTIVE}$) in designing an efficient system power delivery solution. The application note also describes the PCB design trade-offs and offers high-level design methodology that you can follow when combining multiple power rails on the board.

Introduction

Supply voltage decreases as you move to smaller process geometries. This reduction in voltage helps to reduce dynamic power consumption. Taking advantage of process enhancements, semiconductor vendors are increasing device densities from one product generation to the next. This causes an increase in the total current demand. This, in turn, creates challenges from a power delivery standpoint because designers have to meet increasingly stringent noise requirements for proper device operation.

Figure 1 shows an example of core supply voltage reduction from 1.5 V to 0.9 V as you move from a 130 nm Stratix® I device family to a 40 nm Stratix IV device family. The total current increased from the Stratix I to the Stratix IV device due to the increase in device density. The maximum number of logic elements (LEs) on a Stratix I device family is 79 K and the maximum number of LEs on a Stratix IV device family is 681 K. This is an increase of ~8.6.

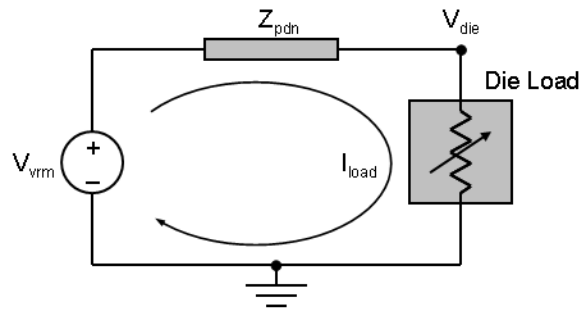
Figure 1. Core Voltage Reduction Due to Process Scaling



Power Delivery Network

The goal of a power delivery network is to provide clean power and reference voltage to the active devices on the die. Similar to an ASIC, field programmable gate array (FPGA) devices need clean power to meet their maximum operating frequency (f_{MAX}) specifications. A simple representation of a system power delivery network is shown in Figure 2.

Figure 2. System Power Delivery Network

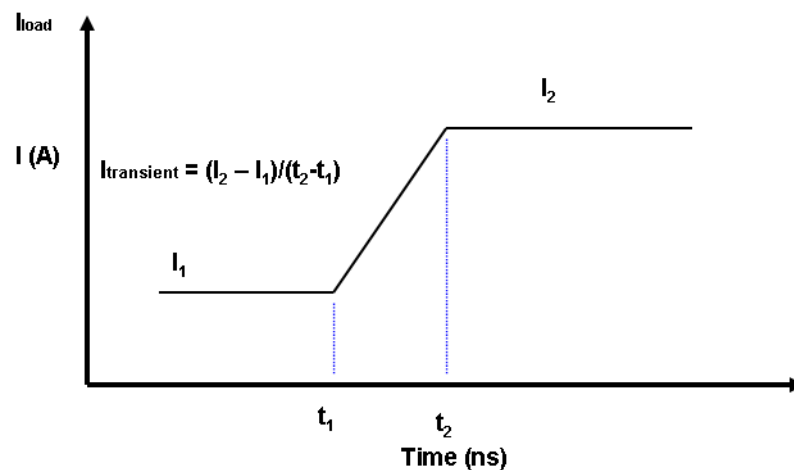


A power delivery network has an impedance (Z_{PDN}) associated with the path from a voltage regulator module (VRM) to the FPGA. The magnitude of noise (voltage ripple) seen on a given power rail is proportional to the impedance (Z_{PDN}) and the transient current ($I_{TRANSIENT}$) draw associated with that rail. Figure 3 shows the schematic representation of $I_{TRANSIENT}$.

Based on Ohms law:

$$V_{RIPPLE} = I_{TRANSIENT} * Z_{PDN}$$

Figure 3. Itransient Definition



The transient current is application-specific and is determined by the switching signal pattern. As a board designer, you have no control over this parameter. You can reduce the voltage ripple by reducing Z_{PDN} . The PCB portion of Z_{PDN} is under your control. You can optimize this parameter through good board design practices. To ensure that the voltage ripple noise is within the FPGA specification, the Z_{PDN} must be designed to meet a certain impedance, called Z_{TARGET} . Z_{TARGET} acts as your guideline on the magnitude of PCB impedance (Z_{PCB})


You can define Z_{TARGET} as follows:

Equation 1.

$$Z_{TARGET} = \left[\frac{VoltageRail \cdot \left(\frac{\%Ripple}{100} \right)}{MaxTransientCurrent} \right]$$

Where:

MaxTransientCurrent is the transient current estimated as a percentage of the total current draw.

 You can approximate the total current for the various Altera® power rails using the [PowerPlay Power Analyzer](#) or [Early Power Estimator](#).

The percentage of ripple is the maximum allowable voltage ripple specified by Altera. The ripple percentage and the maximum transient current values vary for different power rails.

The PDN tool for the Stratix IV GX device family provides a suggested frequency for PCB decoupling. This frequency is called $F_{EFFECTIVE}$. As explained in the following chapters, designing the PCB decoupling beyond this frequency does not result in a system PDN profile improvement. The PDN tool calculates this frequency by taking into account the PCB, package, and die parasitics.

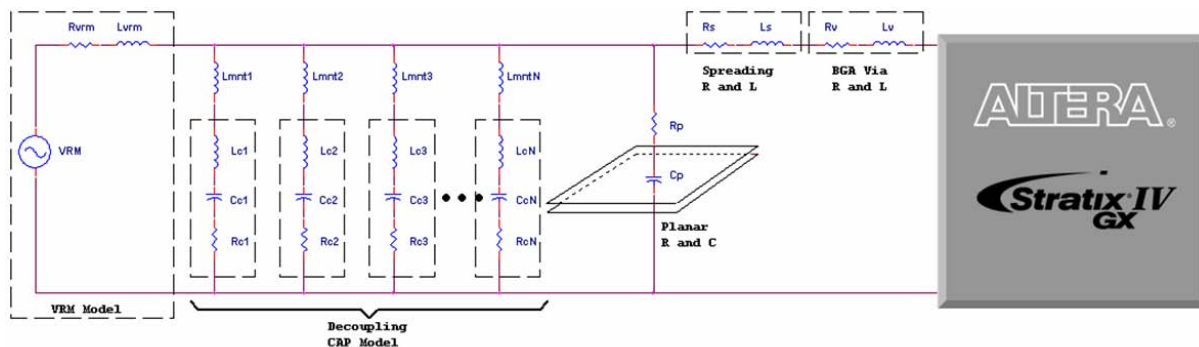
 For the Stratix IV GX device family recommended settings, refer to the [Power Delivery Network \(PDN\) Tool for Stratix IV Devices User Guide](#).

An efficient PDN design minimizes the impedance between the VRM and die such that Z_{PDN} either meets or is lower than Z_{TARGET} . Designing a power delivery network with Z_{PDN} under Z_{TARGET} over a wide band of frequency may or may not be possible under all scenarios. Also, from a design standpoint, this can be very expensive. You must make trade-offs to achieve a reasonable balance between cost and performance. The design trade-offs are described in [“PCB Design Trade-Offs” on page 12](#) and [“Design Trade-Offs for the Multi-Rail Scenario” on page 17](#).

Schematic Representation of the PDN Components

The Altera PDN tool is based on a lumped equivalent model representation of the power delivery network topology. Figure 4 shows a schematic representation of the circuit topology, modeled as part of the tool. The PDN impedance profile is the impedance over frequency looking from the device side.

Figure 4. Schematic Representation of PDN Topology



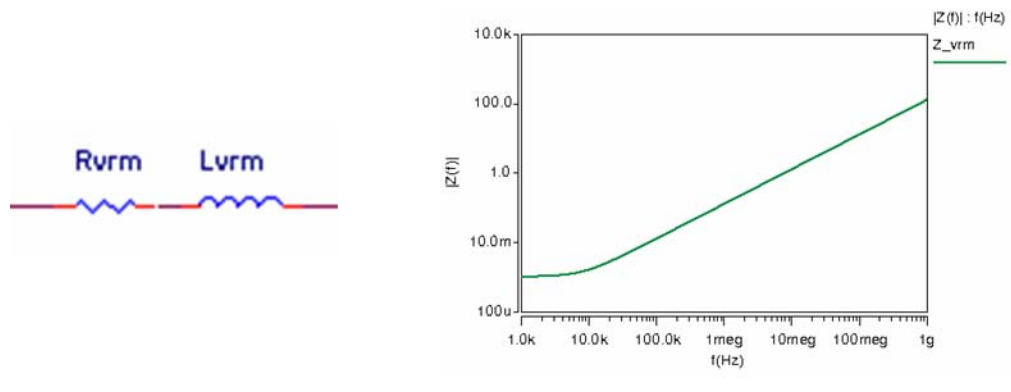
The PCB PDN network contains the following:

- Voltage regulator module (VRM)
- Decoupling capacitors
- Parasitics from power/ground plane spreading, and BGA vias
- Plane capacitance

Voltage Regulator Module (VRM)

For first order analysis, you can model the VRM as a series connected resistor and inductor, as shown in Figure 5. The simulated frequency response is also plotted in Figure 5.

At low frequencies, up to approximately 50 KHz, the VRM has low impedance and is capable of responding to the instantaneous current requirements of the FPGA. At higher frequencies, the VRM impedance is primarily inductive, making it incapable of meeting the transient current requirement. You can obtain the equivalent series resistance (ESR) and equivalent series inductance (ESL) values from the VRM manufacturer.

Figure 5. Voltage Regulator Module (VRM) Schematic and Frequency Response**Decoupling Capacitors**

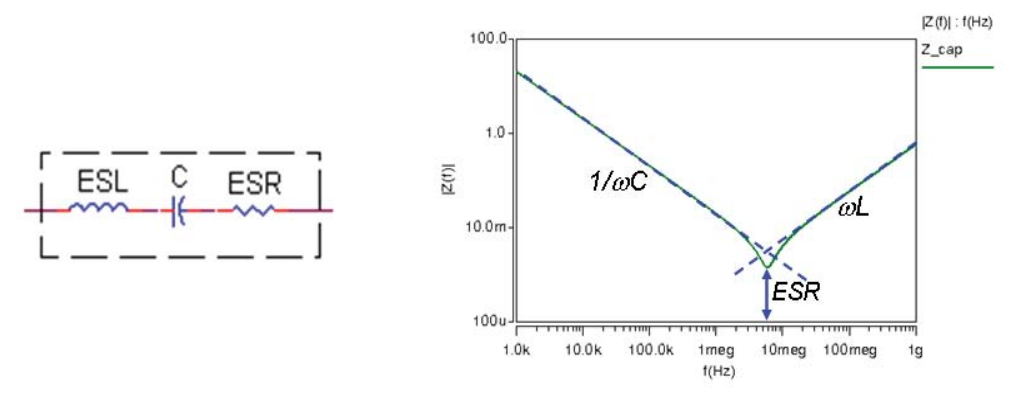
You can model a decoupling capacitor as a series combination of R, L, and C.

- R represents the equivalent series resistance (ESR) of the capacitor
- L represents the equivalent series inductance (ESL)
- C represents the capacitance of the capacitor

Figure 6 shows the frequency response of a capacitor. The equivalent circuit of a capacitor is an RLC series resonant circuit. The self-resonant frequency (SRF) is determined by the L and C of the circuit. This frequency is set by the materials and the construction of the capacitor, as shown in Equation 2.

Equation 2.

$$F = 1/2\pi\sqrt{LC}$$

Figure 6. Capacitor Schematic and Frequency Response

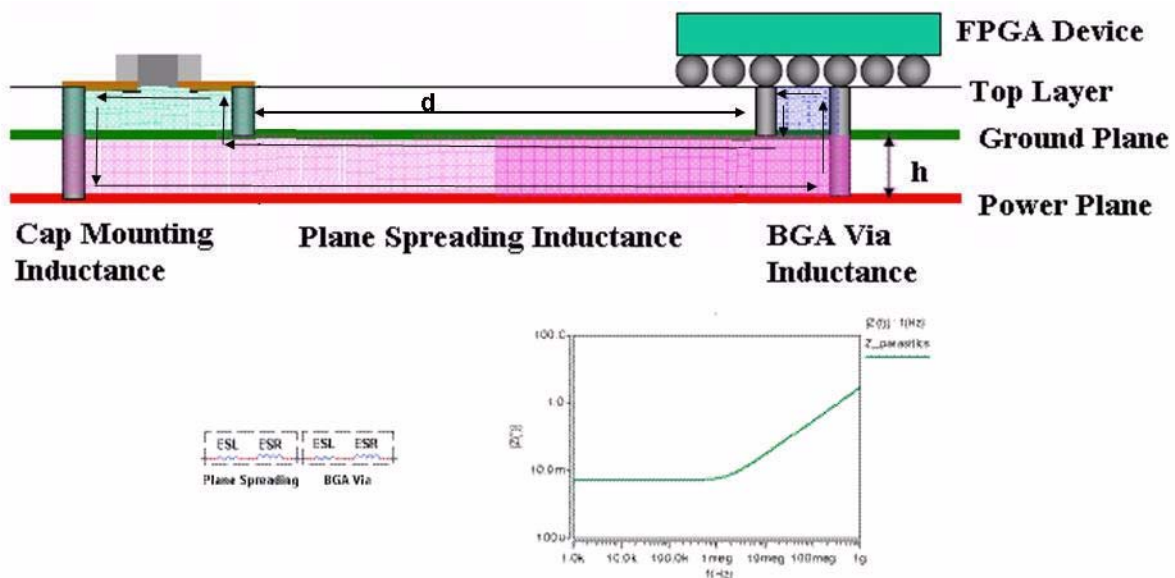
You can choose capacitors with a smaller footprint to minimize the inherent ESL of the capacitor. For example, a 0.1nF 0201 capacitor has a lower inherent ESL when compared with a 0.1nF capacitor with a larger footprint for the same dielectric material and capacitor construction (for example, 0402, 0603, 0805, and so forth). The ESR of the capacitor varies as a function of frequency. You must use the resistance at SRF to represent the capacitor using a lumped RLC model. Above SRF, the impedance of the capacitor is determined by the ESL and increases as a function of frequency. The impedance is independent of the value of the capacitor.

Parasitics from Power Ground Plane Spreading and BGA Vias

Figure 7 shows the schematic and equivalent representation of spreading and ball grid array (BGA) via inductance. In addition to mounting inductance associated with placing a capacitor on the PCB, the effectiveness of a decoupling capacitor also depends on the spreading inductance that the capacitor sees with respect to the load. The spreading inductance is design dependent and scales as a function of the dielectric thickness (h) between the power/ground plane. It is determined by the spatial location (d) of the capacitor with respect to the load. Minimizing the dielectric thickness (h) reduces the capacitor location sensitivity and allows you to place the capacitors farther away from the load.

In addition to the spreading inductance from the power/ground planes, current must travel through the via field underneath the BGA before it reaches the FPGA device. In the PDN tool, the inductance associated with BGA vias is modeled as BGA via inductance. The total inductance seen by any decoupling capacitor is a series combination of the mounting inductance, spreading inductance, and the BGA via inductance.

Figure 7. Capacitor Mounting, Spreading Inductance, BGA Via Inductance Schematic



Plane Capacitance

The amount of distributed capacitance seen by the power/ground sandwich is dependent on the following factors:

- Length of the plane
- Width of the plane
- Dielectric constant
- Dielectric thickness

You can approximate the amount of capacitance by using a parallel plate capacitor equation, as shown in Equation 3. Figure 8 shows the equivalent representation of the plane capacitance between the power/ground sandwich.

Equation 3.

$$C = \frac{\epsilon_0 * \epsilon_r * W * l}{h}$$

Where ϵ_0 = permittivity of free space = 0.225pf/inch

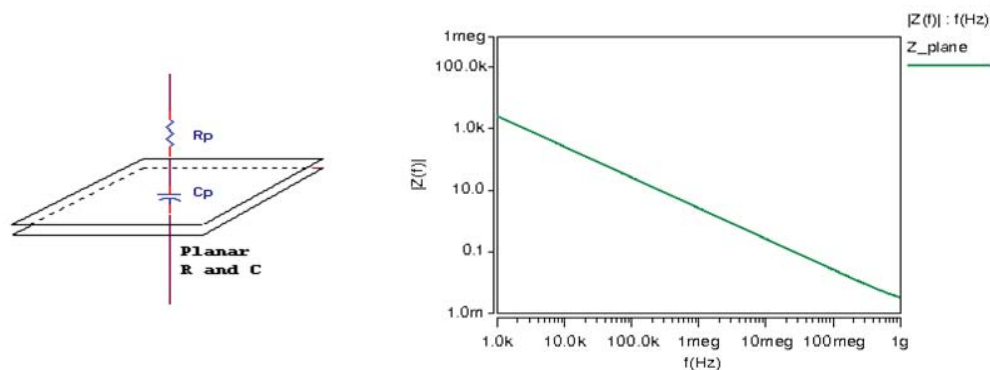
ϵ_r = relative permittivity (dielectric constant) of the dielectric material

W = width of the power plane in inches

l = length of the power plane in inches

h = distance between the power/ground plane in inches

Figure 8. Plane Capacitance Schematic and Frequency Response



Package and Die Parasitics

You can model the package and die parasitics in a similar fashion as the various PCB components. The on-die capacitance (ODC) and on-package decoupling (OPD) are responsible for meeting high-frequency power delivery network requirements. The die capacitance, followed by the OPD capacitor, is the first to respond by providing charge when there is a sudden spike in the current demand at high frequencies. Certain Altera device families; for example, Stratix III and Stratix IV, are designed with OPD.

Defining PCB PDN Cutoff Frequency

Altera's device-specific PDN tool calculates a unique frequency target based on your PCB design for designing a power delivery network. This frequency, referred to as $F_{\text{EFFECTIVE}}$ in the tool, is calculated by taking into account the parasitics on the PCB, the package, and the die you selected in the tool. The purpose of $F_{\text{EFFECTIVE}}$ is:

- To provide guidance on the transition frequency where the package/die takes over.
- To provide a reasonably accurate estimate on the range of frequency where the PCB decoupling is effective. Choosing decoupling capacitors with SRF beyond the $F_{\text{EFFECTIVE}}$ results in PCB over design without improvement in the overall impedance profile seen by the die.

$F_{\text{EFFECTIVE}}$ in PCB Decoupling

The PCB PDN cutoff frequency ($F_{\text{EFFECTIVE}}$) calculated by the PDN tool depends on the design trade-offs made on the PCB. The role of $F_{\text{EFFECTIVE}}$ is analyzed for both OPD and non-OPD packages.

Non-OPD Scenario

Figure 9 shows a simple topology for a rail without on-package decoupling.

Figure 9. Non-OPD Topology

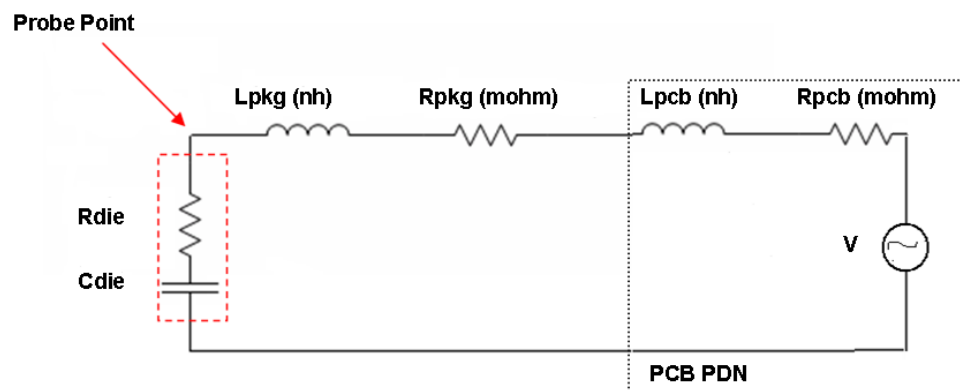


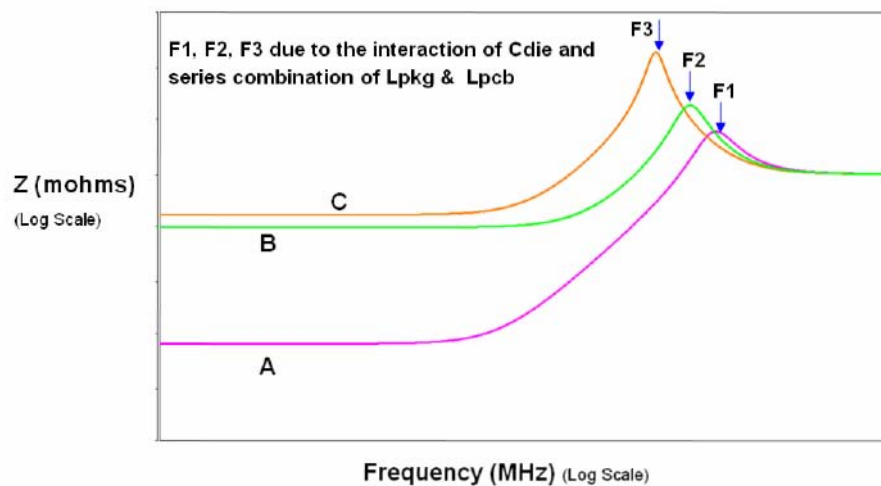
Figure 10 is the impedance profile seen by the die at the Figure 9 probe location. The probe point for this simulation is different from the BGA via probe location used to plot the Z_{EFF} in the PDN tool without the FPGA device. The die (R_{die} and C_{die}) and package (L_{pkg}) parasitics chosen to generate the waveforms in Figure 10 are not based on a specific power rail from an Altera device. These simulations are used to show PDN design concepts. To show the sensitivity of the resonance frequency to variations in inductance seen on the PCB, a low value of package inductance (L_{pkg}), along with high die capacitance (C_{die}), is assumed.

The resonance frequencies ($F1$, $F2$, and $F3$) in Figure 10 are due to the interaction of the series combination of inductance associated with the PCB and the package with on-die capacitance. You can calculate the resonance frequency using Equation 4.

Equation 4.

$$F = 1 / 2\pi \sqrt{(L_{pkg} + L_{pcb}) * C_{die}}$$

Figure 10. Non-OPD Topology Frequency Response



The purple waveform (A) in Figure 10 with resonance frequency $F1$ shows the Z -profile when L_{pcb} and R_{pcb} values are zero. This represents an "Ideal PCB" scenario where the PCB introduces no parasitics between the device and power supply.

The green waveform (B) in Figure 10 with resonance frequency $F2$ shows the "Low PCB parasitic" scenario where the PCB has low parasitic inductance and resistance. The simulation assumes a 30 p μ H PCB inductance and a small amount of resistance for this scenario. As shown in Figure 10, the impedance peak shifts to the left (lower frequency) along with an increase in the magnitude of the peak. The added PCB resistance causes an upward shift in Z -profile at low frequency.

The orange waveform (C) in Figure 10 with resonance frequency F_3 shows the "High PCB parasitic" scenario where the PCB has high parasitic inductance and resistance because of the non-optimized design. The simulation assumes 160 pH of PCB inductance and a higher resistance when compared with the "Low PCB parasitic" scenario. The impedance peak shifts to an even lower frequency (F_3) along with a higher magnitude of peak. The Z-profile at low frequency is higher as well.

 This variation in the inductance on the PCB is due to the design trade-offs that you make during the design process.

On-Package Decoupling (OPD) Scenario

Figure 11 is a generic topology for a rail with on-package decoupling.

Figure 11. OPD Topology

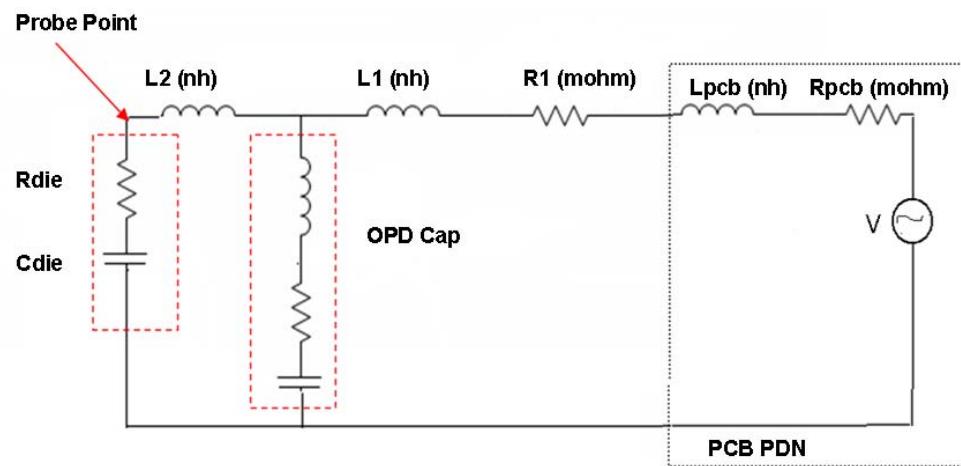


Figure 12 shows the impedance profile seen by the die at the probe location shown in Figure 11. The second peak to the right is due to the interaction of the die capacitance and the series inductance from the die to the OPD capacitor. The first peak is due to the interaction of the OPD capacitance and the series inductance from the PCB spreading inductance, BGA vias, and BGA balls seen by the OPD capacitor.

The second peak is insensitive to the design variations on the PCB. It is primarily a function of the FPGA on-die capacitance and the package design. You do not have control of the magnitude and frequency location of this peak. However, the location and magnitude of the first peak is of interest because you can affect the location and magnitude of this peak by changing the PCB parasitics and decoupling.

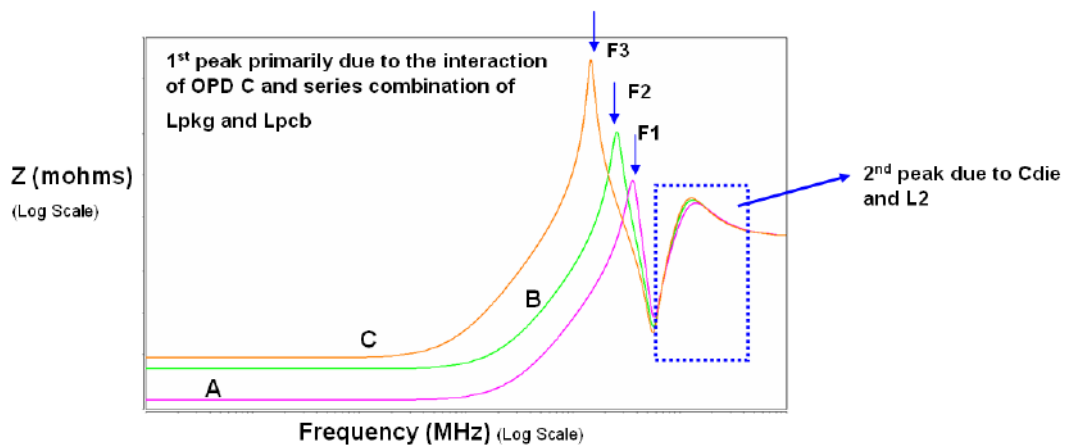
Figure 12. OPD Frequency Response

Figure 12 shows the simulated waveforms for three scenarios:

- Z-profile for "Ideal PCB"—The purple waveform (A) with resonance frequency F1
- Z-profile for "Low PCB parasitics"—The green waveform (B) with resonance frequency F2
- Z-profile for "High PCB parasitics"—The orange waveform (C) with resonance frequency F3

As the PCB inductance increases, the location of the first resonance peak shifts to the left (lower frequency) along with an increase in the magnitude of the peak.

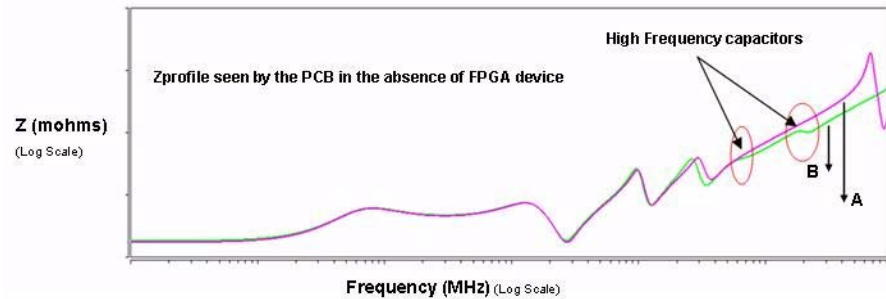
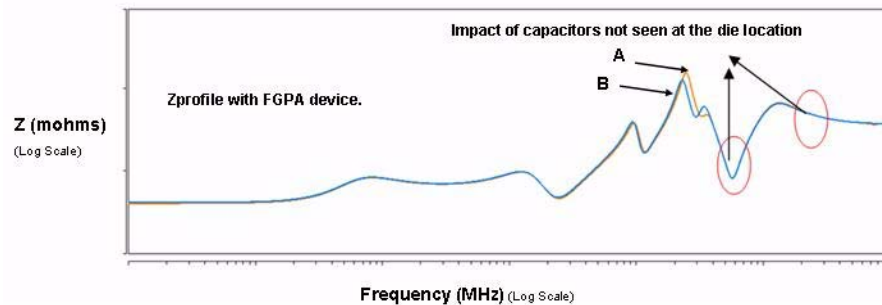
This shift in the frequency can be roughly calculated using Equation 5.

Equation 5.

$$F = 1 / 2\pi \sqrt{(L_{opd} + L1 + L_{pcb}) * C_{opd}}$$

When designing the power delivery network on the PCB, you must take a close look at the $F_{EFFECTIVE}$ frequency reported by the tool. As shown in the following example, over-designing the PCB by adding capacitors with a SRF beyond $F_{EFFECTIVE}$ results in additional build of materials (BOM) cost without performance improvements.

Two designs (A or B) are studied. All the parameters of the two designs are the same except that design B has additional high frequency capacitors with SRF located at the circled locations shown on the plot. Figure 13 shows the Z-profile of two designs probed at the BGA via location in the absence of the FPGA device. As shown in the plot, both profiles look exactly the same at low frequency. Design B (the green curve) impedance is lower than that of design A (the purple curve) at high frequency because of the addition of the high frequency capacitors.

Figure 13. Z-Profile at BGA Via Locations**Figure 14.** OPD System Z-Profile

The profile shown [Figure 14](#) is the system Z_{PROFILE} seen by the die. The orange curve represents the Z-profile of design A; the blue curve represents the Z-profile of design B. As shown in [Figure 14](#), the presence of OPD and ODC masks the effect of the high-frequency capacitors present on the PCB. This shows that adding PCB capacitors beyond the PCB cutoff frequency ($F_{\text{EFFECTIVE}}$) as reported by the Altera PDN tool does not improve the overall system PDN performance.

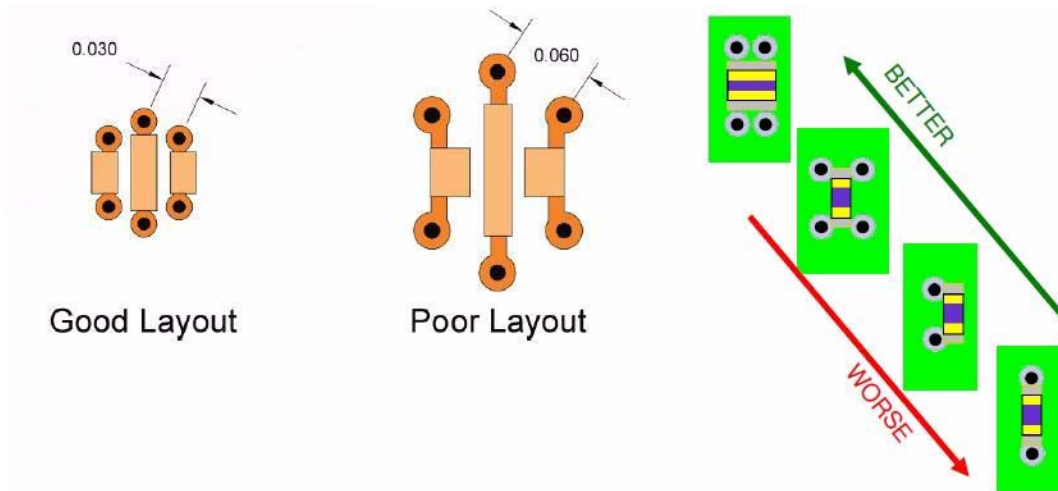
[Figure 13](#) also shows that high-frequency PCB decoupling capacitors are not very effective at high frequency. The effectiveness of the PCB capacitor is affected by the parasitic inductance from PCB spreading, BGA via, and capacitor mounting. You must reduce the parasitic inductance to improve the effectiveness of the high-frequency PCB capacitors. The following section describes design practices that help reduce parasitic inductance.

PCB Design Trade-Offs

You must make design trade-offs due to the complexity of the board design process. Because of these trade-offs, there are performance implications on the effectiveness of the resultant PCB power delivery network design.

When a capacitor is mounted on a PCB, there is additional loop inductance associated with the capacitor mounting. The value of this loop inductance is design-dependent. Loop inductance is based on the width and length of the trace that connects the vias, the length of the vias used to connect the capacitor to the power/ground plane, the pitch between the vias, the diameter of the vias, the capacitor pads, and so forth. Figure 15 shows the various capacitor mounting configurations.

Figure 15. Optimal and Non-Optimal Capacitor Layout

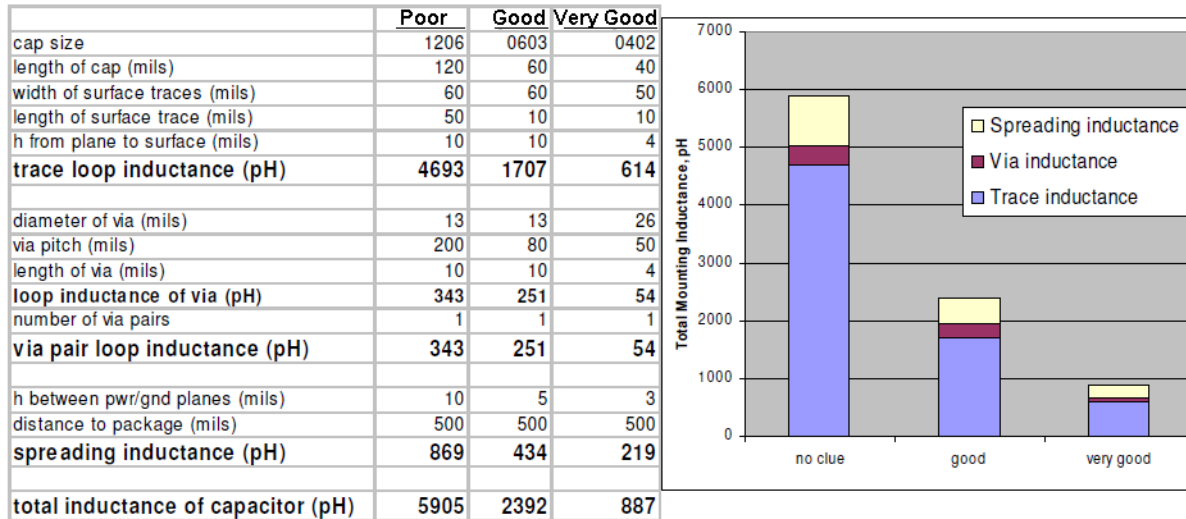


The key design rules for minimizing the capacitor loop inductance are:

- Place the vias as close as possible to the capacitor. Minimize the via pitch between the power/ground vias. If possible, use multiple power/ground via pairs. Place the vias such that the opposite current polarity vias are close together and the same polarity vias are far away from one another.
- Use short, wide surface traces to connect the capacitor pads to the vias.
- Place the capacitors on the PCB surface (top and bottom) closest to their corresponding power/ground planes. This minimizes the via length. Use thin dielectric between the power/ground planes.

The following are three design scenarios for capacitor mounting and spreading inductance. Figure 16 shows the loop inductance contribution for the various design scenarios.

Figure 16. Design Scenarios



Case One—Poor Design Scenario

- The designer does not pay attention to the PDN design.
- The via pitch is not optimized.
- The thickness of the dielectric material between the power/ground plane is not optimized.
- The length of the trace is long.

The trace loop inductance is the dominant contributor to the overall loop inductance because the trace length is 5 times longer when compared with the other two scenarios. The height from the bottom surface of the capacitor to the nearest plane also significantly contributes to the trace loop inductance. Because this was not optimized (10 mil), the trace contribution to the overall loop inductance is very high. Also, because the designer has used 10-mil thick dielectric material between the power/ground plane, the spreading inductance is the second most dominant contributor. The effect of the non-optimal via pitch is not showing up significantly given the relatively small via length (10 mil). The via contribution would become significant for a longer via length.

Case Two—Good Design Scenario

- The designer pays some attention to the PDN design.
- The via pitch is improved. The via length remains the same.
- The thickness of the dielectric material between the power/ground plane is improved.
- The length of the surface trace is optimized.

Trace loop inductance is still the dominant contributor to the overall loop inductance. However, the contribution of the trace loop inductance is ~2.75 times less than the poor scenario due to the reduction in trace length. Because the designer has reduced the thickness of the dielectric material from 10 mil to 5 mil, the spreading inductance is cut in half from the poor scenario. The via contribution is slightly improved due to the reduction in via pitch.

Case Three—Very Good Design Scenario

- The designer fully optimizes the PDN design.
- The via pitch and length are improved.
- The thickness of the dielectric material between the power/ground plane is fully optimized.
- The length of the surface trace is optimized.

The contribution of the trace inductance is ~7.65 times less than the poor scenario. This is achieved due to the reduced trace length along with a reduction in the board thickness from the bottom surface of capacitor to the nearest plane. Because the designer has optimized the dielectric thickness between the power/ground plane, the spreading inductance is reduced further. The via loop inductance contribution is improved significantly due to a further reduction in the via pitch and via length. The total loop inductance was reduced by a factor of seven when compared with the poor design scenario.

The additional via loop inductance introduced by mounting a capacitor on the PCB decreases the observed SRF of a capacitor. You must take this factor into account when designing your power delivery network. Minimizing the loop inductance is the only way to reduce the impedance seen at high frequencies.

For a given power rail, The PDN tool reports that the PCB cutoff frequency for the “Very Good” design will be higher when compared with the Poor design scenario. This may be counter intuitive because decoupling to a higher $F_{\text{EFFECTIVE}}$ frequency requires more capacitors when compared with decoupling to a lower $F_{\text{EFFECTIVE}}$ frequency.

For a “Very Good” scenario, the higher $F_{\text{EFFECTIVE}}$ means that the board is capable of decoupling to a higher frequency. The capacitors that are placed on the board are effective in reducing the noise until a higher frequency.

For the “Poor” design scenario, the board is incapable of decoupling beyond the lower $F_{\text{EFFECTIVE}}$ frequency. Any additional capacitors that are added beyond the $F_{\text{EFFECTIVE}}$ frequency only increases the build of materials (BOM) cost without being effective. For this scenario, the PDN design is more susceptible to noise at certain frequencies when compared with the “Very Good” scenario.

As another example, assume a 20-layer PCB with a total thickness of 115 mil. The power plane of interest is located on layer 3. The thickness from the top of the board where the FPGA is located to layer 3 is 12 mils. The thickness from the bottom of the board to layer 3 is 103 mil. The power/ground planes are separated by a dielectric thickness of 3 mils. The BGA via inductance contribution for this rail is 0.05 nH (five via pairs for this power rail). The associated decoupling capacitors for the rail are

located on the bottom layer of the board due to tight breakout routing on the top layer of the board. This trade-off results in a very high value of the capacitor mounting inductance due to the long via lengths. The fully optimized capacitor mounting inductance for a 0402 capacitor placed on the bottom layer is 2.3 nH, while the same capacitor placed on the top layer yields a mounting inductance of 0.57 nH.

To improve the effectiveness of the PDN for this rail, you can move some of the high-frequency capacitors to the top while keeping the mid-frequency and bulk capacitors at their original locations. This is critical for an effective PDN solution because the high-frequency capacitors are the first ones to respond on a PCB below the $F_{\text{EFFECTIVE}}$ frequency. The capacitor effectiveness depends on the total loop (capacitor mounting + spreading + BGA via inductance) inductance with respect to the FPGA device. You can place these high-frequency capacitors slightly far away from the device on the top layer. The spreading inductance for the capacitor located away from the FPGA breakout region is 0.2 nH for the above configuration. This new placement is still beneficial when compared with the original scenario because the total loop inductance (0.57 nH + 0.2 nH + 0.05 nH = 0.82 nH) is lower than the bottom layer capacitor mounting inductance.

The PCB spreading inductance is design-dependent. It is proportional to the thickness of the dielectric material between the power/ground plane. A thickness of 3 mils or lower is optimal for minimizing plane spreading inductance. You can follow these guidelines for effective PDN performance.

The following guidelines are in the order of importance from top to bottom—the guidelines at the top are the most important:

- Minimize the dielectric thickness between the power/ground plane. When designing the board stackup, ensure that the power/ground layers are next to one another. As an example, a stackup arrangement with PWR1 - GND1 - SIG1 - SIG2 - GND2 - PWR2 is preferable to PWR1 - SIG1 - GND1 - SIG2 - GND2 - PWR2. The second orientation results in a non-optimal arrangement for PWR1/GND1. This configuration results in larger capacitor spreading inductance for PWR1/GND1 when compared with PWR2/GND2. You can achieve a typical dielectric thickness of 3 mils between the power/ground planes without additional PCB cost. For additional performance improvements, consider dielectric thickness lower than 3 mils. However, this leads to an increase in the cost of the PCB.
- When selecting the capacitors, choose capacitors with multiple values rather than a large number of capacitors of the same value to meet your target impedance. The impedance peaks in Z-profile are formed by resonance behavior within the power delivery network. High ESR at resonance frequency helps in damping the resonance, thereby reducing the magnitude of the impedance peak. Using a large number of capacitors of the same value significantly reduces the ESR near a capacitor SRF and results in a higher magnitude of nearby impedance peaks. Choosing capacitors with multiple values helps maintain a relative high ESR over a wide frequency range.
- Choose the placement of the high-frequency capacitors so that you minimize the overall loop inductance. This overall inductance is a combination of capacitor ESL, capacitor mounting, capacitor spreading, and BGA via inductance. Give high-priority placement to high-frequency capacitors when compared with mid- and low-frequency capacitors.

- When carving plane shapes, ensure the plane shapes are reasonably square in shape. Avoid having a long and narrow plane shape because this limits the current flow and increases plane spreading inductance.
- The mid- and low-frequency capacitors are not sensitive to placement. They can be placed far away from the FPGA.

Design Trade-Offs for the Multi-Rail Scenario

Your design can end up sharing a power supply on the board with multiple rails on the device. This may be required by your design where, to implement a DDR interface, you combine the various I/O bank rails or you combine the various transceiver rails to reduce the PCB BOM cost and the PCB layout complexity.

Power rail sharing increases PDN complexity. Rail sharing may increase the amount of the noise seen at the PCB and die locations. Designing the power delivery solution for a multi rail scenario is a two step process:

1. Low-frequency solution
2. High-frequency solution

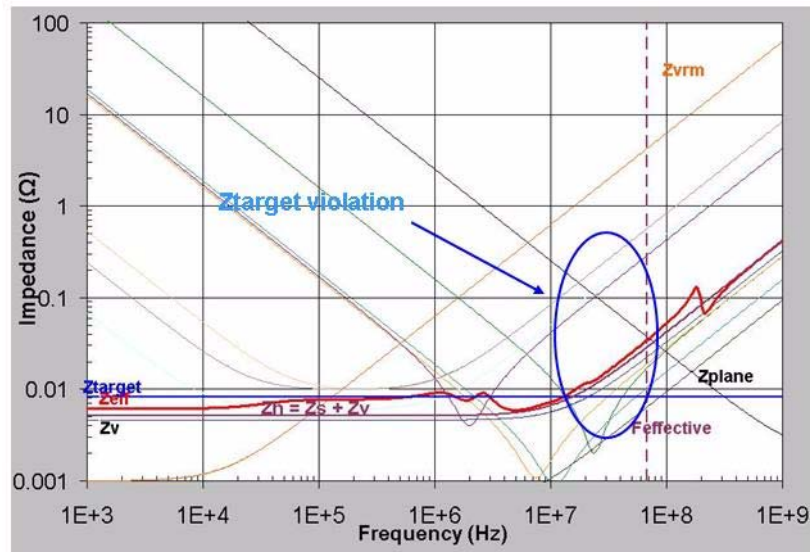
At very low frequencies, the first step is to ensure that the VRM is sized appropriately to handle the current requirements of the various rails that are feeding off this supply. Low-frequency decoupling must be designed by taking into account the combined current of the various power rails. The bulk capacitors must be selected so that the target impedance (using the combined current) is met across a range of frequencies. It is difficult to exactly quantify this frequency range because there is a transition region beyond which the impedance profile that a given rail sees at the die is based on its own current draw rather than a combined current draw associated with all the other rails that are feeding off the same power supply. A reasonable estimate for designing the bulk decoupling is a frequency range from DC to approximately 5–10 MHz.

The methodology used by the PDN tool follows a similar approach but recommends you decouple to the highest $F_{\text{EFFECTIVE}}$ frequency among the shared rails. This is done to arrive at a single PDN tool design flow for both single- and shared-power rail decoupling. This approach is suitable for power rail sharing among power rails with similar current demands. However, there are certain exceptions to this methodology.

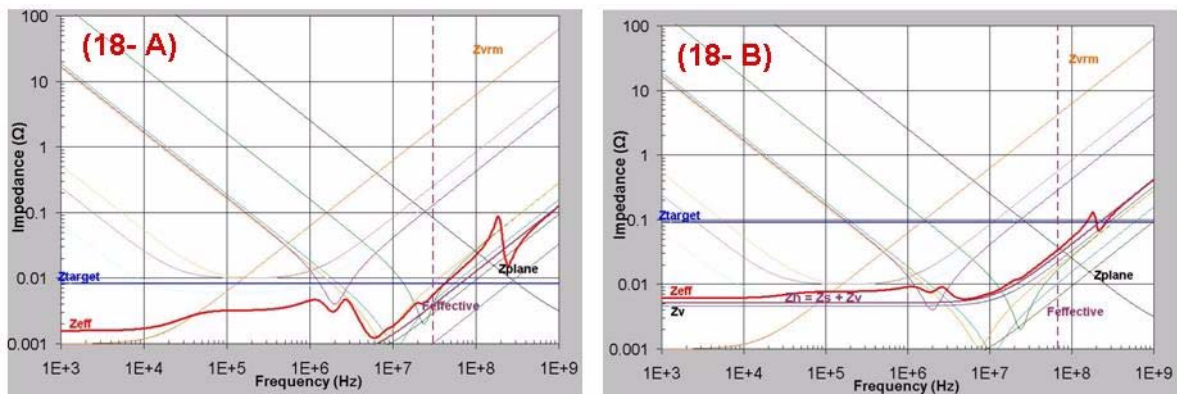
An example is the power rail sharing among the core power supply (V_{CC}) and the PCI Express hard IP Block (V_{CCHIP}) power supplies. The reasons behind the exception are:

- The current draw for the V_{CC} rail will be much larger than V_{CCHIP} .
- The BGA via inductance contribution for V_{CC} is much lower (a large number of BGA ball/via pairs) when compared with V_{CCHIP} .
- The $F_{\text{EFFECTIVE}}$ frequency for V_{CC} is much lower than V_{CCHIP} .

Therefore, the existing methodology of decoupling to the highest $F_{\text{EFFECTIVE}}$ frequency using the BGA vias for the rail with the highest $F_{\text{EFFECTIVE}}$ is not applicable for this scenario. [Figure 17](#) shows the impedance profile of the combined V_{CC} , V_{CCHIP} rail not meeting the Z_{TARGET} up to the V_{CCHIP} rail $F_{\text{EFFECTIVE}}$ frequency. This is because of the decap effectiveness limitations imposed by the overall PCB inductance.

Figure 17. $Z_{PROFILE}$ with V_{CCHIP} $F_{EFFECTIVE}$ Frequency

As explained previously, high-frequency noise within a power rail is mainly created by its own transient current. It is overly pessimistic to use Z_{TARGET} calculated based on the total transient current as the decoupling guideline to the highest $F_{EFFECTIVE}$ of the shared rails.

Figure 18. Modified Power Rail Sharing Scenarios

In such situations, you must derive the PCB decoupling scheme using Z_{TARGET} calculated with the total transient current up to the $F_{EFFECTIVE}$ of the power rail with the largest current draw. You must use the $F_{EFFECTIVE}$ of the V_{CC} rail in the V_{CC} and V_{CCHIP} power rail sharing example. Figure 18-A shows the $Z_{PROFILE}$ of the combined rail when decoupling to the $F_{EFFECTIVE}$ frequency of the core interface. The total current ($V_{CC} + V_{CCHIP}$), along with the BGA ball/via pairs for the core interface, were used to derive the $Z_{PROFILE}$. You can then check if you have met the individual target impedance guideline for these rails up to their individual $F_{EFFECTIVE}$ with the derived PCB decoupling scheme.

Figure 18-B shows the Z_{PROFILE} for the V_{CCHIP} interface based on the same decoupling scheme used in Figure 18-A. However the current draw and the BGA via count for only V_{CCHIP} are taken into account when deriving this profile. As seen in Figure 18-B, the Z_{PROFILE} meets the Z_{TARGET} until the $F_{\text{EFFECTIVE}}$ frequency of the V_{CCHIP} rail.

The final decoupling scheme that you arrive at must be able to meet the individual Z_{TARGET} frequency to their respective $F_{\text{EFFECTIVE}}$ frequencies. If there are any specific violations, you can make minor adjustments to optimize the decoupling scheme.

You can follow the example of V_{CC} and V_{CCHIP} for any power supply combination that have similar characteristics.

You can apply a similar strategy to a scenario where multiple FPGA devices are being fed from the same power supply on the board. The total current draw from both devices must be used for designing the low-frequency solution and the current draw associated with one device must be used for the high-frequency solution. You can replicate the same number of capacitors arrived at for the high-frequency scenario for the other device.

If the two FPGA devices are spatially very close to each other, the high frequency approach may result in a slight over-design when compared with the solution offered by a field solver tool, which takes into account the board layout. This may be because the devices are spatially close to one another and fewer capacitors may be sufficient to address the needs of both devices. This is also dependent on the effective loop inductance that the capacitors see with respect to these FPGA devices.

One of the most commonly used design trade-offs is to create a separate power island and use a filter to provide clean power to a power rail from a power supply that supplies a different power rail. In most cases, the filter is a ferrite bead connecting the two power rails on the board. As a rule, you can follow these guidelines to supply clean power to a given power rail:

- Ensure that the mounting inductance is minimized when connecting the ferrite bead across the two rails of interest.
- Choose the ferrite bead based on the characteristics listed below. Ensure that the current draw for the power rail is smaller than the rated current of the ferrite bead.
 - Package (0603, 0402, and so forth)
 - Rated current
 - DC resistance
 - Impedance at the target frequency (10 MHz, 100 MHz, 1 GHz, and so forth)
- An equivalent RLC model for the ferrite bead must be created that closely matches the frequency response given in the data sheet.
- An AC analysis must be performed by including the ferrite bead model with the various capacitors that were chosen to meet the target impedance across the frequency of interest. When designing the equivalent RLC models for the capacitors, the mounting inductance must be included as part of the model. If the AC response does not show peaking in the frequency of interest (DC to 200 MHz), you can use the ferrite bead to provide clean power to the rail.
- The resultant PDN profile from the above simulation must meet the target impedance across the frequency of interest.

Reference Document

This application note referenced the following document:

- *Power Delivery Network (PDN) Tool for Stratix IV Devices User Guide*

Document Revision History

Table 1 shows the revision history for this application note.

Table 1. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
May 2009, v1.0	Initial release.	—



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