

## Introduction

The Altera® V-Series of reference designs deliver high-quality up, down, and cross conversion of standard definition (SD), high definition (HD) and 3 gigabits per second (Gbps) video streams in interlaced or progressive format. The reference designs are highly software and hardware configurable, enabling rapid system configuration and design. The designs have been developed targeting typical broadcast applications such as switcher, multi-viewer, converter, and video conferencing products.

The V-Series of reference designs is an evolution of the M-Series of video processing reference designs (M1–M5). The V-Series provides a roadmap of functionality key to broadcast applications, as well as run-time capability and software configurability typically associated with ASSPs.



For more information on the M-Series of reference designs, refer to the [Broadcast](#) page on the Altera website or contact the Altera Broadcast Business Unit.

The V-Series reference designs are working application templates that can be used directly or as a starting point to rapidly build further broadcast applications using a flexible, re-usable, and parameterizable video framework.

The configuration of video interfaces and control of video processing functions is conveniently implemented in software. This environment provides a very rapid development cycle for software control code changes, without the requirement for hardware re-compilation.

All the hardware functions in the designs use standard, open interfaces and protocols to facilitate function re-use and system design. The Video and Image Processing Suite MegaCore functions use Avalon® Streaming (Avalon-ST) data interfaces and Avalon Memory-Mapped (Avalon-MM) control interfaces to simplify the connection of a chain of video functions and video system design. Video data is transmitted between the Video and Image Processing Suite functions using the Avalon-ST Video protocol, which facilitates building run-time controllable systems and handling error recovery.



For a full description of how the Avalon-ST Video protocol and Avalon interfaces are implemented, refer to the [Interfaces](#) chapter in the *Video and Image Processing User Guide*. For more information about the Avalon-MM and Avalon-ST interfaces, refer to the [Avalon Interface Specifications](#).

The V-Series designs are delivered using the system level design tool SOPC Builder to facilitate system capture, integration, parameterization and system generation. SOPC Builder provides a library of parameterizable software and hardware IP modules, an abstracted view of the system interconnect, and automatically creates the bus arbitration logic connecting the individual components together to create an overall system.



For more information on SOPC Builder, refer to the [SOPC Builder User Guide](#).

The designs use the Altera Video and Image Processing Suite MegaCore® functions library, the SDI MegaCore function, the DDR2 High Performance Memory Controller MegaCore function, the Nios® II processor, and supporting development tools.



For information about these MegaCore functions, refer to the *Video and Image Processing Suite User Guide*, *SDI MegaCore function User Guide*, *DDR and DDR2 SDRAM High-Performance Controller User Guide*, and the *Nios II Processor* handbooks on the Altera website.

## Key Features

Table 1 lists the key features of the V1 reference design.

**Table 1.** Key Features of the V-Series Reference Designs (Part 1 of 2)

| Feature      | Description   |
|--------------|---|
| Input        | Two video input streams from a triple-rate serial digital interface SDI MegaCore function support SD-SDI, HD-SDI, or 3G-SDI progressive/interlaced inputs up to 1080p60 (such as: NTSC, PAL, 720p, 1080i, and 1080p). All frame rates up to 60Hz supported (including 30 Hz, 59.94 Hz, 60 Hz).  |
| Output       | One video output stream via a digital video interface (DVI). Run-time switching of output resolution (1920×1080p60, 1280×720p60, or 720×480p60) using push-button switches.   |
| Processing   | <p>Two streams are mixed with a test pattern background stream.</p> <p>Auto-detects inputs and can receive either 0 (test pattern output only), 1, or 2 active video sources.</p> <p>Multiple viewing modes:</p> <ul style="list-style-type: none"> <li>■ Both streams side by side</li> <li>■ Stream 1 upscaled to output resolution</li> <li>■ Stream 2 upscaled to output resolution</li> </ul> <p>Format conversion functions include clipping, chroma resampling, color space conversion, deinterlacing, and scaling.</p> <p>Stream 1:</p> <ul style="list-style-type: none"> <li>■ High quality processing (motion adaptive deinterlacer, 12×12 tap scaler)</li> <li>■ Voltage-controlled crystal oscillator (VCXO) used to synchronize input and output video clock rates (where applicable) to reduce judder</li> <li>■ Performs frame rate conversion in the deinterlacer function between input and output to support any input frame rate</li> </ul> <p>Stream 2:</p> <ul style="list-style-type: none"> <li>■ Lower quality processing (weave deinterlacer, nearest neighbor scaler)</li> <li>■ Performs frame rate conversion in the deinterlacer function between input and output to support any input frame rate</li> </ul> |
| Software     | System initialization and configuration in software. Dynamic scaler coefficient generation and reload. Class application programming interface (API) provided to facilitate read/write access to the Video and Image Processing Suite register maps at run time.  |
| System Tools | Rapid system capture and design with SOPC Builder, Quartus® II, and the Nios II development environments.   |

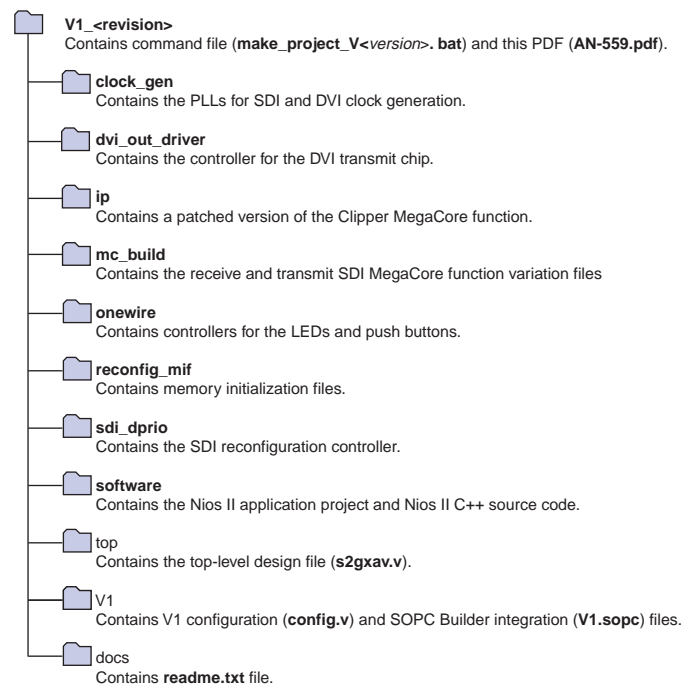
**Table 1.** Key Features of the V-Series Reference Designs (Part 2 of 2)

| Feature            | Description  |
|--------------------|--|
| Design Framework   | Highly parameterizable and modular hardware functions (15 Video and Image Processing Suite MegaCore functions, Nios II processor, open source software for system configuration, video frame buffers, high performance memory controllers, peripherals, auto-generation of switch fabric). Standard Avalon-ST and Avalon-MM interfaces for rapid integration, and Avalon-ST Video protocol for video transmission between functions. |
| Device Support     | Stratix II GX (2SGX90) Audio Video Development Kit   |
| Device Utilization | 94% logic, 42% memory implementation bits, 29% DSP blocks  |

## Installing the Reference Design

The V-Series reference designs are available as a **.zip** file from the [Broadcast](#) pages on the Altera website.

[Figure 1](#) shows the directory structure for the reference design files when they have been extracted from the **.zip** file.

**Figure 1.** Reference Design Directory Structure

The top level directory contains a command file **make\_project\_V<version>.bat**.

Run this command file to:

- Copy a SOPC Builder project file (**.sopc**) to the top level
- Copy the design configuration file (**config.v**) to the top level
- Generate the Quartus II project files (**.qpf**, and **.qsf**)

## System Requirements

This section describes the hardware and software requirements to run the V-Series reference designs.

### Hardware Requirements

The video monitoring reference design requires the following hardware components:

- Audio Video Development Kit Stratix II GX Edition including:
  - Stratix II GX video development board
  - Digital video interface (DVI) and serial digital interface (SDI) inputs and outputs
  - DDR2 DIMM external memory
- A monitor or display with a DVI interface supporting 1,920×1,080 resolution
- One DVI cable to connect the DVI\_TX output to the monitor
- Two SDI sources providing progressive or interlaced output up to 1080p60 output.
- Two coaxial cables to connect the SDI sources to the BNC connectors SDI\_IN0 and/or SDI\_IN1 on the development board.

### Software Requirements

Table 2 shows the operating systems and software tool versions that are supported by the V-Series of reference designs.

**Table 2.** Operating Systems and Software Tool Versions supported by V-Series Reference Designs

|    | Operating System    | Altera Software Tools | Altera Development Kit              |
|----|---------------------|-----------------------|-------------------------------------|
| V1 | Windows XP or Linux | v8.1                  | Stratix II GX (2SGX 90) Audio Video |

**Note to Table 2:**

- (1) The Altera software tools include the Quartus II software, SOPC Builder, Nios II EDS, and MegaCore IP Library (including the Video and Image Processing Suite).

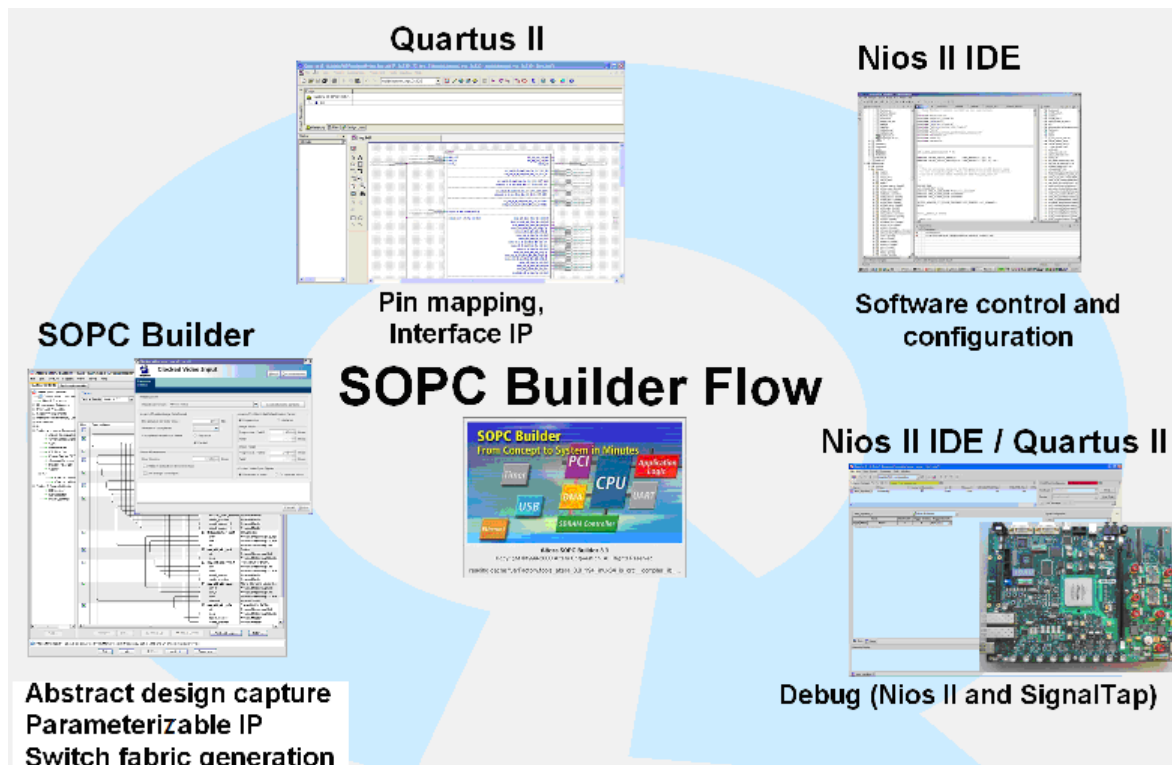


For more information on the Altera development kit software installation, refer to the documentation provided with the development kit.

## Video Design Flow

The V-Series reference designs demonstrate a simple, yet highly parameterizable, design flow for rapid system development. **Figure 2** provides a high level view of the typical design flow within Altera's video design framework.

**Figure 2.** SOPC Builder Design Flow



The video design framework provides:

- Open interface and protocol standards to enable design re-use, and connection of custom IP functions with off-the-shelf IP including:
  - Data streaming interfaces and protocols for transmission of video data between IP functions in the framework (Avalon-ST Video protocol layers on the Avalon-ST interface)
  - Control interfaces (Avalon-MM master and slave interfaces)
  - Random access to external memory (Avalon-MM master and slave interfaces)
- System level tools and design methodology for rapid system construction, integration and re-design. The SOPC Builder tool takes advantage of standard interfaces by presenting an abstracted view of the design, and generating an application specific switch fabric to construct the system.
- Parameterizable MegaCore IP functions that enable you to quickly construct complete video systems.
- Reference designs that demonstrate the capabilities of the video framework.
- Development kits to rapidly prototype the designs.

The reference designs described in this application note demonstrate each of these aspects of the framework. The video design tool flow is described in the following sections.

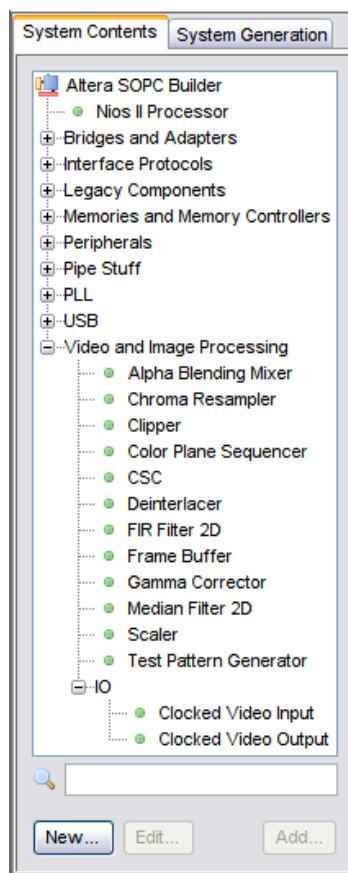
## SOPC Builder

The SOPC Builder tool flow is the primary design flow for rapid video system development. Specifically, SOPC Builder simplifies the process of system design, including the data path, processor core and external memory integration. The tool enables you to capture the design at an abstract level with single point-to-point data connections rather than connecting individual data and control interface wires.

All the connections in the SOPC Builder system use Avalon-ST and Avalon-MM interfaces. SOPC Builder enables you to rapidly build systems containing IP products that support the Avalon-ST Video protocol and Avalon-MM interfaces. The Video and Image Processing Suite MegaCore functions that support Avalon-ST Video protocol for data transmission can be connected together by the click of a button.

The MegaCore functions are displayed in the SOPC Builder **System Contents** tab under the category **Video and Image Processing** as shown in [Figure 3](#).

**Figure 3.** Video and Image Processing Functions in the SOPC Builder System Contents tab

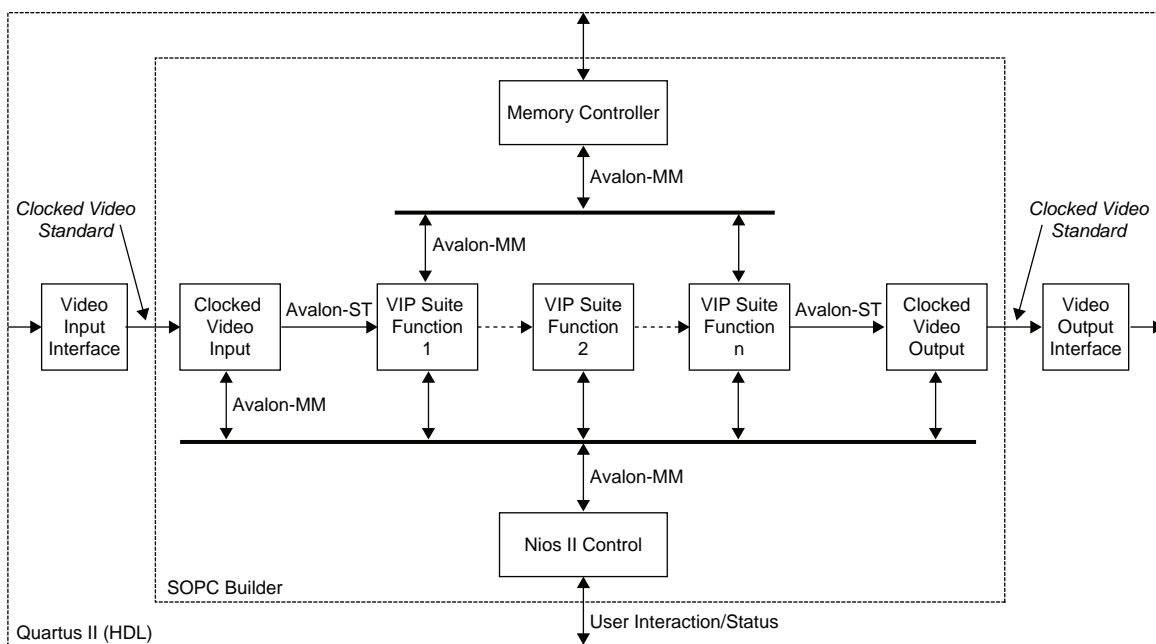


The SOPC Builder tool automatically generates an interconnect switch fabric, including arbitration logic to connect together the memory mapped masters and slaves. A common example is where the system contains multiple Avalon-MM Masters which need to buffer video data in an external memory using a single memory controller.

The video design flow in SOPC Builder (Figure 4) has four main external connections:

- Video input from an external video interface. The connection to the external video interface is made using a parameterizable video conversion IP function. The IP function provides a bridge between a clocked video interface (such as a SDI MegaCore function) and the Avalon-ST flow controlled domain.
- Video output to an external video interface. The connection to the external video interface is made using a parameterizable video conversion IP function. The IP function provides a bridge between the Avalon-ST flow controlled domain and a clocked video interface (such as DVI).
- Connection to an external memory interface. This connection uses a DDR and DDR2 SDRAM High performance Controller MegaCore function. SOPC Builder generates the application specific switch fabric to arbitrate between multiple masters trying to access the controller.
- Connection to user controls and board components such as push buttons, LEDs, and quad seven-segment displays.

**Figure 4.** V-Series Video Design Flow Block Diagram



## The Quartus II Software

The top-level system is described within the Quartus II software environment and the SOPC Builder system is integrated into the top level design. The Quartus II software environment is well suited for mapping external connections to the SOPC Builder system in the form of exported wires to video interface IP (such as SDI) and memory interfaces (such as DDR2) as well as making the appropriate pin assignments.

A wide range of tools are provided to facilitate timing closure and perform hardware compilation to generate an FPGA programming file.

The Quartus II software also provides a system-level debugging tool (SignalTap® II logic analyzer) that captures and displays real-time signal behavior so you can observe interactions between hardware and software in system designs.



For information on the Quartus II software, refer to the Quartus II Help.

## Nios II IDE

The Nios II integrated development environment (IDE) is the primary software development tool for the Nios II family of embedded processors. All software development tasks can be accomplished within the Nios II IDE, including editing, building, and debugging programs.

The Nios II IDE provides a consistent development platform that works for all Nios II processor systems. Configuration of video interfaces and control of video processing functions can conveniently be implemented in software. This provides a very rapid development cycle for software control code changes, without the requirement for hardware re-compilation.

This environment provides you with all the standard software debug tools, including breakpoints, memory/variable/register windows, and single stepping. This flow is further enhanced by the inclusion of C++ software classes that provides a software API between the Nios II control code and the Video and Image Processing Suite MegaCore functions. The C++ classes contain member functions that provide easy control of the MegaCore functions and easy access to useful data flow information such as the number of frames that have been dropped or repeated by a frame buffer in the data path.



For information on the Nios II IDE software, refer to the Nios II Help.

## Functional Description

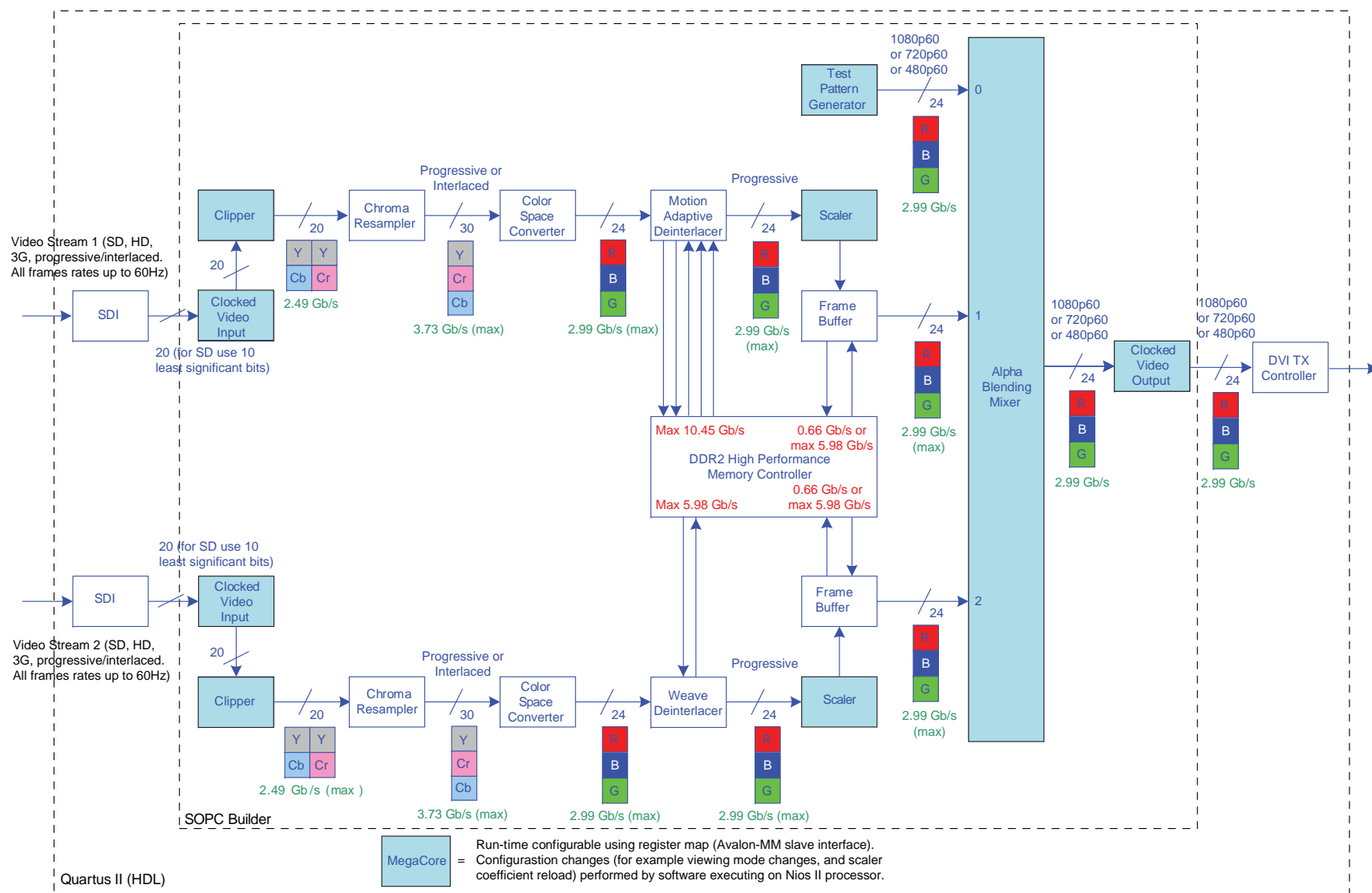
Figure 5 on page 9 shows a detailed block diagram of the V1 reference design.

### Video Input

Video is input to the Stratix II GX 90 device using two triple-rate SDI MegaCore functions, supporting data in SD-SDI, HD-SDI or 3G-SDI standard format. Both video streams, with active picture data in Y'CbCr 4:2:2 format and associated embedded synchronization signals, are input from the SDI functions to the Clocked Video Input MegaCore functions.



**Figure 5.** V1 Reference Design Block Diagram



The Clocked Video Input MegaCore function converts from a notionally clocked video format (such as BT656 or DVI) to the flow-controlled Avalon-ST Video protocol. All Video and Image Processing Suite MegaCore functions (except the Line Buffer Compiler) transmit data using the Avalon-ST Video protocol, which allows an increased level of productivity through design flexibility and re-use.

The Clocked Video Input MegaCore function strips the incoming clocked video of horizontal and vertical blanking, leaving active picture data. Using this data with horizontal and vertical synchronization information, the MegaCore function creates the necessary Avalon-ST Video control and active picture packets.

With default parameterization, no conversion is done to the active picture data; the color plane information remains the same as in the clocked video format. However, in the V1 design, the Clocked Video Input MegaCore function is configured to accept SD-SDI SMPTE 259M (sequential 10-bit data—the least significant 10 bits of the 20-bit wide data received from the SDI MegaCore function), and output data in Avalon-ST Video (two 10-bit color planes in parallel). This allows the Clocked Video Input MegaCore function to support SD-SDI, HD-SDI and 3G-SDI data input at run-time.

The Clocked Video Input MegaCore function also provides clock-crossing capabilities that allow video formats running at different frequencies to enter the system. It also provides greater design flexibility by enabling the video processing system clock to be decoupled from the video input pixel clock. In the V1 design, the pixel clock and the system clocks are separate, both with a clock frequency of 148.5 MHz.

## Video Processing

Two SD-SDI, HD-SDI or 3G-SDI progressive/interlaced video streams are processed and mixed together with a test pattern background image as described in the following sections.

### Stream 1 (High Quality Format Conversion)

The SDI video stream input to connector `SDI_IN0` is formatted as either SD-SDI SMPTE 259M (Y'CbCr 4:2:2 10-bit wide data, alternating Cb Cr), HD-SDI (SMPTE 292M) or 3G-SDI SMPTE 424M (Y'CbCr 4:2:2 20-bit wide data, Y' and CbCr in parallel). The Clocked Video Input MegaCore function produces data in the format Y'CbCr 4:2:2, 10 bits per color plane, 2 colors in parallel for SD-SDI, HD-SDI, and 3G-SDI data.

The first processing function in the data path clips a rectangular region parameterized at run time using the control interface. For example, when NTSC video is input, a region of 720 pixels by 240 lines from each field, offset three lines from the top of the field is clipped. In this case, the Clipper MegaCore function outputs fields with an equal number of odd and even lines, for further processing.

The clipped video data is resampled to Y'CbCr 4:4:4 format by a Chroma Resampler MegaCore function before converting the color space to R'G'B' from Y'CbCr. The Color Space Converter MegaCore function also applies rounding (Round - Half Up), and outputs 8-bit wide data. The video is then streamed to the Deinterlacer MegaCore function.



The chroma resampling is applied before the motion adaptive deinterlacing because the motion adaptive algorithm requires the input color channels to have the same sampling rate.

The Deinterlacer MegaCore function is configured to accept both progressive and interlaced video. When the input video is in interlaced format, the motion adaptive algorithm produces a video stream in progressive format. When the input video is in progressive format, the data is output unprocessed. Note that the data is also buffered in external memory when in this mode, and supports frame rate conversion.

The progressive video stream is then scaled by the polyphase algorithm of the parameterizable Scaler MegaCore function (with 12 horizontal and 12 vertical taps). The Scaler MegaCore function is configured with an Avalon-MM slave control interface to allow run-time specification of the scaler output resolution. In addition, when the scaler ratio changes, software running on the Nios II processor calculates and reloads suitable coefficients for improved picture quality.

Prior to mixing the video stream with a background test pattern and a second video stream, the video data is buffered in external memory by the Frame Buffer MegaCore function. Buffering is required to smooth out the burstiness of the dataflow, due to the scaling and synchronization of the two streams input to the mixer.

### **Stream 1 (Lower Quality Format Conversion)**

The second video stream is configured identically to video stream 1 with the following exceptions:

- The Scaler MegaCore function is configured at compile time with a lower quality nearest neighbor algorithm and no coefficient reloading.
- The Deinterlacer MegaCore function is configured at compile time to deinterlace data by applying a weave algorithm.

### **Mixing the Video Streams**

The Avalon-ST Video output from the Test Pattern Generator MegaCore function and the two video streams are input to the Alpha Blending Mixer MegaCore function. The test pattern forms the background layer. The mixer is configurable via an Avalon-MM slave interface to allow run-time control of the following parameters:

- The x and y coordinates of each video stream relative to the background layer
- Enable and disable mixing of each video stream

Software running on the Nios II processor changes the parameters at run time when a viewing mode change, or output resolution change occurs.

The Avalon-ST Video data output from the mixer is transmitted to the Clocked Video Output MegaCore function before being output over DVI.

## **Video Output**

A video stream of progressive R'G'B' data is output from the DVI Tx port on the Stratix II GX audio video development board. The Clocked Video Output MegaCore function converts from the Avalon-ST Video protocol to clocked video formats (such as BT656 and DVI). It formats Avalon-ST Video into clocked video by inserting horizontal and vertical blanking and generating horizontal and vertical sync information using the Avalon-ST Video control and active picture packets. No conversion is done to the active picture data, the color plane information remains the same as in the Avalon-ST Video format.

The Clocked Video Output MegaCore function also provides clock-crossing capabilities to provide greater design flexibility by enabling the video processing system clock to be decoupled from the video output pixel clock.

The video frame is described using the mode registers that are accessed using the Avalon-MM control port on the Clocked Video Output MegaCore function. If you turn off **Use control port** in the MegaWizard interface for the Clocked Video Output MegaCore function, then the output video format always has the format specified in the MegaWizard interface.

The Clocked Video Output MegaCore function can be configured to support between 1 to 14 different modes and each mode has a bank of registers that describe the output frame. When the Clocked Video Output MegaCore function receives a new control packet on the Avalon-ST Video input, it searches the mode registers for a mode that is valid and has a field width and height that matches the width and height in the control packet. Both the register `VidModeMatch` and the signal `vid_mode_match` show the currently selected mode. Once found, the Clocked Video Output MegaCore function restarts the video output with those format settings. If a matching mode is not found, the video output format is unchanged and a restart does not occur.

In the V1 reference design, the clocked video output function is configured with three progressive video modes, 720×480 pixels, 1280×720 pixels, and 1920×1080 pixels.

In addition, the Clocked Video Output MegaCore function provides a queue where pixels can wait when the DVI output is in blanking and does not need pixel data. If this FIFO ever becomes full, then the flow controlled interface indicates that the clocked video output is not ready for data and earlier parts of the pipe are stalled.

## IP Configurations

This section provides information on the configuration of the IP components in the V1 design.

### SDI MegaCore Function

The SDI MegaCore function is configured as a triple-rate receiver serial digital interface. Two instances are required, one for each source. The SDI input clock frequency is 148.5/148.35 MHz for 3Gb/s (3G-SDI) or 74.25/74.175 MHz for 1.5Gb/s (HD-SDI) video inputs, or 27.0 MHz for SD-SDI video inputs. In this design, a clock frequency of 148.5 MHz is used which allows use of SD-SDI, HD-SDI and 3G-SDI input clocks.



For more information about the SDI MegaCore function, refer to the [SDI MegaCore Function User Guide](#).

### Clocked Video Input MegaCore Function

Two instances of the Clocked Video Input MegaCore function are required, one for each video stream. Both instances are configured as follows:

- Input of 20-bit wide video (two 10-bit color planes in parallel, Y' with alternating Cb and Cr), and syncs embedded in the video to support HD-SDI or 3G-SDI (SMPTE 292M/424M).

- The least significant 10 bits of 20-bit wide input data (two 10-bit color planes in sequence, Y' with alternating Cb and Cr), and syncs embedded in the video stream to support SD-SDI.
  - This is enabled by turning on **Allow color planes in sequence input** in the **Parameter Settings** GUI. The MegaCore function re-sequences the color planes to output the data as two 10-bit color planes in parallel.
- Output of two 10-bit color planes in parallel transmitted as Avalon-ST Video protocol.
- FIFO depth of one line of the maximum video line length supported (1920 pixels). The data is 20 bits wide.
- Run-time control is enabled by turning on **Use control port**. This provides an Avalon-MM slave interface, with interrupt support to indicate resolution changes. Status information, such as the image resolution, stability of video and FIFO fill level are exposed through the register map to the software control code.



For more information about the Clocked Video Input MegaCore function, refer to the *Video and Image Processing Suite User Guide*.

### Clipper MegaCore Function

Two instances of the Clipper MegaCore function are required, one for each video stream. Both instances are configured as follows:

- Support up to a maximum resolution of 1920×1080 pixels.
- A **Rectangle** clipping method to specify the width and height of the output video stream.
- Run-time control of the offset, width and height of the clipped rectangular region. This is enabled by turning on **Include Avalon-MM Interface** in the **Parameter Settings** GUI.
- Input of two 10-bit color planes in parallel, Y' with alternating Cb and Cr.
- Capable of clipping progressive (frames) or interlaced (fields) video.



For more information about the Clipper MegaCore function, refer to the *Video and Image Processing Suite User Guide*.

### Chroma Resampler MegaCore Function

Two instances of the Chroma Resampler MegaCore Function are required. Both instances are configured as follows:

- Input of two 10-bit color planes in parallel (Y' with alternating Cb and Cr), 4:2:2.
- Output of three 10-bit color planes in parallel, 4:4:4.
- Luma adaptive algorithm for horizontal resampling.



For more information about the Chroma Resampler MegaCore function, refer to the *Video and Image Processing Suite User Guide*.

### Color Space Converter MegaCore Function

Two instances of the Color Space Converter MegaCore function are required. Both instances are configured as follows:

- Input of three 10-bit color planes in parallel (Y'CbCr).
- Output of three 8-bit color planes in parallel (R'G'B').
- Y'CbCr: HDTV to Computer R'G'B' coefficients.



The Color Space Converter MegaCore function supports dynamic coefficient reload at run-time. However, this feature is not demonstrated in this reference design.



For more information about the Color Space Converter MegaCore function, refer to the *Video and Image Processing Suite User Guide*.

### Deinterlacer MegaCore Function

Two instances of the Deinterlacer MegaCore function are required. The MegaCore function in Video Stream 1 is configured as follows:

- High quality motion adaptive deinterlacing algorithm.
- Supports up to a maximum resolution of 1920×1080 pixels.
- Input of three 8-bit color planes in parallel (R'G'B').
- Support for interlaced video input up to a resolution of 1080i60.
- Support for progressive video input up to a resolution of 1080p60. This feature is enabled by turning on **Passthrough mode** in the **Parameter Settings** GUI.
- Triple-buffering with rate conversion to manage changes in the video data rate across the datapath, by dropping and repeating frames as appropriate.
- Separate clock domains to decouple the Avalon-MM master interfaces (which read/write data from/to the external memory controller) from the data processing function.



Higher memory bandwidth can be achieved using the built in clock-crossing support compared to using a separate clock crossing bridge.

- The Avalon-MM master port widths (for the five bursting read and write masters) are set to 256 bits. The masters are configured to read/write large bursts of data for each bus transaction (Burst target = 64).

The Deinterlacer MegaCore function in Video Stream 2 is configured identically to that in Video Stream 1 except that a weave deinterlacing algorithm is used.



For more information about the Deinterlacer MegaCore function, refer to the *Video and Image Processing Suite User Guide*.

## Scaler MegaCore Function

Two instances of the Scaler MegaCore function are required. The MegaCore function in Video Stream 1 is configured as follows:

- Polyphase scaling mode with 12 horizontal and 12 vertical taps, and Lanczos-2 filtering function.
- Input and output of three 8-bit color planes in parallel (R'G'B').
- Run-time control of the output image size up to a maximum resolution of 1920×1080 pixels using an Avalon-MM Slave interface.



In this design, software is provided to change the output resolution depending on the viewing mode or DVI output resolution.

- Run time coefficient calculation and reloading. As with all the Video and Image Processing Suite MegaCore functions in the design, the Scaler automatically configures itself to process the next input video frame by decoding the Avalon-ST Video control packet. When an input or output resolution change occurs, the ratio between the input frame and output frame changes. To retain a high quality scaled image, it is necessary to change the coefficients used in the scaling algorithm. The coefficient loading is performed through the Avalon-MM slave interface. This feature is enabled by turning on **Load coefficient data at runtime** in the **Parameter Settings** GUI.

The scaler in Video Stream 2 is configured identically to the scaler in Video Stream 1 except that a lower quality and lower cost nearest neighbor algorithm is used, and coefficient reloading is not supported.



For more information about the Scaler MegaCore function, refer to the *Video and Image Processing Suite User Guide*.

## Frame Buffer MegaCore Functions

Two instances of the Frame Buffer MegaCore function are required. Both instances are configured as follows:

- Input and output of three 8-bit color planes in parallel (R'G'B').
- 256-bit wide Avalon-MM read and write masters (for 64-bit DDR2 Memory interface).
- Neither frame dropping nor frame repeating is enabled. The change in data rate across the datapath input and output is handled by the Deinterlacer MegaCore function dropping and repeating frames. The Frame Buffer is required to smooth out the burstiness of the data flow.



Dropping and repeating frames at multiple points in a video pipeline will potentially result in a juddering effect, with multiple consecutive frames being dropped/repeated.

- The Avalon-MM master port widths (for the read and write masters) are set to 256 bits. The masters are configured to read/write large bursts of data for each bus transaction (Burst target = 64).



 For more information about the Frame Buffer MegaCore function, refer to the *Video and Image Processing Suite User Guide*.

### DDR2 SDRAM High Performance Controller MegaCore Function

This is the controller block for the external DDR2 SDRAM and is required as a buffer for the two Deinterlacer and the two Frame Buffers described above. It is configured as follows:


- Micron MT9HF6472AY-5EB38 (72-bit, 512MByte, 533MT/s, CL4, 266.7 MHz).
- Memory set up in Half-Rate mode (266.7 MHz internally, 133.35 MHz externally).
- Data width set to use 64 bits with a local data interface of 256 bits (due to half rate mode).

 For more information about the DDR2 SDRAM High Performance Controller MegaCore Function, refer to the *DDR and DDR2 SDRAM High Performance Controller User Guide*.

### Test Pattern Generator MegaCore Function

The Test Pattern Generator MegaCore function generates a standard color bar which is used as the background layer for the Alpha Blending Mixer MegaCore function. It is configured as follows:

- Output of three 8-bit color planes in parallel (R'G'B'), in progressive format.
- Run-time control of the output image size up to a maximum resolution of 1920×1080 pixels, using an Avalon-MM slave interface.


 The test pattern is surrounded by a single pixel black border to make vertical scrolling visible during system development.

 For more information about the Test Pattern Generator MegaCore function, refer to the *Video and Image Processing Suite User Guide*.

### Alpha Blending Mixer MegaCore Function

The Alpha Blending Mixer MegaCore function mixes the two video streams with a test pattern background. It is configured as follows:

- Three input streams (including the background layer).
- Each Avalon-ST source and sink is configured for three 8-bit color planes in parallel (R'G'B').
- Run-time control using an Avalon-MM slave interface including:
  - Output image size up to a maximum resolution of 1920×1080 pixels.

 As with all the Video and Image Processing Suite MegaCore functions in the reference design, the mixer automatically configures itself to process the next input video frame from each stream by decoding the Avalon-ST Video control packet from each input stream.

- Location of video streams relative to background layer.



- Disable/enable video streams.



For more information about the Alpha Blending Mixer MegaCore function, refer to the *Video and Image Processing Suite User Guide*.

## Nios II Processor

The Nios II Processor is configured as a Nios II/e core, clocked at 62.5 MHz. The processor's Avalon-MM data master can access the register map of many of the components in the V1 system, including a number of the Video and Image Processing Suite MegaCore functions and system peripherals. Figure 6 shows all the data master connections in the SOPC Builder patch panel view.

**Figure 6.** Data Master Connections in the SOPC Builder Patch Panel View

| Use                                 | Con... | Module Name   | Description                         | Clock       | Base       | End        | IRQ |
|-------------------------------------|--------|---|-------------------------------------|-------------|------------|------------|-----|
| <input checked="" type="checkbox"/> |        | <input checked="" type="checkbox"/> altmemddr         | DDR2 SDRAM High Performance Cont... | mem_clk     | 0x00000000 | 0x1fffffff |     |
| <input checked="" type="checkbox"/> |        | <input checked="" type="checkbox"/> my_alt_vip_cti_1  | Clocked Video Input                 | vip_clk     | 0x00204200 | 0x002042ff | 0   |
| <input checked="" type="checkbox"/> |        | <input checked="" type="checkbox"/> my_alt_vip_clip_1 | Clipper                             | vip_clk     | 0x00204300 | 0x002043ff |     |
| <input checked="" type="checkbox"/> |        | <input checked="" type="checkbox"/> my_alt_vip_crs_1  | Chroma Resampler                    | vip_clk     |            |            |     |
| <input checked="" type="checkbox"/> |        | <input checked="" type="checkbox"/> my_alt_vip_csc_1  | CSC                                 | vip_clk     |            |            |     |
| <input checked="" type="checkbox"/> |        | <input checked="" type="checkbox"/> pipeline_bridge_1 | Avalon-MM Pipeline Bridge           | altmemdd... | 0x00000000 | 0x1fffffff |     |
| <input checked="" type="checkbox"/> |        | <input checked="" type="checkbox"/> my_alt_vip_dil_1  | Deinterlacer                        | multiple    |            |            |     |
| <input checked="" type="checkbox"/> |        | <input checked="" type="checkbox"/> my_alt_vip_scl_1  | Scaler                              | vip_clk     | 0x00203800 | 0x00203fff |     |
| <input checked="" type="checkbox"/> |        | <input checked="" type="checkbox"/> pipeline_bridge   | Avalon-MM Pipeline Bridge           | altmemdd... | 0x00000000 | 0x1fffffff |     |
| <input checked="" type="checkbox"/> |        | <input checked="" type="checkbox"/> my_alt_vip_vfb_1  | Frame Buffer                        | multiple    |            |            |     |
| <input checked="" type="checkbox"/> |        | <input checked="" type="checkbox"/> my_alt_vip_cti_2  | Clocked Video Input                 | vip_clk     | 0x00204000 | 0x002040ff | 1   |
| <input checked="" type="checkbox"/> |        | <input checked="" type="checkbox"/> my_alt_vip_clip_2 | Clipper                             | vip_clk     | 0x00204100 | 0x002041ff |     |
| <input checked="" type="checkbox"/> |        | <input checked="" type="checkbox"/> my_alt_vip_crs_2  | Chroma Resampler                    | vip_clk     |            |            |     |
| <input checked="" type="checkbox"/> |        | <input checked="" type="checkbox"/> my_alt_vip_csc_2  | CSC                                 | vip_clk     |            |            |     |
| <input checked="" type="checkbox"/> |        | <input checked="" type="checkbox"/> pipeline_bridge_2 | Avalon-MM Pipeline Bridge           | altmemdd... | 0x00000000 | 0x1fffffff |     |
| <input checked="" type="checkbox"/> |        | <input checked="" type="checkbox"/> my_alt_vip_dil_2  | Deinterlacer                        | multiple    |            |            |     |
| <input checked="" type="checkbox"/> |        | <input checked="" type="checkbox"/> my_alt_vip_scl_2  | Scaler                              | vip_clk     | 0x00204500 | 0x002045ff |     |
| <input checked="" type="checkbox"/> |        | <input checked="" type="checkbox"/> my_alt_vip_vfb_2  | Frame Buffer                        | multiple    |            |            |     |
| <input checked="" type="checkbox"/> |        | <input checked="" type="checkbox"/> my_alt_vip_tpg    | Test Pattern Generator              | vip_clk     | 0x00204800 | 0x002048ff |     |
| <input checked="" type="checkbox"/> |        | <input checked="" type="checkbox"/> my_alt_vip_mix    | Alpha Blending Mixer                | vip_clk     | 0x00203000 | 0x002037ff |     |
| <input checked="" type="checkbox"/> |        | <input checked="" type="checkbox"/> my_alt_vip_itc    | Clocked Video Output                | vip_clk     | 0x00200000 | 0x00201fff | 2   |
| <input checked="" type="checkbox"/> |        | <input checked="" type="checkbox"/> cpu               | Nios II Processor                   |             |            |            |     |
|                                     |        | instruction_master                                    | Avalon Memory Mapped Master         | cpu_clk     |            |            |     |
|                                     |        | data_master   | Avalon Memory Mapped Master         |             |            |            |     |
|                                     |        | jtag_debug_module                                     | Avalon Memory Mapped Slave          |             |            |            |     |
| <input checked="" type="checkbox"/> |        | <input checked="" type="checkbox"/> tristate_bridge   | Avalon-MM Tristate Bridge           | cpu_clk     | 0x00202800 | 0x00202fff | 31  |
| <input checked="" type="checkbox"/> |        | <input checked="" type="checkbox"/> ssram             | Cypress CY7C1380C SSRAM             | cpu_clk     | 0x00000000 | 0x001fffff |     |
| <input checked="" type="checkbox"/> |        | <input checked="" type="checkbox"/> sysid             | System ID Peripheral                | cpu_clk     | 0x00204880 | 0x002048bf |     |
| <input checked="" type="checkbox"/> |        | <input checked="" type="checkbox"/> jtag_uart         | JTAG UART                           | cpu_clk     | 0x002048c0 | 0x002048ff | 3   |
| <input checked="" type="checkbox"/> |        | <input checked="" type="checkbox"/> timer             | Interval Timer                      | cpu_clk     | 0x00204100 | 0x002041ff | 4   |
| <input checked="" type="checkbox"/> |        | <input checked="" type="checkbox"/> dip               | PIO (Parallel I/O)                  | cpu_clk     | 0x00204580 | 0x002045ff |     |
| <input checked="" type="checkbox"/> |        | <input checked="" type="checkbox"/> leds              | PIO (Parallel I/O)                  | cpu_clk     | 0x00204680 | 0x002046ff |     |
| <input checked="" type="checkbox"/> |        | <input checked="" type="checkbox"/> buttons           | PIO (Parallel I/O)                  | cpu_clk     | 0x00204600 | 0x002046ff |     |
| <input checked="" type="checkbox"/> |        | <input checked="" type="checkbox"/> flow              | PIO (Parallel I/O)                  | cpu_clk     | 0x00204700 | 0x002047ff |     |
| <input checked="" type="checkbox"/> |        | <input checked="" type="checkbox"/> rxstd             | PIO (Parallel I/O)                  | cpu_clk     | 0x00204780 | 0x002047ff |     |

The Nios II processor executes the control software for the system as described in “Nios II Software” on page 26, providing a highly configurable software design flow.

## Clocked Video Output MegaCore Function

The Clocked Video Output MegaCore function is configured as follows:

- 24-bit R'G'B' output, on separate wires, for transmission over DVI.
- Avalon-ST Video protocol input.
- FIFO depth of one line of the maximum video line length supported (1920 pixels).
- Run-time control is enabled by turning on **Use control port** in the **Parameter Settings** GUI. This provides an Avalon-MM slave interface.
- Three run-time configuration video modes to allow run-time switching between different output resolutions. The resolution, sync and blanking data for each mode is loaded from software executed on the Nios II processor, using the Avalon-MM slave interface.



In this reference design, 1080p60, 720p60 and 480p60 are demonstrated.

- Clock-crossing between the system clock and the pixel clock which is enabled when **Video in and out use the same clock** is turned off in the **Parameter Settings** GUI.
- Status information, such as underflow status and FIFO fill level is exposed through the register map to the software control code.



For more information about the Clocked Video Output MegaCore function, refer to the *Video and Image Processing Suite User Guide*.

## DVI TX Controller

The DVI TX Controller controls the DVI transmitter block on the Stratix II GX audio video development board to output the video stream. This block is configured as follows:

- 24-bit (R'G'B') data input and 12-bit data output with positive and negative clocks.
- Direct connection to Clocked Video Output MegaCore function.
- Runtime changeable display resolution.

## System Peripherals

The system contains several useful memory-mapped peripheral and parallel I/O components to provide information on the status of the design. These include:

- A JTAG UART to display software `printf` output.
- Push buttons configured to allow switching between viewing modes and DVI output resolutions (refer to “*Output Resolution*” on page 19 and “*Viewing Mode*” on page 20).
- Dual in-line package (DIP) switches (not used).
- LEDs for system status (refer to “*Board LEDs Status Information*” on page 21).
- Quad seven-segment display to show the standard of the input video streams (refer to “*Quad Seven-Segment Display Status Information*” on page 21).

## Clock Domains

The video datapath is clocked by the system clock `vip_clk` at 148.5 MHz. This allows the processing functions to process progressive frames of video with resolutions up to 1920×1080 pixels at a rate of 60 frames per second.

The Nios II processor, which executes the software that configures the video processing functions, is clocked at a lower clock rate of 62.5 MHz.

The DDR2 memory is run at its maximum rate of 266 MHz. with the memory controller run in half-rate mode clocked at 133 MHz. The Deinterlacer and the Frame Buffer MegaCore functions de-couple the data processing clock rate (148.5 MHz) from the memory controller clock domain (133.33 MHz).

The Clocked Video Input and Clocked Video Output MegaCore functions provide clock domain crossing which allows the DVI output and SDI input to run at the speed of the relevant standard being used.

## Run Time Resolution Changes

You can make the following changes at run time:

- The resolution of the input video streams
- The output resolution and viewing modes. (Using the push-buttons on the Stratix II GX audio video development board.)

### Input Resolution

The Clocked Video Input MegaCore function retains a count of the height, width and format (progressive or interlaced) of the input video, and detects changes to the resolution or format. After stable video is captured, the Clocked Video Input MegaCore function generates control packets containing the new resolution and progressive/interlaced format. The control packets propagate through each function in the data path, with each MegaCore function configuring itself ready to receive the new video data. The Clocked Video Input MegaCore function also generates an interrupt when a resolution change occurs, with the interrupt line connected to the Nios II processor. When an interrupt is generated, the Nios II interrupt service routine performs the following functions:

- Calculate new coefficients based on the new scaling ratio
- Writes new clipping area parameters
- Writes new scaling coefficients to the scaler control interface

### Output Resolution

The PB1 push-button switch on the Stratix II GX audio video development board can be used to change the output resolution on the display.

Pressing PB1 several times cycles round the output resolutions. The supported resolutions are:

- 1920×1080 pixels @ 60 Hz
- 1280×720 pixels @ 60 Hz
- 720×480 pixels @ 60 Hz

## Viewing Mode

The PB0 push-button switch on the Stratix II GX audio video development board changes the viewing mode on the display.

Pressing PB0 several times cycles round the viewing mode. The supported modes are:

- Multi-viewer
- Stream 1 scaled up to output resolution
- Stream 2 scaled up to output resolution

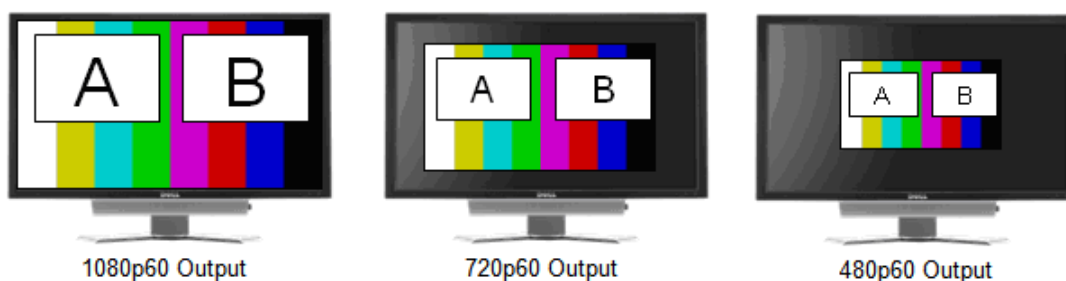


A monitor capable of displaying a 1920×1080 pixel resolution is required. The monitor should be configured to display the video without scaling to the native resolution (1:1 pixel mapping).

## Multi-Viewer Mode

In multi-viewer mode, the two input video streams are format converted, scaled to one third of the output resolution, mixed with the test pattern background image, and displayed side-by-side as shown in Figure 7. The scaling output resolution, scaler coefficient generation and re-load, and location of the video stream relative to the background test pattern are controlled by the software executed on the Nios II processor. Figure 7 shows the multi-viewer mode display for each output resolution.

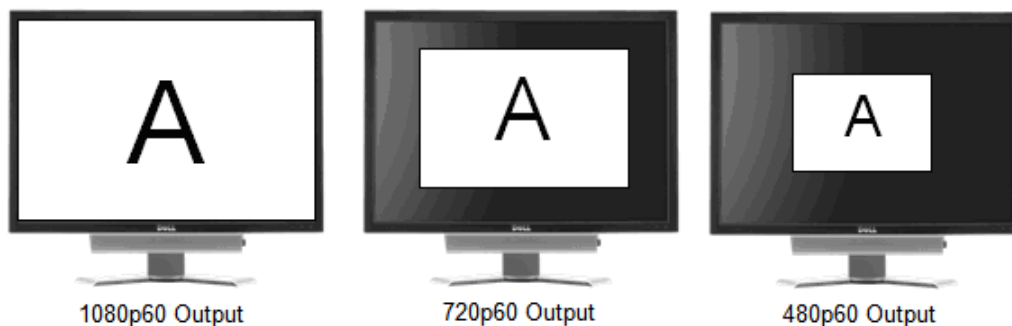
**Figure 7.** Multi-Viewer Mode



## Stream 1 Scaled Up To Output Resolution

In this mode, the first input stream is format converted and scaled to the output resolution. Figure 8 shows this viewing mode for each output resolution.

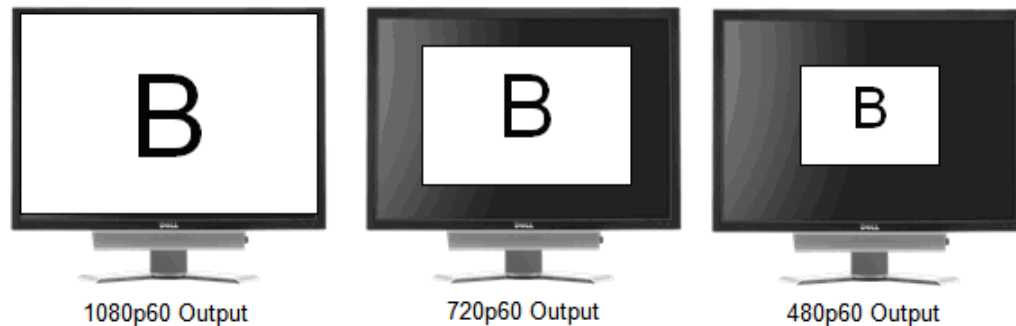
**Figure 8.** Stream 1 Scaled Up To Output Resolution



### Stream 2 Scaled Up To Output Resolution

In this mode, the second input stream is format converted and scaled to the output resolution. [Figure 9](#) shows this viewing mode for each output resolution.

**Figure 9.** Stream 2 Scaled Up To Output Resolution



### Board LEDs Status Information

The LEDs on the Stratix II GX audio video development board provide the status information listed in [Table 3](#).

**Table 3.** Board LED Status Information

| LED | Status   |
|-----|--|
| 0   | Overflow at the input or underflow at the output has occurred.                 |
| 1   | Video stream 1 is active.  |
| 2   | Video stream 2 is active.  |
| 3   | Heartbeat (flashes if the software is running).                                |
| 4   | The viewing mode is <b>Video Stream 1 Scaled Up</b> . <a href="#">(Note 1)</a> |
| 5   | The viewing mode is <b>Video Stream 2 Scaled Up</b> . <a href="#">(Note 1)</a> |
| 6   | The output resolution is 1280×720 pixels. <a href="#">(Note 2)</a>             |
| 7   | The output resolution is 720×480 pixels. <a href="#">(Note 2)</a>              |

**Notes to [Table 3](#):**

- (1) When neither LED4 or LED5 is on, the viewing mode is **Multiviewer**.
- (2) When neither LED6 or LED7 is on, the output resolution is 1920×1080.

### Quad Seven-Segment Display Status Information

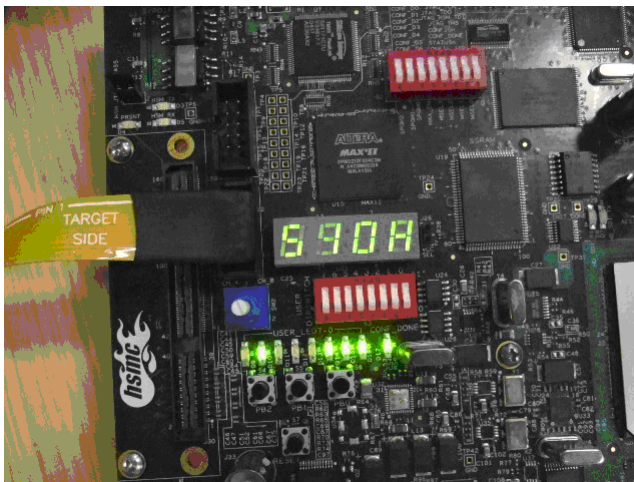
The quad seven-segment display on the Stratix II GX audio video development board provide information about the input standard as listed in [Table 3](#).

**Table 4.** Quad Seven-Segment Display Status Information

| Segment | Status   |
|---------|--|
| 0       | Video Stream 1 standard received (S = SD-SDI, H = HD-SDI, 3 = 3G-SDI)                          |
| 1       | Video Stream 1 Clock rate (3 = 148.5 MHz, 2 = 148.35 MHz, 1 = 74.25 MHz, 0 = 74.175 MHz) or SD |
| 2       | DVI Output standard (0 = 60 Fps, 1 = 59.94 Fps)  |
| 3       | Video Stream 2 standard received (S = SD-SDI, H = HD-SDI, 3 = 3G-SDI)                          |

For example, the seven-segment display in [Figure 10](#) displays S, 1, 0, H which means high definition video on stream 1, at 74.175 MHz clock rate, with 59.94 frames per second (Fps) DVI output and standard definition video on stream 2.

**Figure 10.** Quad Seven-Segment Display Showing Input Video Standard



## External Memory Bandwidth Calculations

[Table 5](#) summarizes the maximum bandwidth requirement for each MegaCore function that accesses external DDR2 memory.

**Table 5.** MegaCore Function Bandwidth Requirements

| MegaCore Function            | Maximum Input Rate   | Maximum Output rate  | Master Type                             | Maximum Bandwidth |
|------------------------------|--|--|---|-------------------|
| Motion Adaptive Deinterlacer | (1080p60)<br>$1920 \times 1080 \times 24 \text{ bits} \times 60$<br>= 2.986 Gbps<br>(progressive pass through) | (1080p60)<br>$1920 \times 1080 \times 24 \text{ bits} \times 60$<br>= 2.986 Gbps | 1 × write at input rate                 | 2.986 Gbps        |
|                              |  |  | 2 × read at output rate                 | 5.972 Gbps        |
|                              |  |  | 1 motion data read at half output rate  | 1.493 Gbps        |
|                              |  |  | 1 motion data write at half output rate | 1.493 Gbps        |
| Weave Deinterlacer           | (1080p60)<br>$1920 \times 1080 \times 24 \text{ bits} \times 60$<br>= 2.986 Gbps<br>(progressive pass through) | (1080p60)<br>$1920 \times 1080 \times 24 \text{ bits} \times 60$<br>= 2.986 Gbps | 1 × write at input rate                 | 2.986 Gbps        |
|                              |  |  | 1 × read at output rate                 | 2.986 Gbps        |
| Frame Buffer (Stream 1)      | (1080p60)<br>$1920 \times 1080 \times 24 \text{ bits} \times 60$<br>= 2.986 Gbps                               | (1080p60)<br>$1920 \times 1080 \times 24 \text{ bits} \times 60$<br>= 2.986 Gbps | 1 × write at input rate                 | 2.986 Gbps        |
|                              |  |  | 1 × read at output rate                 | 2.986 Gbps        |
| Frame Buffer (Stream 1)      | (1080p60)<br>$1920 \times 1080 \times 24 \text{ bits} \times 60$<br>= 2.986 Gbps                               | (1080p60)<br>$1920 \times 1080 \times 24 \text{ bits} \times 60$<br>= 2.986 Gbps | 1 × write at input rate                 | 2.986 Gbps        |
|                              |  |  | 1 × read at output rate                 | 2.986 Gbps        |

The maximum memory bandwidth achieved is when the maximum input resolution is viewed in single view mode. The maximum total bandwidth is then the sum of the bandwidths for the motion adaptive and (for the write master only) the weave Deinterlacer MegaCore functions and the Frame Buffer Megacore function in Video stream 1.

$$\begin{aligned}\text{MaxBandwidth} &= \text{MotionAdaptiveDeinterlacer} + \text{WeaveDeinterlacer} + \text{FrameBuffer} \\ &= 11.94 \text{ Gbps} + 2.986 \text{ Gbps} + 5.972 \text{ Gbps} = 20.90 \text{ Gbps}\end{aligned}$$



In single view mode, the frame buffer on Video Stream 2 does not access external memory because the stream input to the mixer is disabled by the software executed on the Nios II processor.

The Stratix II GX audio video development board when used with the Micron MT9HTF6472AY- 53EB3 high-performance DDR2 SDRAM provides a maximum theoretical bandwidth of:

$$266.7 \text{ MHz} \times 64 \text{ bits} \times 2 \text{ (both clock edges used)} = 34.133 \text{ Gbps}$$

This results in a memory access efficiency requirement of 61%.

The memory bandwidth efficiency is determined by a number of factors, such as randomness of addresses, refresh rate, turnaround times between reads and writes, and burst lengths. Altera's memory controllers can reach an efficiency of up to about 90% if the access conditions are right (long bursts of writes to the same column followed by long bursts of reads).

Using a half-rate memory controller to satisfy the memory bandwidth requirements means that the local interface width between memory controller and internal FPGA logic is 256 bits (= 4 × 64 bits). Both the DDR2 memory and memory controller run at 266 MHz, while the internal FPGA blocks run at half this rate, 133 MHz.

## Reviewing the V1 Reference Design

This section is a walkthrough that demonstrate how to construct a video processing application using the Altera video and image processing framework. This includes a description of the top level design file in the Quartus II software, the full hardware system in SOPC Builder, and the configuration and control software code in the Nios II IDE environment.

To review the complete reference design, perform the following steps:

1. Run the Quartus II software to ensure the `QUARTUS_ROOTDIR` environment variable is correctly set.
2. Close the Quartus II software.
3. In Windows Explorer, browse to the install directory.
4. Double-click on **make\_project\_V1.bat** to copy the **V1.sopc** and **config.v** file to the top level, and create the quartus project **s2gxav.qpf** and **s2gxav.qsf**.



## Quartus II Top Level

To review the top level Quartus II system file, perform the following steps:

1. Launch the Quartus II software.
2. On the File menu in the Quartus II software, click **Open Project**, browse to the *<V1 install directory>* and open the Quartus II project file: **s2gxav.qpf**.
3. On the File menu, click **Open**, browse into the **top** subdirectory and open the top level verilog file **s2gxav.v**.

The top level verilog file **s2gxav.v** instantiates the following modules:

- Phase Locked Loop (PLL) module to generate clocks for different DVI output standards (SD, HD and 3 Gbps).
- PLL reconfiguration and control modules to allow reconfiguration of the PLL, for the DVI output, at runtime.
- DVI output driver module. The DVI output driver module controls the DVI transmitter block on the Stratix II GX audio video development board to output the video stream. This block provides:
  - Configurable run-time resolution and clock frequency, supporting resolutions up to 1080p60.
  - Support for 24-bit (R'G'B') data input and 12-bit data output.
  - Interface to Clocked Video Output MegaCore function.
- Two SDI modules configured in triple rate mode to receive data input in the SD-SDI, HD-SDI, or 3G-SDI standard.
- Quad seven-segment display configuration module to display video standard input and system status.
- A onewire interface handling clock multiplexing, switch input and LED output.
- SOPC Builder system (V1).

The Quartus II project also contains the following timing constraint files: **s2gxav.sdc**, **altmemddr\_phy\_ddr\_timing.sdc**, **alt\_vip\_cvi.sdc**, and **alt\_vip\_cvo.sdc**.

## SOPC Builder System

To review the SOPC Builder system, perform the following steps:

1. Launch SOPC Builder by clicking **SOPC Builder** on the Tools menu in the Quartus II software, with the reference design project open.

The complete SOPC Builder is shown in [Figure 11 on page 25](#).

The system contains the following fully parameterizable components:

- Video processing and buffering functions (Video and Image Processing Suite), Video Stream 1, Video Stream 2 and Video Output in [Figure 11](#).
- DDR2 external memory controller.
- Nios II processor for system configuration and control.
- Peripheral and Parallel I/O components.



- Bridge components (Pipeline and tri-state bridges).

All components in the SOPC Builder system are connected by either Avalon-MM or Avalon-ST interfaces. The Clocked Video Input and Clocked Video Output MegaCore functions form the boundary of the video processing datapath, exporting signals for connection to video interfaces (SDI and DVI) at the top level.

**Figure 11.** Complete SOPC Builder System for the V1 Reference Design

|                        | Module Name       | Description                            | Clock            |
|------------------------|-------------------|--|------------------|
| Video Stream 1         | altmemddr         | DDR2 SDRAM High Performance Controller | mem_clk          |
|                        | my_alt_vip_cti_1  | Clocked Video Input                    | vip_clk          |
|                        | my_alt_vip_clip_1 | Clipper                                | vip_clk          |
|                        | my_alt_vip_crs_1  | Chroma Resampler                       | vip_clk          |
|                        | my_alt_vip_csc_1  | CSC                                    | vip_clk          |
|                        | pipeline_bridge_1 | Avalon-MM Pipeline Bridge              | altmemddr_sysclk |
|                        | my_alt_vip_dil_1  | Deinterlacer                           | multiple         |
|                        | my_alt_vip_scl_1  | Scaler                                 | vip_clk          |
| Video Stream 1         | pipeline_bridge   | Avalon-MM Pipeline Bridge              | altmemddr_sysclk |
|                        | my_alt_vip_vfb_1  | Frame Buffer                           | multiple         |
|                        | my_alt_vip_cti_2  | Clocked Video Input                    | vip_clk          |
|                        | my_alt_vip_clip_2 | Clipper                                | vip_clk          |
|                        | my_alt_vip_crs_2  | Chroma Resampler                       | vip_clk          |
|                        | my_alt_vip_csc_2  | CSC                                    | vip_clk          |
|                        | pipeline_bridge_2 | Avalon-MM Pipeline Bridge              | altmemddr_sysclk |
|                        | my_alt_vip_dil_2  | Deinterlacer                           | multiple         |
| Video Output Processor | my_alt_vip_scl_2  | Scaler                                 | vip_clk          |
|                        | my_alt_vip_vfb_2  | Frame Buffer                           | multiple         |
|                        | my_alt_vip_tpg    | Test Pattern Generator                 | vip_clk          |
|                        | my_alt_vip_mix    | Alpha Blending Mixer                   | vip_clk          |
| Peripherals            | my_alt_vip_itc    | Clocked Video Output                   | vip_clk          |
|                        | cpu               | Nios II Processor                      | cpu_clk          |
|                        | tristate_bridge   | Avalon-MM Tristate Bridge              | cpu_clk          |
|                        | ssram             | Cypress CY7C1380C SSRAM                | cpu_clk          |
|                        | sysid             | System ID Peripheral                   | cpu_clk          |
|                        | jtag_uart         | JTAG UART                              | cpu_clk          |
|                        | timer             | Interval Timer                         | cpu_clk          |
|                        | dip               | PIO (Parallel I/O)                     | cpu_clk          |
|                        | leds              | PIO (Parallel I/O)                     | cpu_clk          |
|                        | buttons           | PIO (Parallel I/O)                     | cpu_clk          |
|                        | flow              | PIO (Parallel I/O)                     | cpu_clk          |
|                        | rxstd             | PIO (Parallel I/O)                     | cpu_clk          |

- To review the configuration of the IP components in SOPC Builder, select the IP module name (for example **my\_alt\_vip\_scl\_1**) and click **Edit**. This displays the corresponding MegaWizard interface **Parameter Settings** GUI page.
- In SOPC Builder, generate the SOPC Builder system by clicking on **Generate**. Progress messages are issued in the SOPC Builder System Generation window and should complete with a message:
 

```
Info: System generation was successful
```
- Close SOPC Builder and click **Start Compilation** on the Processing menu to compile the Quartus II project.

## Nios II Software

The V-Series of reference designs are highly configurable at run time by software executing on a Nios II processor.

The C++ source code provided performs the following functions:

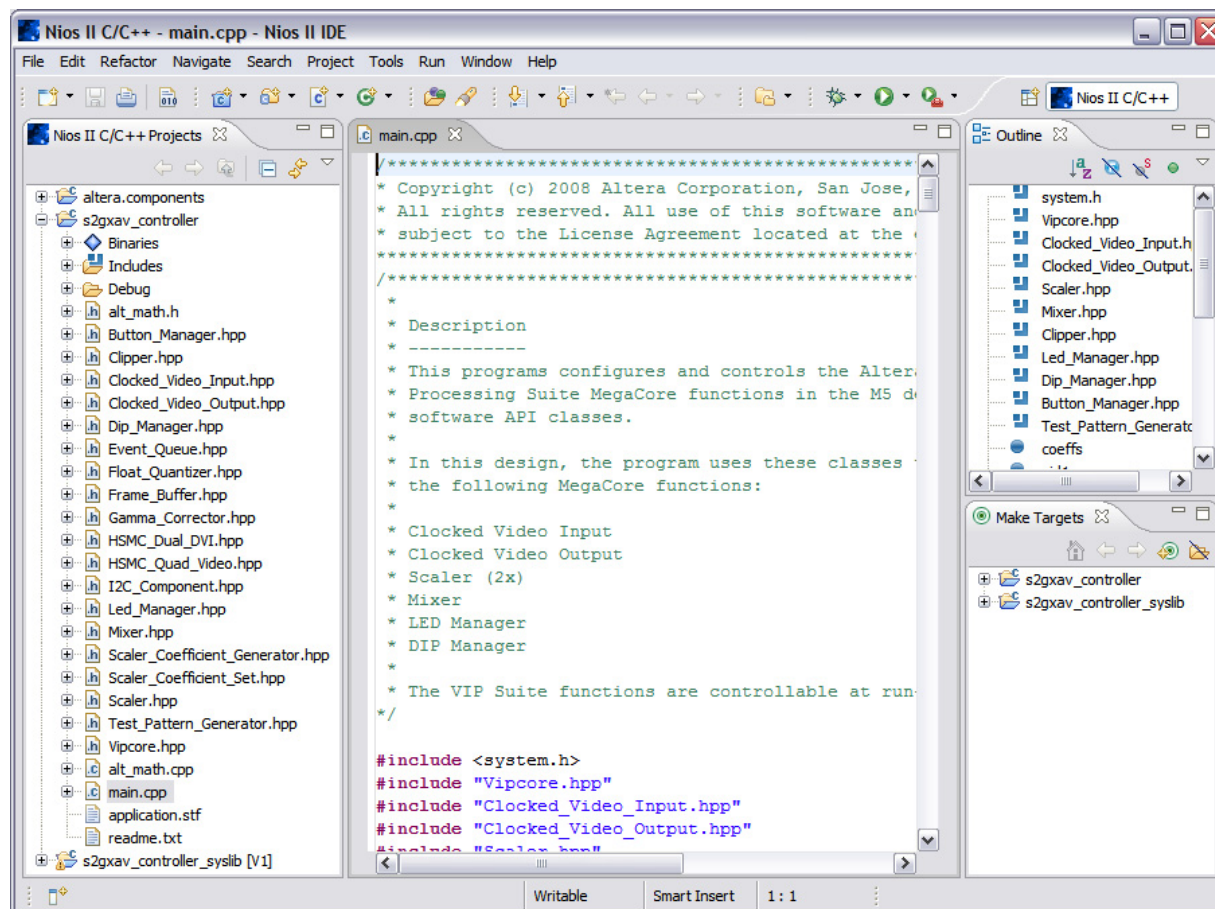
- Initializes the Video and Image processing Suite MegaCore functions:
  - Clocked Video Inputs to generate an interrupt on stable resolution changes.
  - Test Pattern Generator to initial output resolution.
  - Mixer with layers disabled.
  - Clocked Video Output with the resolution, sync and blanking data for the three supported output modes (1080p60, 720p60, 480p60).
  - Starts all run time controllable functions.
- Configures board LEDs to provide status information. For example to show that the software is running, overflow or underflow has occurred, the current display mode, and so on. (Refer to “[Board LEDs Status Information](#)” on page 21 for more information.)
- Manages interrupts and button presses with event and button manager classes.
- Manages mode switching triggered by button presses. (Refer to “[Run Time Resolution Changes](#)” on page 19). These changes include enabling/disabling mixer layers, setting mixer co-ordinates, setting scaler output resolutions.
- Sets the scaler output resolution and automatically calculates and reloads scaler coefficients based on resolution changes.
- Sets the clipper regions based on the video standard. For example, if the resolution detected is NTSC, a rectangle of 720×240 pixels is clipped from the interlaced video, with an offset of three lines from the top of the input stream.

C++ classes are included in the **software/s2gxav\_controller** directory that provide a software API between the Nios II control code and the Video and Image Processing Suite MegaCore functions as well as peripherals and board components (such as DIP Switches, buttons, LEDs, and JTAG UART). The classes provide many member functions to accelerate software development and increase visibility of the data flow. For example, the clocked video input class (**Clocked\_Video\_Input.hpp**) member functions can report the level in a FIFO in the video system, or the member functions in the frame buffer class (**Frame\_Buffer.hpp**) can report the number of frames that have been dropped or repeated by the Frame Buffer MegaCore function in the data path.

All Video and Image Processing Suite MegaCore function classes are derived from the base class **Vipcore.hpp** which contains methods common to all functions such as starting and stopping the video function processing at a frame boundary.

The main function in **main.cpp** demonstrates how to use the C++ class member functions to configure and control the data path functions.

[Figure 12 on page 27](#) shows the Nios II IDE environment and Nios II application project source files.

**Figure 12.** Nios II IDE Environment and Application Project Source Files

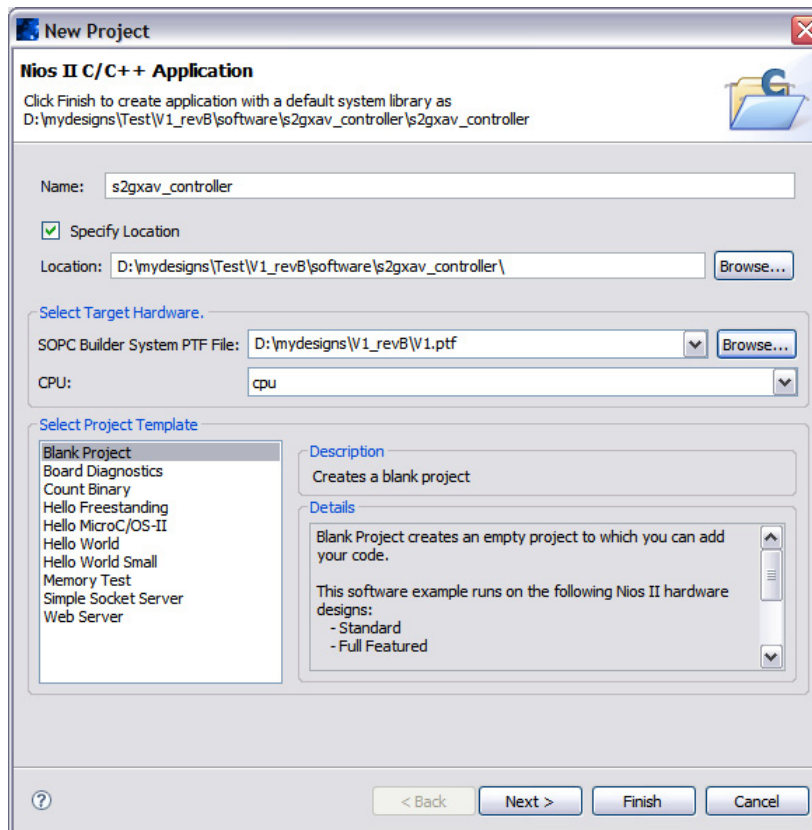
### Building the Software in the Nios II IDE

Perform the following steps to build the software in the Nios II Integrated Development Environment (IDE):

1. Start the Nios II IDE, v8.1 software.
2. Click **Switch Workspace** on the File menu and browse to the **software** subdirectory of the V1 design install directory.
3. Click **OK** to create a new workspace.
4. When the Nios IDE has restarted, click the **Workbench** icon.
5. On the File menu, point to **New** and click **Nios II C/C++ Application**.
6. In the **New Project** dialog box (Figure 13 on page 28):
  - a. Select **Blank Project** as the **Project Template**.
  - b. Type `s2gxav_controller` in the **Name** field.
  - c. Turn on **Specify Location** and type in the path to the directory `<install directory>\V1_<revision>\software\s2gxav_controller`.

- d. Browse to the SOPC Builder System PTF File **V1.ptf** (in the **V1\_<revision>** directory).
- e. Click **Finish**.

**Figure 13.** Nios II IDE New Project Dialog Box



7. Verify that the application project **s2gxav\_controller** appears in the **Nios II C/C++ Projects** list.
8. Browse the application source code files listed below **s2gxav\_controller**.
9. To configure the System Library project, right-click on the **s2gxav\_controller** project and click **System Library Properties**.
10. In the **System Library** dialog box:
  - a. Verify that **Program never exits, Clean exit (flush buffers), Support C++** and **Reduced device drivers** are turned on.
  - b. Click **OK**.
11. To program the Nios II application executable to SRAM from the Nios II IDE, right-click on the **s2gxav\_controller** project, point to **Run As** and click **Nios II Hardware**.



Altera recommends that you review the **.hpp** files included in the application project to quickly understand the control capability from the Nios II software environment.

## Setting Up the Hardware and Configuring the FPGA

To set up the Stratix II GX audio video development board, perform the following steps:

1. Remove power from the development board by disconnecting the power cable.
2. Connect one end of the USB cable to the USB port on your PC.
3. Connect the other end to the 10-pin header labelled SYSTEM\_JTAG on the development board.
4. Connect an SDI video source cable to the BNC input connector labelled SDI\_IN0 (for high quality processing).
5. Connect a second SDI video source cable to the BNC input connector marked SDI\_IN1 (for lower quality processing).

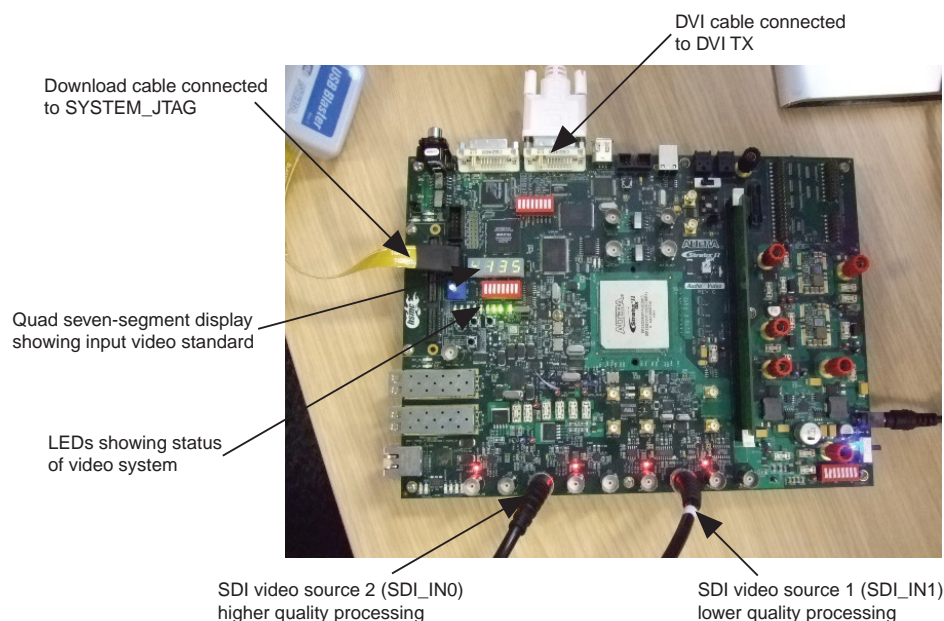


The design automatically detects the input video streams and produces output when 0, 1, or 2 video sources are active. When 0 video sources are active, the test pattern is output.

6. Connect one end of the DVI cable to a DVI monitor, capable of 1920×1080 @ 60Hz. Connect the other end to the DVI Tx connector on the development board.
7. Re-apply power to the development board.

Figure 14 shows the completed connections to the Stratix II GX audio video development board.

**Figure 14.** Stratix II GX Audio Video Development Board Connections.



For details of installing the USB Blaster software driver on the host PC (located at `<quartus_install_dir>\drivers\usb-blaster`), refer to the [USB-Blaster Download Cable User Guide](#).



You can configure the Stratix II GX90 device by downloading the SRAM object file (.sof) image to the development board. To do so, perform the following steps:

1. In the Quartus II software, choose **Programmer** from the Tools menu.
2. In the **Mode** list of the **Programming** window, verify that **JTAG** is selected.
3. Click **Hardware Setup** to configure the programming hardware.
4. Verify that the **Hardware Setup** dialog box appears.
5. In the **Hardware** column, select **USB Blaster**.
6. Click **Close** to exit the **Hardware Setup** window.
7. In the **Programming** window, click **Add File**.
8. Select the file **s2gxav.sof** and click **Open**.
9. In the **Programmer** window, turn on **Program/Configure** on the same line as **s2gxav.sof**.
10. Click **Start**.

The programmer begins to download the configuration data to the FPGA. The **Progress** field displays the percentage of data that is downloaded. A message appears when the configuration is complete.



No video appears on the screen until the software executable has been downloaded to SRAM. Refer to [“Downloading the Nios II Software”](#).

## Downloading the Nios II Software

To download the Nios II executable to SRAM, from a Nios II Command Shell perform the following steps:

1. Launch the Nios II Command Shell (**Start->All Programs->Altera->Nios II EDS 8.1->Nios II Command Shell**).
2. Change directory to `<install>\V1_rev<revision>\` containing **s2gxav\_controller.elf**



If you have re-built your software program, change directory to the appropriate executable and linkable format file (.elf) file.

3. Enter the following command:

```
nios2-download -r -g s2gxav_controller.elf; nios2-terminal
```

Verify that a test pattern background and video stream(s) display on the monitor as shown in [Figure 15 on page 31](#).

**Figure 15.** Reference Design Output Video

## Troubleshooting

This section describes some known problems that may occur and suggested solutions.

### Error When Re-Compiling the Design

1. When re-compiling the design in the Quartus II software, compilation fails with an error:

Error: Node instance "sdi\_megacore\_top\_inst" instantiates undefined entity "sdi\_megacore\_top"

**Solution:** The library path to the SDI MegaCore function in the Quartus II software is incorrect. Update the project library path to point to the correct SDI MegaCore function **altera/sdi/lib directory** (**Assignments->Libraries->Project Libraries->Add**). Remove any incorrect paths by selecting the path and selecting **Remove**.

2. When re-compiling the design in Quartus II compilation fails with the error:

Error: VHDL Use Clause error at \*\_GN.vhd(8): design library "altera" does not contain primary unit "alt\_cusp81\_package"

**Solution:** Remove the project **db** directory and re-compile. This issue will be fixed in a future version of the tools.

### Output Video Does Not Appear on Display

The output video doesn't appear on the display after downloading the Nios II .elf file.

**Solution:** Press the reset button (**RESET**).

## Delay Between a Change of Input and Output

Coefficient calculation is performed at run time so there may be a slight delay between a change of input format and the output video becoming sharp.

**Solution:** The software can be changed to pre-compute known coefficient sets.

## Limited Maximum Resolution of video Stream 2 When Video Stream 1 is 3G-SDI

There is a limitation that when Video Stream 1 input is 3G-SDI (1080p60), Video Stream 2 input is limited to a maximum resolution of 1080i60.

## Revision History

Table 6 shows the revision history for the *AN-559: High Definition (HD) Video Reference Design V1* application note.

**Table 6.** AN-559 Revision History

| Version | Date          | Errata Summary                          |
|---------|---------------|---|
| 1.0     | December 2008 | First release of this application note. |



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