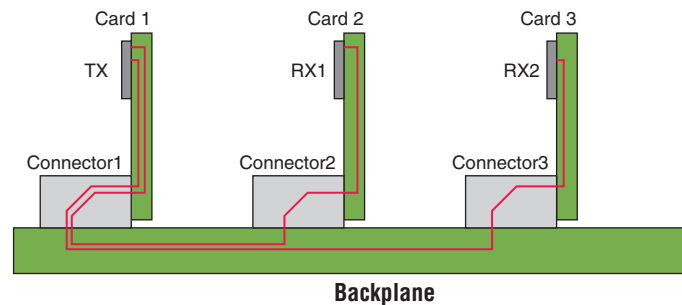


This application note discusses the impact of backplane connectors on a 10 Gbps serial channel performance. It demonstrates how to project the connector's impact at the system level with the help of an industrial simulation software. Design considerations of the backplane connector and pin field are discussed to minimize the connector's impact and to meet the channel's signal integrity requirement. Simulation and measurement results are shown to demonstrate the effectiveness of the design considerations.

## Introduction

A backplane system is widely used in computer and telecommunication systems because of its flexibility and reliability. [Figure 1](#) illustrates a backplane system. The backplane consists of a PCB and several backplane connectors in parallel. It is used as a backbone to connect several plug-in cards together to make up a complete backplane system. Devices in the Altera® Stratix® IV device family are capable of communicating with other devices at data rates of up to 11.3 Gbps. A backplane system design with improved signal integrity (SI) is required to reliably enable devices performing at this speed.

**Figure 1.** Schematic of a Backplane System



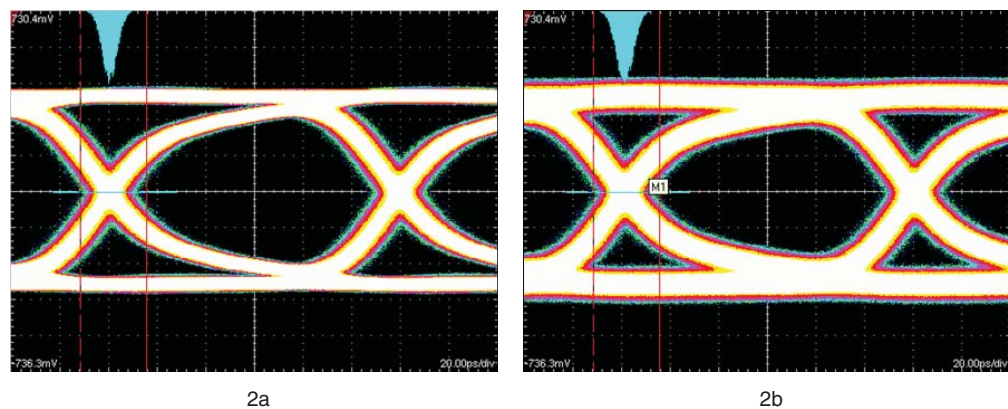
A backplane connector and the associated pin field is one of the most important features in designing a gigabit backplane channel. As shown in [Figure 1](#), the signal generated by a transmitter located on one of the line cards travels through two connectors before it reaches the receiver located at another line card. Signal integrity issues such as reflection, loss, and crosstalk introduced by the connector can significantly degrade system reliability and performance. The ability to simulate and accurately predict the impact of these issues is critical to achieve an operational serial channel design.

## Impact of High-Speed Backplane Connectors

Backplane connectors introduce loss, reflection, and crosstalk to serial channels and degrade the channel's signal integrity. Attenuation reduces the magnitude of the received waveform. The non-uniform loss over frequencies also causes inter-symbol interference (ISI) and adds data-dependent jitter to the channel. Crosstalk and reflection introduce noise and degrade the signal edge rate, which further deteriorates channel jitter performance.

Figure 2 compares the eye diagrams at the receiver side of two HSSI channels. The channels have identical layouts except that one channel has higher crosstalk due to smaller separation of the channels on the next layer. The channel with higher crosstalk has smaller eye height and eye width (Figure 2b), indicating that the received data has higher signal distortion and jitter.

**Figure 2.** Crosstalk Impact on the Eye at 8.5 Gbps



A connector's impact on channel signal integrity becomes increasingly significant as signal margins are reduced at higher data rates. The voltage swing of high-speed signaling tends to decrease to reduce the power consumption and ensure a fast transition, which reduces eye height. The signal unit interval (UI) is also reduced at a higher data rate. For example, a UI is 200 ps at a 5 Gbps data rate, but is reduced to 100 ps at a 10 Gbps data rate. A smaller UI is translated into more stringent timing requirements. The backplane connector's impact is also amplified by the use of pre-emphasis. Pre-emphasis is a commonly used signal processing technique for high-speed data communication. However, it results in higher crosstalk because more high-frequency noise is coupled to victim traces. To minimize the impact, pay attention to every detail of the high-speed backplane connector design.

## Projecting the Connector's Impact on Channel Performance

The goal of backplane connector design is to ensure that the channel with the selected backplane connector design meets the performance requirement defined in the specification. You must explore the connector design space to optimize the design and improve channel performance if there is a violation.

## Challenges in Projecting Channel Performance

The impact of backplane connector design on a serial channel is evaluated with the channel performance change. The channel performance is measured with eye opening and bit error rate (BER), which can only be derived by simulating the transient response of the entire channel at the design stage. Simulation uses limited length pseudo-random binary sequence (PRBS) patterns, which only cover limited data patterns transmitted through the channel. This reduces confidence in the results, especially when the BER is low, because the eye diagram derived from a limited sample does not guarantee that the system BER requirement will be met. The alternative is to use the worst-case data pattern for transient simulation. The challenge for this approach is to define the worst-case pattern. The pattern could be different for two channels with different frequency responses because the pattern is related to the channel frequency response. Using the worst-case patterns also results in an overly pessimistic conclusion. A system could meet the required BER specification even though simulation results using the worst-case pattern fail to meet the eye-mask requirement.

The statistical signal analysis (SSA) methodology expedites the process of projecting channel timing performance and reduces dependency on the data pattern. Instead of simulating lengthy data patterns, the method calculates the receiver probability density function (PDF) from the channel impulse response. The channel BER is derived from the calculated PDF, because the BER requirement can be directly related to a certain PDF. This method takes much less time compared to the traditional transient simulation approach.



For a detailed introduction to the SSA methodology, refer to Anthony Sanders, "Statistical Signal Analysis (SSA) Demystified", *EE Times-India*, August 2007.

## Modeling Channel Performance Using Stateye and MATLAB

Stateye is an open source tool originally developed by members of the Optical Internetworking Forum (OIF). The tool determines the compliance of a channel based on the common electrical interface (CEI) standard. It provides a GUI for entering information related to the serial channel to be studied, such as transceiver profile and channel behavior, and generates code for performing SSA on serial channel performance. Running the code in MATLAB produces results such as statistical eye plots.

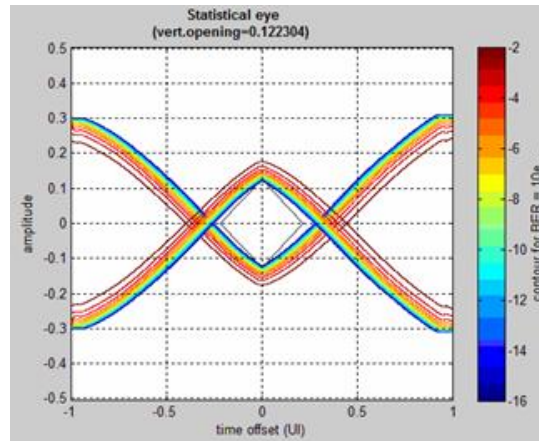


This application note uses the Stateye software version 4.2. The software and user manual can be downloaded from the Stateye website ([www.stateye.org](http://www.stateye.org)). A tutorial on how to configure the model settings in the software can also be downloaded from the website.

The first step of the modeling procedure is to use simulation or measurement to generate S-parameters that capture insertion loss, reflection loss, and crosstalk for aggressor and victim channels. The next step is to configure the channel model to be simulated in the Stateye software. The required inputs include pre-emphasis and equalization settings for driver and receiver, jitter model, a port map that links ports in the S-parameter files to the S-matrix used in the tool, and other related items. Simulation results are derived by running the generated MATLAB code.

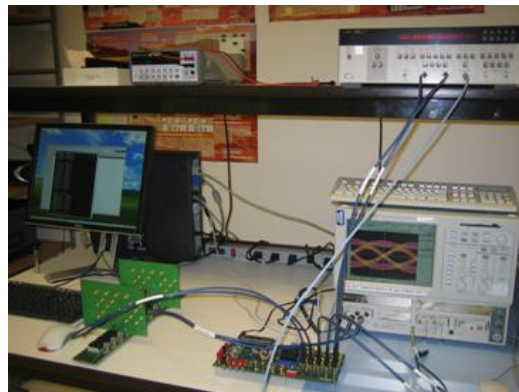
One of the MATLAB outputs is the statistical eye plot of the channel (Figure 3). The plot looks similar to the eye diagram and is composed of colored BER contours instead of time domain waveforms. The BER requirement can be met by the channel if the required eye mask is within the required contour.

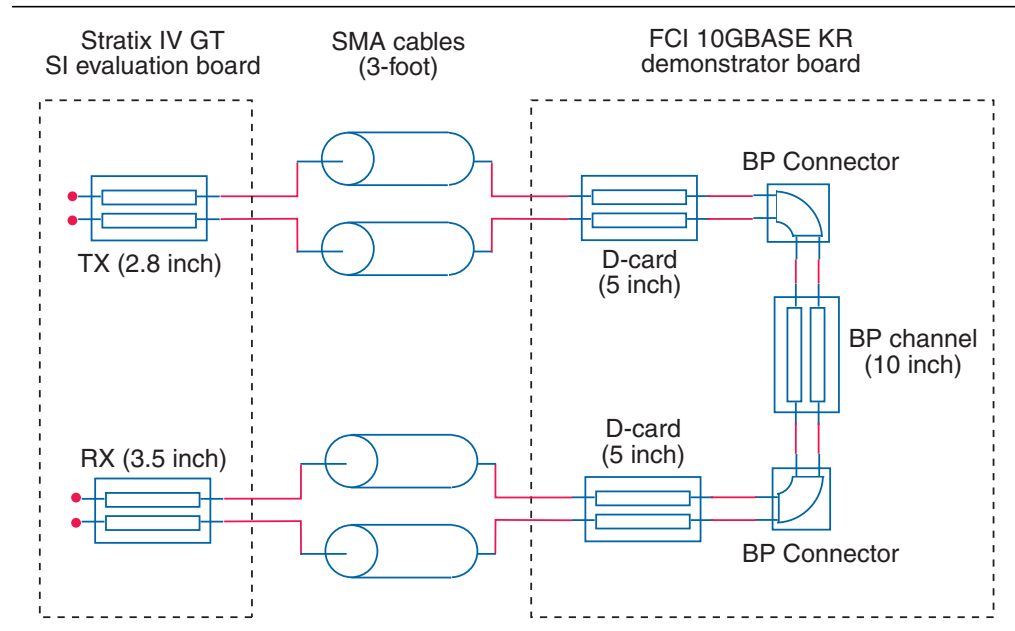
**Figure 3.** Example of a Statistical Eye



The backplane system to be modeled, as shown in Figure 4, consists of an Altera Stratix IV GT signal integrity evaluation board and the FCI 10GBASE KR backplane demonstrator board, which consists of a backplane and two daughter cards. Two sections are connected via 3-foot low-loss SMA cables. Figure 5 shows the configuration and the serial channel to be modeled and the dimension of each section.

**Figure 4.** Setup of the Modeled Backplane System



**Figure 5.** Schematic of the Complete Serial Channel

The complete serial channel is too complicated to be modeled with a single modeling tool. A common practice is to model the serial channel with a hybrid modeling approach. In this approach, a channel is divided into sections and each section is modeled with an appropriate modeling tool for better accuracy and modeling efficiency. The overall channel performance is then derived by cascading the modeling results of all the modules.

The serial channel shown in [Figure 5](#) is divided into an SI evaluation board section, a backplane demonstrator board section, and an SMA cable section. Each section is modeled separately:

- The SI evaluation board design file is imported into the Sigroty PowerSI software and the behavior of the TX and RX channels are simulated. This ensures that the impacts of discontinuities in the physical channel layout are captured.
- The performance of the FCI backplane demonstrator board is characterized up to 20 GHz with measured S-parameter data provided by the connector manufacturer. Measurement data is preferred because some effects, such as connector contact resistance, frequency dependent dielectric loss, fiber wave effect, and manufacture variation, can only be accurately captured by measurement.
- The SMA cables are modeled with a simple transmission line model provided by the Agilent ADS software because the cable loss is small in the applicable frequency range.

A model representing the entire channel is constructed in the Agilent ADS software by cascading the S-parameters of all the sections, as shown in [Figure 6](#). The simulated insertion loss and return loss of the serial channel are shown in [Figure 7](#).

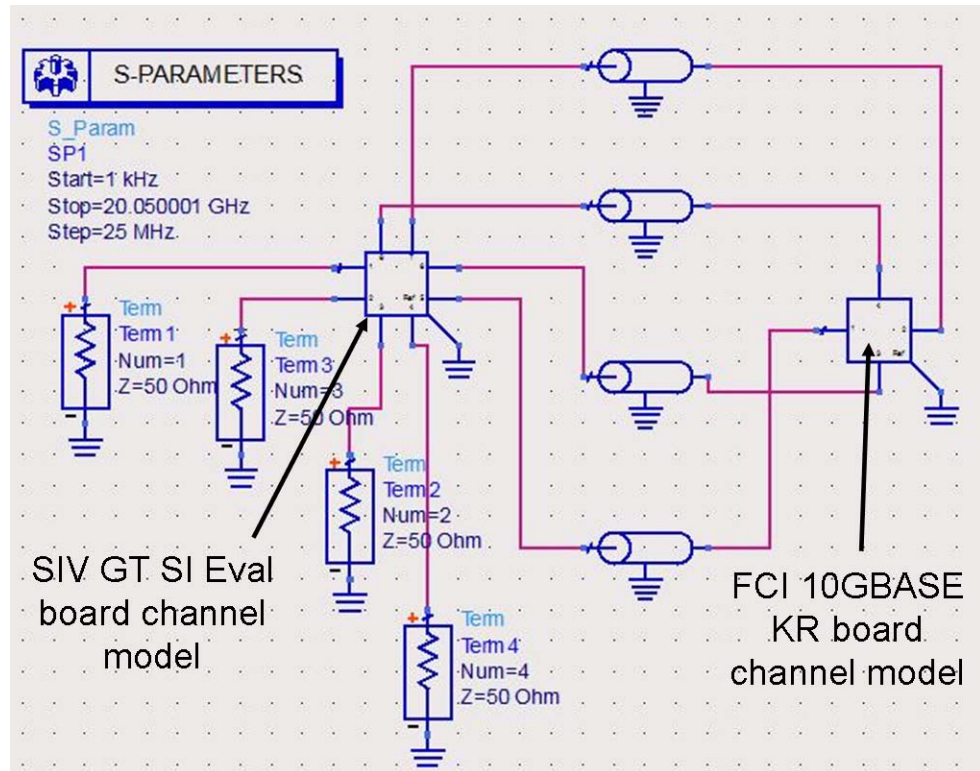
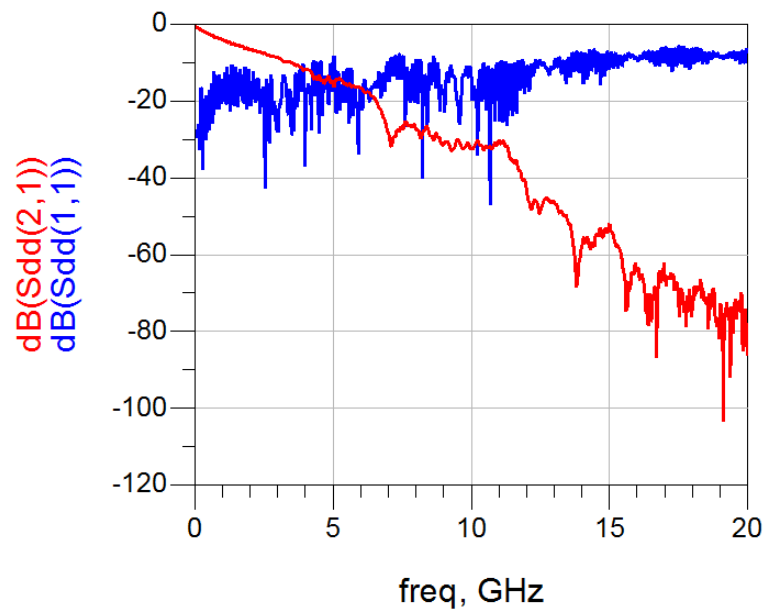
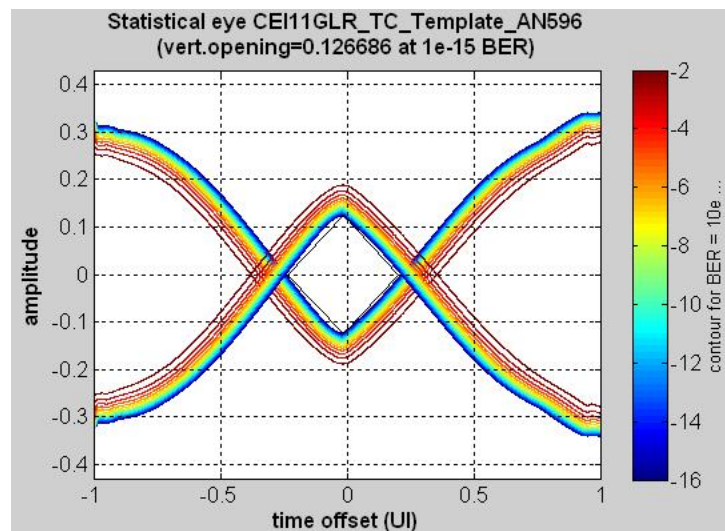
**Figure 6.** ADS Simulation Deck of the Serial Channel**Figure 7.** Simulated S-Parameters of Benchmark Serial Channel



Figure 8 shows a generated statistical eye plot, where the eye mask, as defined in the CEI-11G-LR long reach interface specification, is within the  $1\text{e-}16$  BER, indicating that this particular channel meets the  $1\text{e-}16$  BER requirement when used with CEI-11G-LR compliant transceivers. It only takes about 20 minutes for the MATLAB program to generate results.

The Stateye simulation deck, S-parameter files, and the generated MATLAB code are contained in the associated zip file `an596_stateye_examples.zip`.

**Figure 8.** Generated Statistical Eye of the Studied Serial Channel



A time domain measurement is conducted to check the performance of the channel modeled. The channel is driven by a Stratix GT device. The data rate is 10.3125 Gbps. The magnitude of the output differential signal is 0.8 V with optimized pre-emphasis settings. The data pattern is PRBS-31. The receiver detected three errors after the system ran for 26 hours. The result indicates that the serial channel is capable of transmitting data at 10.3125 Gbps with a low BER.

The BER can be simply calculated by dividing the number of errors detected by the number of total bits going through the channel. Based on the measurement data, the BER is  $3.078\text{e-}15$ . The computation process becomes more complicated when the confidence level (CL) is required for the measured results and the calculated BER becomes higher. For example, the BER of this channel is  $8\text{e-}15$  with a CL of 0.95.



Refer to MAXIM application note 1095, *HFTA-05.0: Statistical Confidence Levels for Estimating Error Probability* for details on how to calculate the BER with the CL requirement taken into consideration. ([www.maxim-ic.com](http://www.maxim-ic.com))



The Stateye software assumes the channel is driven by CEI compliant transceivers and the signaling meets CEI specifications. However, the behavior of the transceivers and signaling used in the application may not be fully CEI-compliant at the studied frequency range. The projected optimized pre-emphasis setting may not be available in the transceivers. The measured channel performance might be different from that predicted by the Stateye software as a result.



Backplane applications at 10 Gbps are dependent on both transceiver characteristics and customer channel designs. Though testing has indicated interoperability across serial channels up to 20 inches at 10.3125 Gbps using Altera Stratix IV GT devices, it is up to you to determine the link reliability across the channel in your design.

Stateye provides the means for quickly projecting channel BER performance. The actual channel performance may vary from the projected one due to the difference between simulated channel behavior and actual channel behavior. However, the tool is helpful for “what if” design space exploration. Stateye simulation results, along with the data from simulation and measurement, are used in the discussion in the next section.

## Transparent Backplane Connector Structure Design

An ideal connector is transparent to the propagating signal when the discontinuities introduced by the connector are small enough that their effect on the signal is negligible. This section describes the features and design considerations of the connector and pin fields that help reduce the loss, reflection, and crosstalk introduced by backplane connectors and improve the channel signal integrity.

### Backplane Connector Features that Improve Signal Integrity at 10 Gbps

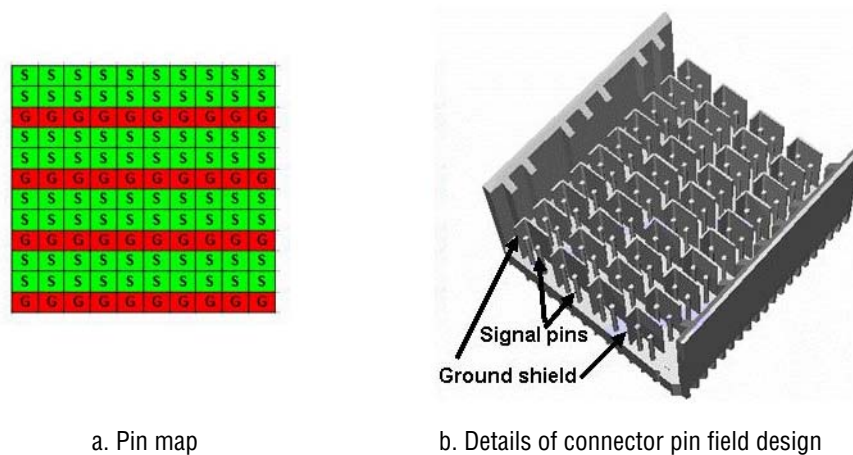
Backplane connectors designed for 10 Gbps and higher data rates are required for a 10 Gbps backplane design. There are several 10 Gbps backplane connectors available in the market, such as the Airmax VS connector from FCI, the Z-pack connector from Tyco electronics, and the Gbx connector from Molex. Compared to the connectors designed for low-speed applications, these 10 Gbps connectors have some common features that help reduce the effects of discontinuities and improve the connectors performance for 10 Gbps or higher data rate applications:

- 10 Gbps connectors are optimized to handle differential signals. All high-speed standards adopt differential signaling for 10 Gbps and higher data rate communication. Compared to single-ended signaling, differential signaling is less affected by noise. It also uses a lower voltage swing, which allows higher data rates. Differential signaling offers better electromagnetic interference performance as well.
- Pin function is pre-defined in 10 Gbps connectors for optimized ground distribution. Ground pins provide a return path for the signal current and affect the transmission line's impedance. Good ground pin distribution reduces impedance discontinuity and minimizes reflection. A ground pin between two signal pins also improves isolation between the two signal pins and reduces crosstalk. [Figure 9a](#) and [Figure 10a](#) show pin maps of two 10 Gbps backplane connectors. Ground pins are marked with the letter “G” and signal pins are marked with the letter “S”. As shown in the figures, there is an evenly distributed ground via pattern in both pin maps.
- 10 Gbps connectors have design features that limit electromagnetic (EM) field distribution within the pin field inside the connector. The connector design illustrated in [Figure 9b](#) has an extended “L” shaped ground shield around each pair of signal pins, which helps confine the EM field of the signal pins. The connector design illustrated in [Figure 10b](#) uses an edge-coupled signal-ground

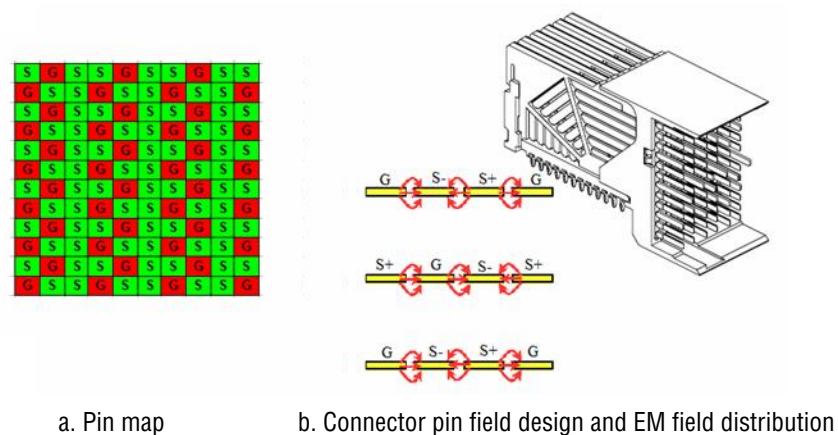


pin design, where the EM field distribution is concentrated on the edge of two coupled traces. Coupling to signal traces located in the next row is greatly reduced. Noise is coupled to the victim trace when the trace is within the EM field of the aggressor trace. Confining the EM field distribution of the signal trace limits the coupled noise and reduces the impact of crosstalk.

**Figure 9.** 10 Gbps Backplane Connector Design 1



**Figure 10.** 10 Gbps Backplane Connector Design 2



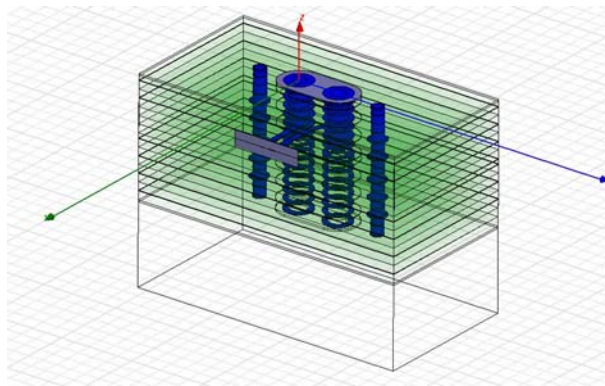
## Optimize Via Pin Field Design

There is a via pin field underneath the backplane connector. The pin field holds the backplane connector to its position on the PCB. It also serves as a transition between the PCB traces and the connector. A via pin field can cause more degradation to the signal quality than the connector. Design optimization of the via pin field is required for 10 Gbps or higher applications.

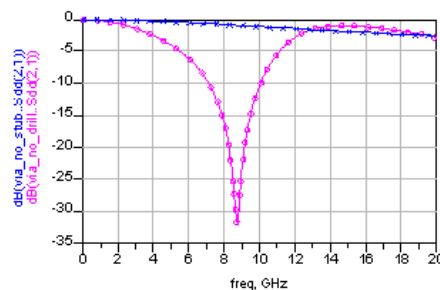
## Via Optimization

A significant contributor to signal integrity issues comes from the reflections caused by via stubs. A via stub in a transmission line can be modeled as an open-ended stub connected to the transmission line. The frequency response of the transmission line with a stub is similar to a band block filter, which blocks signal propagation along the transmission line at certain frequencies. The location of the dip is related to the length of the open stub and the dielectric constant of the material used. A via transition with a 106-mil stub is simulated in HFSS (Figure 11). The dielectric material used is Nelco4000-13 with a dielectric constant of 3.4. The simulated S21 parameter shows that the stub causes a resonance with the center located around 8.7 GHz (Figure 12). For comparison, the via transition with no stub shows much less loss in the affected region.

**Figure 11.** HFSS Simulation Deck of Back Drill Via



**Figure 12.** Comparison of Differential Insertion Loss of Via Transitions with and without Stub



A simple serial channel is simulated to demonstrate the via stub's impact on channel insertion loss and the eye opening of 10 Gbps data. The simulated channel consists of a 20-inch PCB trace, two backplane connectors, and six vias (Figure 13). The simulation assumes that the two affected vias are those connecting the backplane connector and backplane trace.

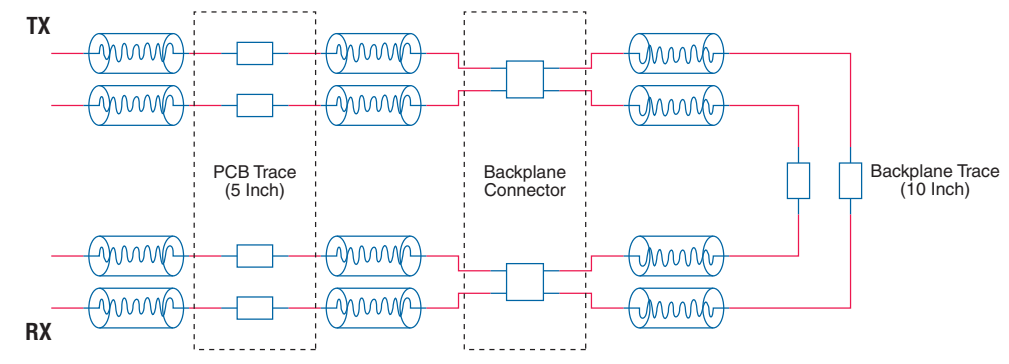
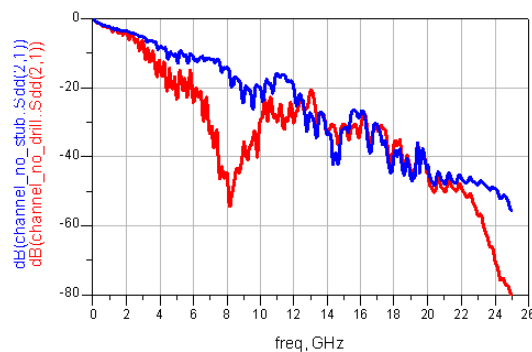
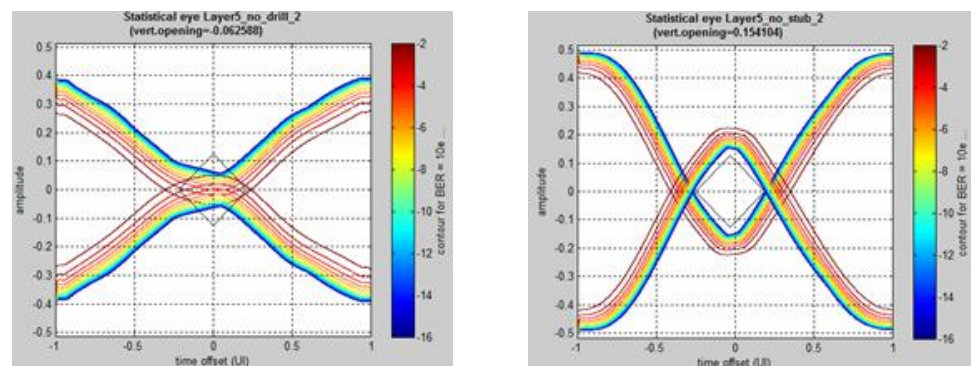
**Figure 13.** Simulated Serial Channel

Figure 14 compares the simulated differential channel insertion loss with and without the stub. As shown in the plot, two long stubs cause significant loss to the signal going through the channel near 8 GHz. Figure 15 compares the calculated statistical eye based on the simulated frequency domain response. The eye is closed for 10 Gbps data when the channel has two 106-mil stubs. The eye opening is 0.308 V if the two stubs are eliminated.

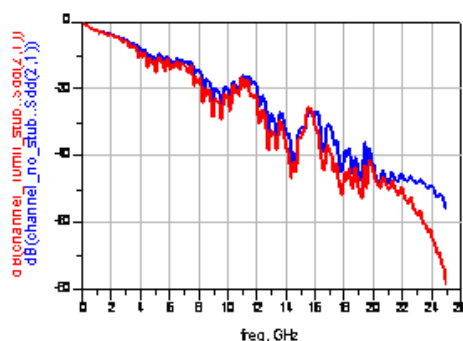
**Figure 14.** Simulated Differential Channel Insertion Loss with and without Stub**Figure 15.** Statistical Eye for Channel with and without Stub

You can reduce the stub by routing high-speed serial channels on PCB layers that are close to the bottom of the PCB stack-up. However, this limits the available layers for serial channel routing. Back drill is another commonly used method for reducing via stub length in high-speed board designs. The unwanted via stub is removed by drilling the backside of the PCB with a slightly oversized drill bit. Back drilling requires an additional step in the PCB fabrication process and increases the cost of the PCB. A via stub cannot be removed completely by back drilling. There is a limitation on the accuracy of back drilling depth control. A 5- to 10-mil buffer zone is necessary to avoid destroying the via connection during the drilling process.

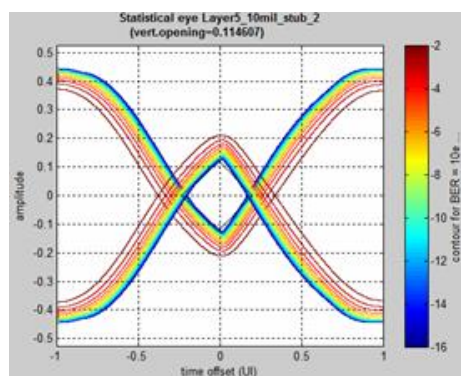
Figure 16 shows similar differential insertion loss for a channel with ideal via (no stub) and a channel with a 10-mil via. The calculated statistical eye, however, indicates that the eye opening is reduced to 0.23 V due to the 10-mil via stub (Figure 17).

The maximum depth of back drilling is determined by the connector pin length because these pins cannot be back drilled. A via stub cannot be completely removed by back drilling if a trace is located at a PCB layer in which the via stub length is longer than the maximum drilling depth. The trace performance will be affected by the stub. The effect can be reduced by optimizing the PCB stack-up and moving those traces to the lower layers of the PCB stack-up.

**Figure 16.** Simulated Differential Channel Insertion Loss with No Stub and 10-Mil Stub



**Figure 17.** Statistical Eye for Channel with 10-Mil Stub



Other via features, such as the non-functional pad (NFP) and the anti-pad, can cause an increase in both channel insertion loss and return loss. The discontinuities introduced by these features can be reduced with techniques such as reducing the capture pads dimension, eliminating the NFP, and increasing the anti-pad dimension.



For more information about the effects of via discontinuities and techniques to mitigate their effects, refer to *AN 529: Via Optimization Techniques for High-Speed Channel Designs*. Additionally, this application note offers guidelines, recommendations, and other considerations for signal via design.

Most backplane connectors are press-fitted to the PCB because press-fitting allows back drilling within the connector via pin field. You must specify the finished PCB via hole size for the via pin field according to the manufacturer's recommendation. An incorrect via hole size will cause assembly difficulty or degrade signal quality.

### Trace Routing Optimization

From a transmission line perspective, the characteristic impedance,  $Z_0$ , of a transmission line is defined in [Equation 1](#).

**Equation 1.**

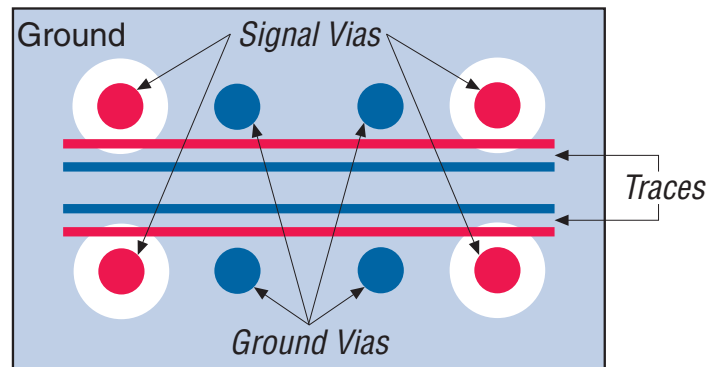
$$Z_0 = \sqrt{\frac{L}{C}}$$

$L$  and  $C$  are equivalent inductance and capacitance between a transmission line and its reference plane. Changes in the transmission line, such as width and shape, and the reference plane affect equivalent  $L$  and  $C$ . This may cause a change in the characteristic impedance and may increase signal loss due to higher reflection.

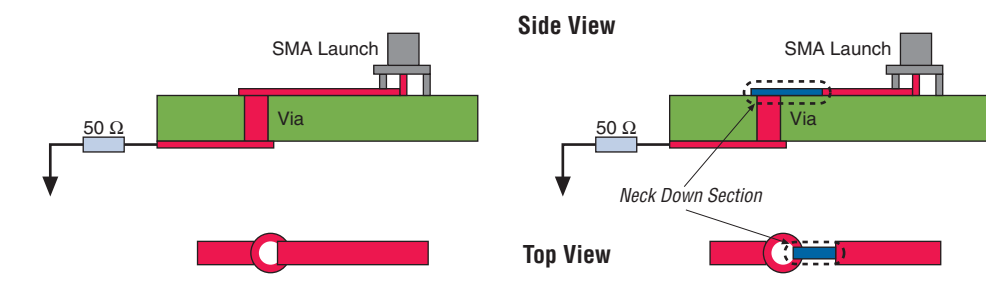
Space is limited within the pin field in some cases and traces have to fan out through narrow routing channels. It can be difficult to follow the layout guide line and keep the trace referenced within this region. This affects the equivalent  $L$  and  $C$  of the trace. Typical discontinuities within the pin field include the following:

- **Anti-pad**—Anti-pad is the void region surrounding a via pad. [Figure 18](#) shows two differential pairs that are routed between two rows of vias. Two green traces have a solid reference plane. However, the two red traces have sections above the anti-pad region of signal vias due to the limitation of routing space. The trace does not have a good reference in the void region. This causes increased trace inductance and decreased capacitance. Trace characteristic impedance increases as a result.

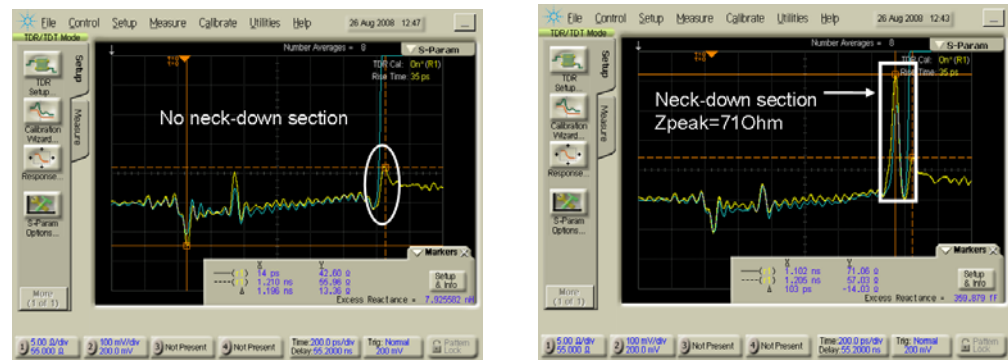
In addition to impedance change, the signal propagation speed is reduced in the void region. This also has an impact on the length matching for differential signal traces because the difference in signal propagation time is not proportional only to the trace length difference. Asymmetry in reference ground also causes mode conversion and induces higher common mode noise for the differential signal. Reducing trace routing density and anti-pad dimension increases routing space and reduces the impact of anti-pad.

**Figure 18.** Discontinuities in the Via Pin Field

- **Power/ground vias**—The impact of power/ground vias on signal integrity is from coupling between trace and power/ground vias. Inductance of a trace is not affected because the trace is perpendicular to the power/ground vias. Capacitance increases because of the additional coupling between the trace and vias. The characteristic impedance  $Z_0$  of the trace is consequently reduced. Increasing the separation between trace and power/ground vias reduces the impedance variation due to capacitive coupling.
- **Narrow trace break-out**—The routing channel is limited for some designs. Reducing the trace width (neck down) and moving the trace closer allows more traces to fan out. These changes increase the trace characteristic impedance and the insertion/reflection loss. The trace receives more crosstalk from nearby traces as well. Figure 19 illustrates the configuration of two similar trace designs being measured. The TDR measurement results are shown in Figure 20. The neck-down section causes a spike with a peak value of  $71\ \Omega$  in the impedance plot on the right. The trace width of a tightly coupled differential pair is narrower than that of a loosely coupled differential pair for the same differential impedance. Therefore, increasing coupling between two traces in a differential pair helps reduce the impedance change due to reduced trace width.

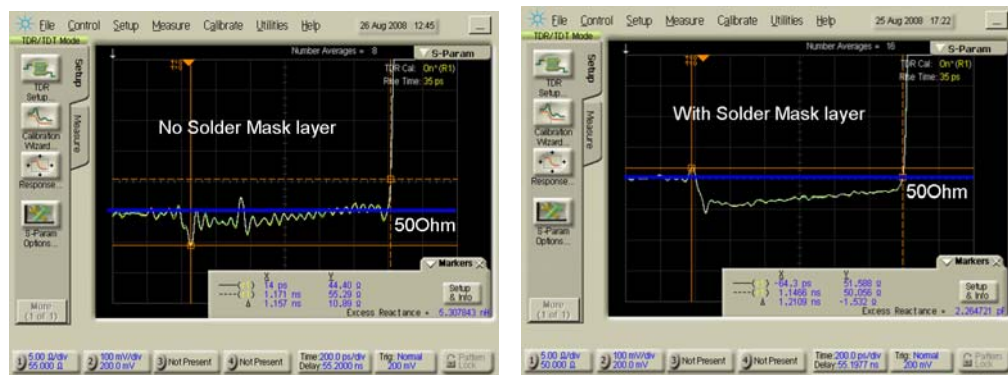
**Figure 19.** Schematic of Two Trace Benchmark Structures



**Figure 20.** TDR Measurement Results of Benchmark Structures Shown in Figure 19

- **Solder mask**—A solder mask is a layer of polymer material applied to the surface of PCBs to protect the surface copper trace. The dielectric constant of the solder mask is higher than that of air. The surface trace dimension is usually calculated with the assumption that traces are exposed to air. A PCB trace has a lower characteristic impedance after being coated with a solder mask (refer to Figure 21).

The measured impedance of a 50-Ω surface PCB trace without a solder mask is about 50 Ω. The measured impedance of an identical PCB trace with a solder mask layer is about 47 Ω. The effect of solder mask on trace impedance must be taken into consideration when deriving the dimension for surface high speed serial channel design.

**Figure 21.** Comparison of TDR Results on Traces with and without Solder Mask Layer

Some discontinuities have the opposite effect on trace impedance. Also, there are other restrictions that limit the available design optimization options. Simulation and measurement are required to finalize the optimum parameters for a pin field design. The following general guidelines are helpful in the design process:

- Maintain a uniform trace width and trace spacing (for differential traces). Keep the neck-down section short and the trace width reduction as small as possible if it must be used.
- Maintain a solid reference plane. Avoid routing trace across the void in the reference plane, such as anti-pad and moat.

- Keep the routing of two traces in a differential pair identical because this helps reduce trace skew and mode conversion due to asymmetry of the traces.
- Keep a good separation between different differential trace pairs. The recommended separation between nearby differential trace pairs is five times the distance between the trace and the nearest reference plane.
- Take the effect of the solder mask layer into consideration when designing the surface layer PCB trace.

## Pin Assignment Optimization

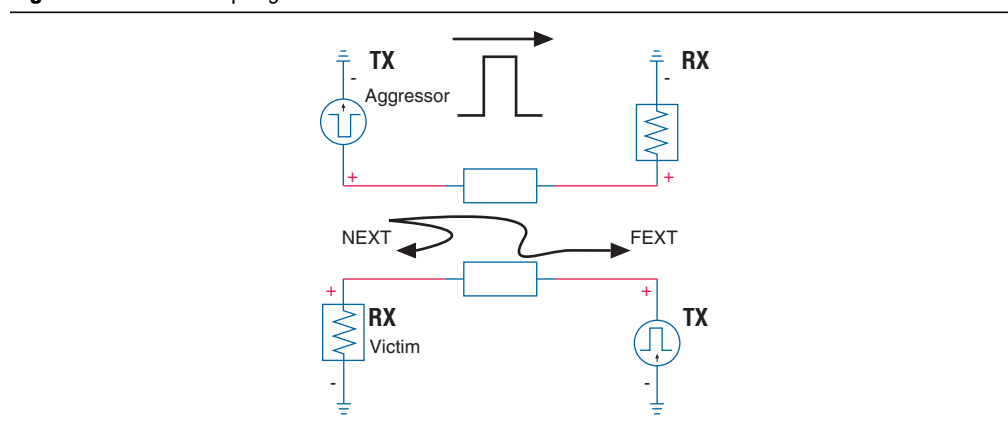
Noise coupled from nearby channels affects the signal integrity of the channel. There are two types of crosstalk: near-end crosstalk (NEXT) and far-end crosstalk (FEXT). The two types behave differently. The duration of FEXT noise created by a switching bit is equal to the rising/falling edge of the bit. NEXT noise lasts much longer. Its duration is twice the time required for the bit edge to travel through the coupled section on the aggressor trace. FEXT is greatly reduced by using stripline instead of microstrip. The improvement is much less for NEXT. NEXT, therefore, has more impact on signal integrity and is the major concern of crosstalk.

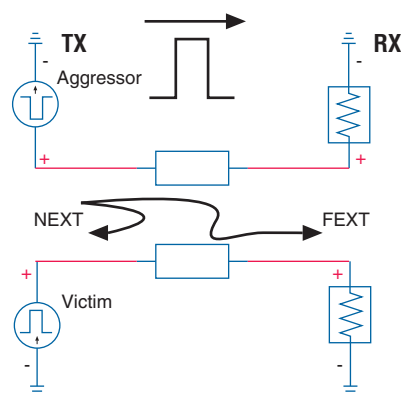
Figure 22 illustrates the noise coupling route when a TX channel is placed next to an RX channel. As shown in Figure 22, the NEXT generated on the victim flows directly into the receiver of the victim channel. This increases the noise floor of the victim receiver and degrades the victim channel performance. The noise coupling route between two TX channels is illustrated in Figure 23. FEXT is coupled to the receiver of the victim channel. The impact on the victim channel is smaller, because the FEXT duration is shorter and the magnitude is smaller.



You can help reduce the impact of crosstalk by optimizing the location of the TX and RX pins on the connector and by increasing the separation between the RX and TX channels.

**Figure 22.** Noise Coupling Route in the Case of RX and TX Channel in Parallel



**Figure 23.** Noise Coupling Route in the Case of Two TX Channels in Parallel

## Conclusion

Loss, reflection, and crosstalk introduced by a backplane connector have significant impact on serial channel signal integrity for 10 Gbps applications. New design guidelines and a simulation methodology are required to ensure the serial channel meets the design specification with a derived connector design. This paper introduces a methodology to help you project a connector's impact on channel BER performance. The design optimization methods discussed in this application note help minimize the backplane connector's impact on signal integrity and improve channel performance.

## Document Revision History

Table 1 shows the revision history for this application note.

**Table 1.** Document Revision History

Date	Version	Changes Made
March 2010	1.0	Initial release.



101 Innovation Drive  
San Jose, CA 95134  
[www.altera.com](http://www.altera.com)  
Technical Support  
[www.altera.com/support](http://www.altera.com/support)

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