Cyclone® II EP2C70 Device Pin-Out
PT-EP2C70-1.7

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Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F672	F896	DQS for x8/x9 in F672	DQS for x16/x18 in F672	DQS for x8/x9 in F896	DQS for x16/x18 in F896
B2	VREFB2N0	GND_PLL3			E4	K10				
B2	VREFB2N0	VCCD_PLL3			H7	J9				
B2	VREFB2N0	GND_PLL3			G7	J8				
B2	VREFB2N0	GND								
B2	VREFB2N0	IO	ASDO	ASDO	E3	G7				
B2	VREFB2N0	IO	nCSO	nCSO	D3	K9				
B2	VREFB2N0	IO	LVDS68p	CRC_ERROR	B2	H7				
B2	VREFB2N0	IO	LVDS68n	CLKUSR	B3	H8				
B2	VREFB2N0	IO	PLL3_OUTp		E5	G5				
B2	VREFB2N0	IO	PLL3_OUTn		F6	G6				
B2	VREFB2N0	VCCIO2								
B2	VREFB2N0	IO	LVDS67p		C2	F3				
B2	VREFB2N0	IO	LVDS67n		C3	F4				
B2	VREFB2N0	IO	VREFB2N0		G5	H5				
B2	VREFB2N0	IO			G6	H6				
B2	VREFB2N0	IO	LVDS66p			G3				
B2	VREFB2N0	IO	LVDS66n			G4				
B2	VREFB2N0	GND								
B2	VREFB2N0	IO	LVDS65p			E3				
B2	VREFB2N0	IO	LVDS65n			E4				
B2	VREFB2N0	IO	LVDS64p		F3	B2				
B2	VREFB2N0	IO	LVDS64n		F4	C3				
B2	VREFB2N0	IO	LVDS63p		D2	C1				
B2	VREFB2N0	VCCIO2								
B2	VREFB2N0	IO	LVDS63n		D1	C2				
B2	VREFB2N1	IO	LVDS62p		F7	D2				
B2	VREFB2N1	IO	LVDS62n			D3				
B2	VREFB2N1	IO	LVDS61p		J8	H3				
B2	VREFB2N1	IO	LVDS61n		J7	H4				
B2	VREFB2N1	IO	LVDS60p			J7				
B2	VREFB2N1	IO	LVDS60n		H6	J6				
B2	VREFB2N1	GND								
B2	VREFB2N1	IO	VREFB2N1		J5	J5				
B2	VREFB2N1	IO	LVDS59p		E2	K8				
B2	VREFB2N1	IO	LVDS59n		E1	K7				
B2	VREFB2N1	IO	LVDS58p		K6	L8				
B2	VREFB2N1	IO	LVDS58n		K5	L7				
B2	VREFB2N1	VCCIO2								
B2	VREFB2N1	IO	LVDS57p		G4	L10				
B2	VREFB2N1	IO	LVDS57n		G3	L9				

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F672	F896	DQS for x8/x9 in F672	DQS for x16/x18 in F672	DQS for x8/x9 in F896	DQS for x16/x18 in F896
B2	VREFB2N1	IO	LVDS56p			K6				
B2	VREFB2N1	IO	LVDS56n		J6	K5	DQ2L0	DQ1L0		
B2	VREFB2N1	IO	LVDS55p		K8	L6	DQ2L1	DQ1L1		
B2	VREFB2N1	IO	LVDS55n		K7	L5	DQ2L2	DQ1L2		
B2	VREFB2N1	IO	LVDS54p		F2	M9	DQ2L3	DQ1L3		
B2	VREFB2N1	IO	LVDS54n		F1	M8	DQ2L4	DQ1L4		
B2	VREFB2N1	GND								
B2	VREFB2N1	IO	LVDS53p		G1	E1	CDPCLK0/DQS2L	CDPCLK0/DQS2L	CDPCLK0/DQS2L	CDPCLK0/DQS2L
B2	VREFB2N1	IO	LVDS53n		G2	E2				
B2	VREFB2N2	VCCIO2								
B2	VREFB2N2	IO	LVDS52p		H3	F1	DQ2L5	DQ1L5	DQ2L0	
B2	VREFB2N2	IO	LVDS52n		H4	F2	DQ2L6	DQ1L6	DQ2L1	
B2	VREFB2N2	IO	LVDS51p		J3	G1	DQ2L7	DQ1L7	DQ2L2	
B2	VREFB2N2	IO	LVDS51n		J4	G2		DQ1L8	DQ2L3	
B2	VREFB2N2	IO	LVDS50p		H2	H1	DM2L	DM1L0/BWS#1L0	DQ2L4	
B2	VREFB2N2	IO	LVDS50n		H1	H2			DQ2L5	
B2	VREFB2N2	GND								
B2	VREFB2N2	IO	LVDS49p		J2	K3			DQ2L6	
B2	VREFB2N2	GND								
B2	VREFB2N2	IO	LVDS49n		J1	K4	DQ0L0	DQ1L9	DQ2L7	
B2	VREFB2N2	IO	LVDS48p		K4	N10	DQ0L1	DQ1L10		
B2	VREFB2N2	IO	LVDS48n		K3	M10	DQ0L2	DQ1L11	DM2L	DQ1L0
B2	VREFB2N2	VCCIO2								
B2	VREFB2N2	IO	LVDS47p			M6				DQ1L1
B2	VREFB2N2	IO	LVDS47n			M7				DQ1L2
B2	VREFB2N2	IO	LVDS46p		K1	J1	DQ0L3	DQ1L12		DQ1L3
B2	VREFB2N2	IO	LVDS46n		K2	J2	DQ0L4	DQ1L13		
B2	VREFB2N2	IO	VREFB2N2		L4	M5				
B2	VREFB2N2	IO	LVDS45p			L3				
B2	VREFB2N2	IO	LVDS45n			L4				DQ1L4
B2	VREFB2N2	GND								
B2	VREFB2N2	IO	LVDS44p			K1				
B2	VREFB2N2	GND								
B2	VREFB2N2	IO	LVDS44n			K2				
B2	VREFB2N2	IO	LVDS43p			N8				DQ1L5
B2	VREFB2N2	IO	LVDS43n			N7				DQ1L6
B2	VREFB2N3	IO	LVDS42p			L1				DQ1L7
B2	VREFB2N3	VCCIO2								
B2	VREFB2N3	IO	LVDS42n			L2				DQ1L8
B2	VREFB2N3	IO	LVDS41p		L7	P9	DQ0L5	DQ1L14		DM1L0/BWS#1L0

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B2	VREFB2N3	IO	LVDS41n		L6	N9	DQ0L6	DQ1L15		
B2	VREFB2N3	IO	LVDS40p			M1				
B2	VREFB2N3	IO	LVDS40n			M2			DQ0L0	DQ1L9
B2	VREFB2N3	IO	LVDS39p		L2	M3	DQ0L7	DQ1L16	DQ0L1	DQ1L10
B2	VREFB2N3	GND								
B2	VREFB2N3	IO	LVDS39n		L3	M4		DQ1L17	DQ0L2	DQ1L11
B2	VREFB2N3	IO	LVDS38p			N2			DQ0L3	DQ1L12
B2	VREFB2N3	IO	LVDS38n			N3			DQ0L4	DQ1L13
B2	VREFB2N3	IO				P7				
B2	VREFB2N3	VCCIO2								
B2	VREFB2N3	IO	VREFB2N3		M4	N4				
B2	VREFB2N3	GND								
B2	VREFB2N3	IO			M5	P6	DM0L	DM1L1/BWS#1L1	DQ0L5	DQ1L14
B2	VREFB2N3	GND								
B2	VREFB2N3	IO	LVDS37p			P3			DQ0L6	DQ1L15
B2	VREFB2N3	VCCIO2								
B2	VREFB2N3	IO	LVDS37n			P4			DQ0L7	DQ1L16
B2	VREFB2N3	IO	LVDS36p		M3	P1	DPCLK0/DQS0L	DPCLK0/DQS0L	DPCLK0/DQS0L	DPCLK0/DQS0L
B2	VREFB2N3	IO	LVDS36n		M2	P2				
B2	VREFB2N3	TDI		TDI	M8	P8				
B2	VREFB2N3	TCK		TCK	M6	P5				
B2	VREFB2N3	TMS		TMS	L8	R7				
B2	VREFB2N3	TDO		TDO	M7	R4				
B2	VREFB2N3	DCLK	DCLK	DCLK	N6	R9				
B2	VREFB2N3	DATA0	DATA0	DATA0	N3	R8				
B2	VREFB2N3	nCE		nCE	N4	R6				
B2	VREFB2N3	CLK0	LVDSCLK0p/input*(3)*		N2	R2				
B2	VREFB2N3	CLK1	LVDSCLK0n/input*(3)*		N1	R3				
B2	VREFB2N3	GND								
B2	VREFB2N3	nCONFIG		nCONFIG	N7	R5				
B1	VREFB1N0	CLK2	LVDSCLK1p/input*(3)*		P2	T2				
B1	VREFB1N0	CLK3	LVDSCLK1n/input*(3)*		P1	T3				
B1	VREFB1N0	VCCIO1								
B1	VREFB1N0	IO	LVDS35p		P3	T6	DPCLK1/DQS1L	DPCLK1/DQS1L	DPCLK1/DQS1L	DPCLK1/DQS1L
B1	VREFB1N0	IO	LVDS35n		P4	T7				
B1	VREFB1N0	IO	LVDS34p		R2	T4	DQ1L0	DQ3L0		DQ1L17
B1	VREFB1N0	IO	LVDS34n		R3	T5	DQ1L1	DQ3L1	DM0L	DM1L1/BWS#1L1
B1	VREFB1N0	GND								
B1	VREFB1N0	IO	LVDS33p		R4	U1	DQ1L2	DQ3L2		
B1	VREFB1N0	GND								

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F672	F896	DQS for x8/x9 in F672	DQS for x16/x18 in F672	DQS for x8/x9 in F896	DQS for x16/x18 in F896
B1	VREFB1N0	IO	LVDS33n			U2				
B1	VREFB1N0	GND								
B1	VREFB1N0	IO	VREFB1N0		R5	U5				
B1	VREFB1N0	IO	LVDS32p			T9				
B1	VREFB1N0	IO	LVDS32n			T8			DQ1L0	DQ3L0
B1	VREFB1N0	IO	LVDS31p		P7	U9	DQ1L3	DQ3L3	DQ1L1	DQ3L1
B1	VREFB1N0	IO	LVDS31n		P6	U8	DQ1L4	DQ3L4	DQ1L2	DQ3L2
B1	VREFB1N0	VCCIO1								
B1	VREFB1N0	IO	LVDS30p		T2	U6	DQ1L5	DQ3L5	DQ1L3	DQ3L3
B1	VREFB1N0	IO	LVDS30n		T3	U7	DQ1L6	DQ3L6	DQ1L4	DQ3L4
B1	VREFB1N1	IO	LVDS29p			U3				
B1	VREFB1N1	GND								
B1	VREFB1N1	IO	LVDS29n			U4			DQ1L5	DQ3L5
B1	VREFB1N1	GND								
B1	VREFB1N1	IO	LVDS28p		R6	V2	DQ1L7	DQ3L7	DQ1L6	DQ3L6
B1	VREFB1N1	IO	LVDS28n		R7	V3	DQ1L8	DQ3L8	DQ1L7	DQ3L7
B1	VREFB1N1	IO	LVDS27p			W1				
B1	VREFB1N1	IO	LVDS27n			W2				
B1	VREFB1N1	VCCIO1								
B1	VREFB1N1	IO	VREFB1N1		T4	V4				
B1	VREFB1N1	IO	LVDS26p		U2	W3	DM1L/BWS#1L	DM3L0/BWS#3L0		
B1	VREFB1N1	IO	LVDS26n		U1	W4			DQ1L8	DQ3L8
B1	VREFB1N1	IO	LVDS25p		U3	Y1			DM1L/BWS#1L	DM3L0/BWS#3L0
B1	VREFB1N1	IO	LVDS25n		U4	Y2				
B1	VREFB1N1	IO	LVDS24p		V1	Y3				
B1	VREFB1N1	GND								
B1	VREFB1N1	IO	LVDS24n		V2	Y4				
B1	VREFB1N1	IO	LVDS23p		T7	V10				
B1	VREFB1N1	IO	LVDS23n		T6	V9				
B1	VREFB1N1	IO	LVDS22p		V4	V8				
B1	VREFB1N1	IO	LVDS22n		V3	V7				
B1	VREFB1N1	VCCIO1								
B1	VREFB1N1	IO				W5				
B1	VREFB1N1	IO	LVDS21p		W2	AA1	DQ3L0	DQ3L9		
B1	VREFB1N1	IO	LVDS21n		W1	AA2	DQ3L1	DQ3L10		
B1	VREFB1N1	IO	LVDS20p			AA3			DQ3L0	DQ3L9
B1	VREFB1N1	IO	LVDS20n			AA4				
B1	VREFB1N1	IO	LVDS19p			AB1			DQ3L1	DQ3L10
B1	VREFB1N1	IO	LVDS19n			AB2				
B1	VREFB1N1	GND								

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F672	F896	DQS for x8/x9 in F672	DQS for x16/x18 in F672	DQS for x8/x9 in F896	DQS for x16/x18 in F896
B1	VREFB1N2	IO	LVDS18p		U6	W9	DQ3L2	DQ3L11	DQ3L2	DQ3L11
B1	VREFB1N2	IO	LVDS18n		U7	W10	DQ3L3	DQ3L12	DQ3L3	DQ3L12
B1	VREFB1N2	IO			U5	W6	DQ3L4	DQ3L13	DQ3L4	DQ3L13
B1	VREFB1N2	IO	LVDS17p		W4	W8	CDPCLK1/DQS3L	CDPCLK1/DQS3L	CDPCLK1/DQS3L	CDPCLK1/DQS3L
B1	VREFB1N2	IO	LVDS17n		W3	W7				
B1	VREFB1N2	VCCIO1								
B1	VREFB1N2	IO				Y5			DQ3L5	DQ3L14
B1	VREFB1N2	IO	LVDS16p		Y2	AC1				
B1	VREFB1N2	IO	LVDS16n		Y1	AC2	DQ3L5	DQ3L14	DQ3L6	DQ3L15
B1	VREFB1N2	IO	LVDS15p		V5	AC3	DQ3L6	DQ3L15	DQ3L7	DQ3L16
B1	VREFB1N2	IO	LVDS15n		V6	AC4	DQ3L7	DQ3L16		
B1	VREFB1N2	IO	LVDS14p		AA2	AD1	DQ3L8	DQ3L17	DQ3L8	DQ3L17
B1	VREFB1N2	GND								
B1	VREFB1N2	IO	LVDS14n		AA1	AD2	DM3L/BWS#3L	DM3L1/BWS#3L1	DM3L/BWS#3L	DM3L1/BWS#3L1
B1	VREFB1N2	GND								
B1	VREFB1N2	IO	LVDS13p			AD3				
B1	VREFB1N2	IO	LVDS13n			AD4				
B1	VREFB1N2	IO	LVDS12p			AA5				
B1	VREFB1N2	IO	LVDS12n			AA6				
B1	VREFB1N2	VCCIO1								
B1	VREFB1N2	IO	LVDS11p		Y3	Y9				
B1	VREFB1N2	IO	LVDS11n		Y4	Y10				
B1	VREFB1N2	IO	VREFB1N2		W6	Y6				
B1	VREFB1N2	IO	LVDS10p		V7	Y7				
B1	VREFB1N2	IO	LVDS10n			Y8				
B1	VREFB1N2	IO	LVDS9p			AE1				
B1	VREFB1N2	GND								
B1	VREFB1N2	IO	LVDS9n			AE2				
B1	VREFB1N2	GND								
B1	VREFB1N2	IO				AA7				
B1	VREFB1N3	IO	LVDS8p		AB2	AB6				
B1	VREFB1N3	IO	LVDS8n		AB1	AB5				
B1	VREFB1N3	IO	LVDS7p		AA4	AC6				
B1	VREFB1N3	IO	LVDS7n		AA3	AC5				
B1	VREFB1N3	VCCIO1								
B1	VREFB1N3	IO	LVDS6p		AC2	AF1				
B1	VREFB1N3	IO	LVDS6n		AC1	AF2				
B1	VREFB1N3	IO	LVDS5p			AG2				
B1	VREFB1N3	IO	LVDS5n			AG3				
B1	VREFB1N3	IO	LVDS4p			AH1				

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F672	F896	DQS for x8/x9 in F672	DQS for x16/x18 in F672	DQS for x8/x9 in F896	DQS for x16/x18 in F896
B1	VREFB1N3	IO	LVDS4n			AH2				
B1	VREFB1N3	GND								
B1	VREFB1N3	IO	VREFB1N3		AA5	AD5				
B1	VREFB1N3	IO			Y5	AA8				
B1	VREFB1N3	IO	LVDS3p		AD2	AE3				
B1	VREFB1N3	IO	LVDS3n		AD3	AE4				
B1	VREFB1N3	IO	LVDS2p		AE2	AF3				
B1	VREFB1N3	VCCIO1								
B1	VREFB1N3	IO	LVDS2n		AE3	AF4				
B1	VREFB1N3	IO	LVDS1p		AB3	AA9				
B1	VREFB1N3	IO	LVDS1n		AB4	AA10				
B1	VREFB1N3	IO	LVDS0p			AB7				
B1	VREFB1N3	IO	LVDS0n		AC3	AC7				
B1	VREFB1N3	IO	PLL1_OUTp		AA7	AD6				
B1	VREFB1N3	IO	PLL1_OUTn		AA6	AD7				
B1	VREFB1N3	GND								
B1	VREFB1N3	GND_PLL1			W7	AB8				
B1	VREFB1N3	VCCD_PLL1			Y7	AB9				
B1	VREFB1N3	GND_PLL1			Y6	AC8				
B8	VREFB8N3	VCCA_PLL1			AA8	AC9				
B8	VREFB8N3	GNDA_PLL1			Y8	AC10				
B8	VREFB8N3	GND								
B8	VREFB8N3	IO	LVDS256n	DEV_OE	AE4	AE8				
B8	VREFB8N3	IO	LVDS256p		AF4	AE7	DM1B			
B8	VREFB8N3	IO	LVDS255p		AC5	AG4	DQ1B7			
B8	VREFB8N3	IO	LVDS255n		AC6	AG5	DQ1B6		DM1B	
B8	VREFB8N3	IO	LVDS254p		AD4	AJ2	DQ1B5		DQ1B7	
B8	VREFB8N3	IO	LVDS254n		AD5	AH3	DQ1B4		DQ1B6	
B8	VREFB8N3	VCCIO8								
B8	VREFB8N3	IO	LVDS253p		AE5	AK3	CDPCLK2/DQS1B	CDPCLK2/DQS1B	CDPCLK2/DQS1B	CDPCLK2/DQS1B
B8	VREFB8N3	GND								
B8	VREFB8N3	IO	LVDS253n		AF5	AJ3				
B8	VREFB8N3	IO			AD6	AD8	DQ1B3			
B8	VREFB8N3	IO	VREFB8N3		AD7	AH5				
B8	VREFB8N3	GND								
B8	VREFB8N3	IO	LVDS252p			AG6			DQ1B5	
B8	VREFB8N3	IO	LVDS252n			AF7			DQ1B4	
B8	VREFB8N3	IO	LVDS251p			AJ4				
B8	VREFB8N3	IO	LVDS251n			AH4			DQ1B3	
B8	VREFB8N3	VCCIO8								

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F672	F896	DQS for x8/x9 in F672	DQS for x16/x18 in F672	DQS for x8/x9 in F896	DQS for x16/x18 in F896
B8	VREFB8N3	IO	LVDS250p			AK5			DQ1B2	
B8	VREFB8N3	GND								
B8	VREFB8N3	IO	LVDS250n			AJ5			DQ1B1	
B8	VREFB8N2	IO	LVDS249p			AG8				
B8	VREFB8N2	IO	LVDS249n			AF8			DQ1B0	
B8	VREFB8N2	GND								
B8	VREFB8N2	IO	LVDS248p			AH7				
B8	VREFB8N2	IO	LVDS248n			AG7				
B8	VREFB8N2	IO	VREFB8N2		AC7	AF9				
B8	VREFB8N2	VCCIO8								
B8	VREFB8N2	IO	LVDS247p			AK6				
B8	VREFB8N2	GND								
B8	VREFB8N2	IO	LVDS247n		Y10	AJ6	DQ1B2			
B8	VREFB8N2	GND								
B8	VREFB8N2	IO			AB8	AD9	DQ1B1			
B8	VREFB8N2	IO	LVDS246p		AC8	AC11	DQ1B0			
B8	VREFB8N2	IO	LVDS246n		AD8	AD10	DM3B/BWS#3B	DM3B1/BWS#3B1		
B8	VREFB8N2	IO	LVDS245p		AE6	AK7	DQ3B8	DQ3B17	DM3B/BWS#3B	DM3B1/BWS#3B1
B8	VREFB8N2	VCCIO8								
B8	VREFB8N2	IO	LVDS245n		AF6	AJ7	DQ3B7	DQ3B16	DQ3B8	DQ3B17
B8	VREFB8N2	GND								
B8	VREFB8N2	IO			AA9	AF10	DQ3B6	DQ3B15	DQ3B7	DQ3B16
B8	VREFB8N2	IO	LVDS244p		AA10	AC12	DQ3B5	DQ3B14	DQ3B6	DQ3B15
B8	VREFB8N2	IO	LVDS244n		AB10	AD11	DQ3B4	DQ3B13	DQ3B5	DQ3B14
B8	VREFB8N2	GND								
B8	VREFB8N2	IO	LVDS243p		AA11	AF11	DQ3B3	DQ3B12		
B8	VREFB8N2	IO	LVDS243n		Y11	AE11	DQ3B2	DQ3B11		
B8	VREFB8N2	IO	LVDS242p		AE7	AK8	DQ3B1	DQ3B10		
B8	VREFB8N2	VCCIO8								
B8	VREFB8N2	IO	LVDS242n		AF7	AJ8	DQ3B0	DQ3B9	DQ3B4	DQ3B13
B8	VREFB8N1	GND								
B8	VREFB8N1	IO	LVDS241p			AH9			DQ3B3	DQ3B12
B8	VREFB8N1	IO	LVDS241n			AG9			DQ3B2	DQ3B11
B8	VREFB8N1	GND								
B8	VREFB8N1	IO	LVDS240p			AE12			DQ3B1	DQ3B10
B8	VREFB8N1	IO	LVDS240n			AD12			DQ3B0	DQ3B9
B8	VREFB8N1	IO	LVDS239p		AE8	AH10	DPCLK2/DQS3B	DPCLK2/DQS3B	DPCLK2/DQS3B	DPCLK2/DQS3B
B8	VREFB8N1	IO	LVDS239n		AF8	AG10				
B8	VREFB8N1	VCCIO8								
B8	VREFB8N1	IO	LVDS238p			AK9				DM3B0/BWS#3B0

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F672	F896	DQS for x8/x9 in F672	DQS for x16/x18 in F672	DQS for x8/x9 in F896	DQS for x16/x18 in F896
B8	VREFB8N1	GND								
B8	VREFB8N1	IO	LVDS238n			AJ9				DQ3B8
B8	VREFB8N1	IO	LVDS237p		AC9	AK10	DM5B/BWS#5B	DM3B0/BWS#3B0		DQ3B7
B8	VREFB8N1	IO	LVDS237n			AJ10				
B8	VREFB8N1	GND								
B8	VREFB8N1	IO	VREFB8N1		AC10	AF12				
B8	VREFB8N1	IO				AB12				
B8	VREFB8N1	IO	LVDS236p		AE9	AK11	DQ5B8	DQ3B8		DQ3B6
B8	VREFB8N1	IO	LVDS236n		AF9	AJ11	DQ5B7	DQ3B7		DQ3B5
B8	VREFB8N1	VCCIO8								
B8	VREFB8N1	GND								
B8	VREFB8N1	IO	LVDS235p		AD10	AE13	DQ5B6	DQ3B6		DQ3B4
B8	VREFB8N1	IO	LVDS235n		AC11	AD13	DQ5B5	DQ3B5		DQ3B3
B8	VREFB8N1	IO				AC13				DQ3B2
B8	VREFB8N1	GND								
B8	VREFB8N0	IO			AB12	AB13	DQ5B2	DQ3B2		DQ3B1
B8	VREFB8N0	IO	LVDS234p		AE10	AH12	DQ5B4	DQ3B4		DQ3B0
B8	VREFB8N0	IO	LVDS234n		AF10	AG12	DQ5B3	DQ3B3		
B8	VREFB8N0	VCCIO8								
B8	VREFB8N0	IO	LVDS233p		AD11	AK12	DQ5B1	DQ3B1	DM5B/BWS#5B	DM5B1/BWS#5B1
B8	VREFB8N0	GND								
B8	VREFB8N0	IO	LVDS233n		AE11	AJ12	DQ5B0	DQ3B0	DQ5B8	DQ5B17
B8	VREFB8N0	IO				AD14				
B8	VREFB8N0	GND								
B8	VREFB8N0	IO	VREFB8N0		AC12	AG13				
B8	VREFB8N0	IO				AC14				
B8	VREFB8N0	IO	LVDS232p			AG14			DQ5B7	DQ5B16
B8	VREFB8N0	VCCIO8								
B8	VREFB8N0	IO	LVDS232n			AF14			DQ5B6	DQ5B15
B8	VREFB8N0	GND								
B8	VREFB8N0	IO	LVDS231p		AA12	AF15	DM4B	DM5B1/BWS#5B1	DQ5B5	DQ5B14
B8	VREFB8N0	IO	LVDS231n		Y12	AE15		DQ5B17	DQ5B4	DQ5B13
B8	VREFB8N0	GND								
B8	VREFB8N0	IO	LVDS230p		AD12	AJ13	DQ4B7	DQ5B16	DQ5B3	DQ5B12
B8	VREFB8N0	IO	LVDS230n		AE12	AH13	DQ4B6	DQ5B15	DQ5B2	DQ5B11
B8	VREFB8N0	VCCIO8								
B8	VREFB8N0	IO	LVDS229p			AK14			DQ5B1	DQ5B10
B8	VREFB8N0	GND								
B8	VREFB8N0	IO	LVDS229n			AJ14			DQ5B0	DQ5B9
B8	VREFB8N0	IO	LVDS228p		AE13	AJ15	DPCLK3/DQS5B	DPCLK3/DQS5B	DPCLK3/DQS5B	DPCLK3/DQS5B

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F672	F896	DQS for x8/x9 in F672	DQS for x16/x18 in F672	DQS for x8/x9 in F896	DQS for x16/x18 in F896
B8	VREFB8N0	GND								
B8	VREFB8N0	IO	LVDS228n		AF13	AH15				
B8	VREFB8N0	CLK15	LVDSCLK7p/input*(3)*		AC13	AG15				
B8	VREFB8N0	CLK14	LVDSCLK7n/input*(3)*		AD13	AH14				
B7	VREFB7N3	CLK13	LVDSCLK6p/input*(3)*		AF14	AD15				
B7	VREFB7N3	CLK12	LVDSCLK6n/input*(3)*		AE14	AC15				
B7	VREFB7N3	IO	LVDS227p		AE15	AJ16	DPCLK4/DQS4B	DPCLK4/DQS4B	DPCLK4/DQS4B	DPCLK4/DQS4B
B7	VREFB7N3	VCCIO7								
B7	VREFB7N3	IO	LVDS227n		AD15	AH16				
B7	VREFB7N3	GND								
B7	VREFB7N3	IO			AC14	AE16	DQ4B5	DQ5B14	DM4B	DM5B0/BWS#5B0
B7	VREFB7N3	GND								
B7	VREFB7N3	IO	LVDS226p		AA13	AD16	DQ4B4	DQ5B13		DQ5B8
B7	VREFB7N3	IO	LVDS226n		Y13	AC16	DQ4B3	DQ5B12		
B7	VREFB7N3	IO	VREFB7N3		AA14	AG16				
B7	VREFB7N3	IO			Y14	AF16	DQ4B2	DQ5B11		
B7	VREFB7N3	IO	LVDS225p		Y15	AH17	DQ4B1	DQ5B10	DQ4B7	DQ5B7
B7	VREFB7N3	IO	LVDS225n		AA15	AG17	DQ4B0	DQ5B9	DQ4B6	DQ5B6
B7	VREFB7N3	VCCIO7								
B7	VREFB7N3	IO				AE17			DQ4B5	DQ5B5
B7	VREFB7N3	GND								
B7	VREFB7N3	IO	LVDS224p		AB15	AK17			DQ4B4	DQ5B4
B7	VREFB7N3	GND								
B7	VREFB7N3	IO	LVDS224n		AC15	AJ17	DM2B	DM5B0/BWS#5B0	DQ4B3	DQ5B3
B7	VREFB7N2	IO	LVDS223p			AD17			DQ4B2	DQ5B2
B7	VREFB7N2	IO	LVDS223n			AC17			DQ4B1	DQ5B1
B7	VREFB7N2	IO	LVDS222p			AJ18			DQ4B0	DQ5B0
B7	VREFB7N2	VCCIO7								
B7	VREFB7N2	IO	LVDS222n			AH18				
B7	VREFB7N2	GND								
B7	VREFB7N2	GND								
B7	VREFB7N2	IO	LVDS221p		AE16	AK19		DQ5B8		
B7	VREFB7N2	IO	LVDS221n		AD16	AJ19	DQ2B7	DQ5B7		
B7	VREFB7N2	IO	VREFB7N2		AC16	AF17				
B7	VREFB7N2	IO	LVDS220p		AF17	AK20	DQ2B6	DQ5B6	DM2B	
B7	VREFB7N2	VCCIO7								
B7	VREFB7N2	IO	LVDS220n		AE17	AJ20	DQ2B5	DQ5B5		
B7	VREFB7N2	GND								
B7	VREFB7N2	IO	LVDS219p			AH19			DQ2B7	
B7	VREFB7N2	GND								

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F672	F896	DQS for x8/x9 in F672	DQS for x16/x18 in F672	DQS for x8/x9 in F896	DQS for x16/x18 in F896
B7	VREFB7N2	IO	LVDS219n			AG19			DQ2B6	
B7	VREFB7N2	IO	LVDS218p		AC17	AF18	DQ2B4	DQ5B4	DQ2B5	
B7	VREFB7N2	IO	LVDS218n		AD17	AG18	DQ2B3	DQ5B3		
B7	VREFB7N2	IO	LVDS217p		AA16	AD18	DQ2B2	DQ5B2	DQ2B4	
B7	VREFB7N2	IO	LVDS217n		Y16	AC18	DQ2B1	DQ5B1	DQ2B3	
B7	VREFB7N2	VCCIO7								
B7	VREFB7N2	IO	LVDS216p		AF18	AK21	DQ2B0	DQ5B0	DQ2B2	
B7	VREFB7N2	GND								
B7	VREFB7N2	IO	LVDS216n		AE18	AJ21			DQ2B1	
B7	VREFB7N2	GND								
B7	VREFB7N2	IO	LVDS215p			AG20			DQ2B0	
B7	VREFB7N2	IO	LVDS215n			AF20				
B7	VREFB7N2	IO	LVDS214p		AF19	AK22	DPCLK5/DQS2B	DPCLK5/DQS2B	DPCLK5/DQS2B	DPCLK5/DQS2B
B7	VREFB7N2	IO	LVDS214n		AE19	AJ22				
B7	VREFB7N1	IO	LVDS213p		AB18	AB18				
B7	VREFB7N1	IO	LVDS213n		AC18	AB19				
B7	VREFB7N1	VCCIO7								
B7	VREFB7N1	GND								
B7	VREFB7N1	GND								
B7	VREFB7N1	IO	LVDS212p			AD19				
B7	VREFB7N1	IO	LVDS212n			AC19				
B7	VREFB7N1	IO	VREFB7N1		AA17	AH20				
B7	VREFB7N1	IO				AE19				
B7	VREFB7N1	IO	LVDS211p			AK23				
B7	VREFB7N1	IO	LVDS211n		AA18	AJ23				
B7	VREFB7N1	VCCIO7								
B7	VREFB7N1	IO	LVDS210p			AK24				
B7	VREFB7N1	GND								
B7	VREFB7N1	IO	LVDS210n			AJ24				
B7	VREFB7N1	GND								
B7	VREFB7N1	IO	LVDS209p		AD19	AF21	DM0B			
B7	VREFB7N1	IO	LVDS209n		AC19	AE20				
B7	VREFB7N1	IO	LVDS208p		AF20	AH22	DQ0B7			
B7	VREFB7N1	IO	LVDS208n		AE20	AG22	DQ0B6			
B7	VREFB7N1	IO	LVDS207p		AB20	AC20	DQ0B5			
B7	VREFB7N1	IO	LVDS207n		AC20	AD20	DQ0B4			
B7	VREFB7N0	VCCIO7								
B7	VREFB7N0	IO	LVDS206p		AF21	AK25	DQ0B3			
B7	VREFB7N0	GND								
B7	VREFB7N0	IO	LVDS206n		AE21	AJ25			DM0B	

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F672	F896	DQS for x8/x9 in F672	DQS for x16/x18 in F672	DQS for x8/x9 in F896	DQS for x16/x18 in F896
B7	VREFB7N0	GND								
B7	VREFB7N0	IO	LVDS205p			AG23				
B7	VREFB7N0	IO	LVDS205n			AF22			DQ0B7	
B7	VREFB7N0	IO	LVDS204p			AK26			DQ0B6	
B7	VREFB7N0	IO	LVDS204n			AJ26				
B7	VREFB7N0	IO	VREFB7N0		Y18	AD22				
B7	VREFB7N0	IO	LVDS203p		AA20	AH24	DQ0B2			
B7	VREFB7N0	VCCIO7								
B7	VREFB7N0	IO	LVDS203n			AG24			DQ0B5	
B7	VREFB7N0	GND								
B7	VREFB7N0	GND								
B7	VREFB7N0	IO	LVDS202p			AG25			DQ0B4	
B7	VREFB7N0	IO	LVDS202n			AH26			DQ0B3	
B7	VREFB7N0	IO	LVDS201p			AD21				
B7	VREFB7N0	IO	LVDS201n			AC21			DQ0B2	
B7	VREFB7N0	IO	LVDS200p		AF22	AK28	DQ0B1		DQ0B1	
B7	VREFB7N0	VCCIO7								
B7	VREFB7N0	IO	LVDS200n		AE22	AJ28	DQ0B0		DQ0B0	
B7	VREFB7N0	GND								
B7	VREFB7N0	IO	LVDS199p		AC21	AF23	CDPCLK3/DQS0B	CDPCLK3/DQS0B	CDPCLK3/DQS0B	CDPCLK3/DQS0B
B7	VREFB7N0	IO	LVDS199n		AD21	AF24				
B7	VREFB7N0	VCCIO7								
B7	VREFB7N0	IO	LVDS198p		AD23	AJ27				
B7	VREFB7N0	IO	LVDS198n		AD22	AH27				
B7	VREFB7N0	IO	LVDS197p		AC22	AG27				
B7	VREFB7N0	IO	LVDS197n		AB21	AG26				
B7	VREFB7N0	IO	LVDS196p		AF23	AE23				
B7	VREFB7N0	IO	LVDS196n		AE23	AE24				
B7	VREFB7N0	GND								
B7	VREFB7N0	GNDA_PLL4			Y19	AD23				
B7	VREFB7N0	VCCA_PLL4			AA19	AC22				
B6	VREFB6N3	GND_PLL4			AA21	AA21				
B6	VREFB6N3	VCCD_PLL4			Y20	AB22				
B6	VREFB6N3	GND_PLL4			W20	AA22				
B6	VREFB6N3	GND								
B6	VREFB6N3	IO			AC23	AB23				
B6	VREFB6N3	IO	LVDS195n	INIT_DONE	AE25	AD24				
B6	VREFB6N3	IO	LVDS195p	nCEO	AE24	AD25				
B6	VREFB6N3	IO	LVDS194n		AD25	AC23				
B6	VREFB6N3	IO	LVDS194p		AD24	AC24				

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F672	F896	DQS for x8/x9 in F672	DQS for x16/x18 in F672	DQS for x8/x9 in F896	DQS for x16/x18 in F896
B6	VREFB6N3	IO			AC24	AB24				
B6	VREFB6N3	IO	PLL4_OUTn		V20	AF27				
B6	VREFB6N3	VCCIO6								
B6	VREFB6N3	IO	PLL4_OUTp		V21	AF28				
B6	VREFB6N3	IO			Y21	AD26				
B6	VREFB6N3	IO	VREFB6N3		Y22	AD27				
B6	VREFB6N3	IO	LVDS193n		W21	AC25				
B6	VREFB6N3	IO	LVDS193p			AC26				
B6	VREFB6N3	GND								
B6	VREFB6N3	IO	LVDS192n			AG29				
B6	VREFB6N3	IO	LVDS192p			AG28				
B6	VREFB6N2	IO	LVDS191n		AA24	AH29				
B6	VREFB6N2	IO	LVDS191p		AA23	AH28				
B6	VREFB6N2	VCCIO6								
B6	VREFB6N2	IO	LVDS190n		AB24	AH30				
B6	VREFB6N2	IO	LVDS190p		AB23	AJ29				
B6	VREFB6N2	IO	LVDS189n		AC25	AE27				
B6	VREFB6N2	IO	LVDS189p		AC26	AE28				
B6	VREFB6N2	GND								
B6	VREFB6N2	IO	VREFB6N2		V22	AD28				
B6	VREFB6N2	GND								
B6	VREFB6N2	IO	LVDS188n		AB26	AA24				
B6	VREFB6N2	IO	LVDS188p		AB25	AA23				
B6	VREFB6N2	IO	LVDS187n		Y24	AB25				
B6	VREFB6N2	IO	LVDS187p		Y23	AB26				
B6	VREFB6N2	IO	LVDS186n		AA25	AF29				
B6	VREFB6N2	VCCIO6								
B6	VREFB6N2	IO	LVDS186p		AA26	AF30				
B6	VREFB6N2	IO	LVDS185n		Y26	Y24	DM3R/BWS#3R	DM3R1/BWS#3R1	DM3R/BWS#3R	DM3R1/BWS#3R1
B6	VREFB6N2	IO	LVDS185p		Y25	Y23	DQ3R8	DQ3R17	DQ3R8	DQ3R17
B6	VREFB6N2	IO			U22	AA25	DQ3R7	DQ3R16		
B6	VREFB6N2	GND								
B6	VREFB6N2	IO	LVDS184n			Y22			DQ3R7	DQ3R16
B6	VREFB6N2	IO	LVDS184p			Y21				
B6	VREFB6N2	IO	LVDS183n		W24	AC27	DQ3R6	DQ3R15	DQ3R6	DQ3R15
B6	VREFB6N2	IO	LVDS183p		W23	AC28	DQ3R5	DQ3R14		
B6	VREFB6N2	IO	LVDS182n			AE29			DQ3R5	DQ3R14
B6	VREFB6N2	IO	LVDS182p			AE30				
B6	VREFB6N2	IO	LVDS181n		W25	AD29				
B6	VREFB6N2	VCCIO6								

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F672	F896	DQS for x8/x9 in F672	DQS for x16/x18 in F672	DQS for x8/x9 in F896	DQS for x16/x18 in F896
B6	VREFB6N2	IO	LVDS181p		W26	AD30	CDPCLK4/DQS3R	CDPCLK4/DQS3R	CDPCLK4/DQS3R	CDPCLK4/DQS3R
B6	VREFB6N1	IO	LVDS180n		V23	AA26	DQ3R4	DQ3R13	DQ3R4	DQ3R13
B6	VREFB6N1	IO	LVDS180p		V24	AA27	DQ3R3	DQ3R12	DQ3R3	DQ3R12
B6	VREFB6N1	IO	LVDS179n		V25	W23	DQ3R2	DQ3R11	DQ3R2	DQ3R11
B6	VREFB6N1	IO	LVDS179p		V26	W24	DQ3R1	DQ3R10	DQ3R1	DQ3R10
B6	VREFB6N1	GND								
B6	VREFB6N1	IO	LVDS178n			Y26			DQ3R0	DQ3R9
B6	VREFB6N1	IO	LVDS178p			Y25				
B6	VREFB6N1	IO				W26				
B6	VREFB6N1	GND								
B6	VREFB6N1	IO	LVDS177n		U21	W22	DQ3R0	DQ3R9		
B6	VREFB6N1	IO	LVDS177p		U20	W21				
B6	VREFB6N1	IO	LVDS176n			AC29				
B6	VREFB6N1	IO	LVDS176p			AC30			DM1R/BWS#1R	DM3R0/BWS#3R0
B6	VREFB6N1	VCCIO6								
B6	VREFB6N1	IO	LVDS175n		U24	W25			DQ1R8	DQ3R8
B6	VREFB6N1	IO	LVDS175p		U23	V24	DM1R/BWS#1R	DM3R0/BWS#3R0		
B6	VREFB6N1	IO	VREFB6N1		T21	AA28				
B6	VREFB6N1	IO				V22				
B6	VREFB6N1	IO	LVDS174n		U25	AB29	DQ1R8	DQ3R8		
B6	VREFB6N1	GND								
B6	VREFB6N1	IO	LVDS174p		U26	AB30	DQ1R7	DQ3R7		
B6	VREFB6N1	IO			T20	V21	DQ1R6	DQ3R6	DQ1R7	DQ3R7
B6	VREFB6N1	IO	LVDS173n			Y28			DQ1R6	DQ3R6
B6	VREFB6N1	IO	LVDS173p			Y27			DQ1R5	DQ3R5
B6	VREFB6N1	IO	LVDS172n			AA29			DQ1R4	DQ3R4
B6	VREFB6N1	VCCIO6								
B6	VREFB6N1	IO	LVDS172p			AA30				
B6	VREFB6N1	IO	LVDS171n			W27				
B6	VREFB6N1	IO	LVDS171p			W28				
B6	VREFB6N1	IO	LVDS170n		T25	Y29	DQ1R5	DQ3R5		
B6	VREFB6N1	IO	LVDS170p		T24	Y30	DQ1R4	DQ3R4		
B6	VREFB6N0	IO				V23				
B6	VREFB6N0	GND								
B6	VREFB6N0	IO	LVDS169n			W29				
B6	VREFB6N0	GND								
B6	VREFB6N0	IO	LVDS169p			W30			DQ1R3	DQ3R3
B6	VREFB6N0	GND								
B6	VREFB6N0	IO	LVDS168n			V28			DQ1R2	DQ3R2
B6	VREFB6N0	IO	LVDS168p			V29				

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F672	F896	DQS for x8/x9 in F672	DQS for x16/x18 in F672	DQS for x8/x9 in F896	DQS for x16/x18 in F896
B6	VREFB6N0	IO	VREFB6N0		T23	V27				
B6	VREFB6N0	IO				U25				
B6	VREFB6N0	VCCIO6								
B6	VREFB6N0	IO	LVDS167n			U24			DQ1R1	DQ3R1
B6	VREFB6N0	IO	LVDS167p		T22	U23	DQ1R3	DQ3R3	DQ1R0	DQ3R0
B6	VREFB6N0	IO	LVDS166n			U29				
B6	VREFB6N0	IO	LVDS166p		R20	U30	DQ1R2	DQ3R2		
B6	VREFB6N0	nSTATUS		nSTATUS	R22	U26				
B6	VREFB6N0	GND								
B6	VREFB6N0	CONF_DONE		CONF_DONE	R23	U27				
B6	VREFB6N0	GND								
B6	VREFB6N0	MSEL1		MSEL1	P21	U28				
B6	VREFB6N0	MSEL0		MSEL0	P20	U22				
B6	VREFB6N0	IO	LVDS165n		R24	T28	DQ1R1	DQ3R1	DM0R	DM1R1/BWS#1R1
B6	VREFB6N0	IO	LVDS165p		R25	T29	DQ1R0	DQ3R0		DQ1R17
B6	VREFB6N0	VCCIO6								
B6	VREFB6N0	IO	LVDS164n		P24	T27				
B6	VREFB6N0	IO	LVDS164p		P23	T26	DPCLK6/DQS1R	DPCLK6/DQS1R	DPCLK6/DQS1R	DPCLK6/DQS1R
B6	VREFB6N0	CLK7	LVDSCLK3n/input*(3)*		P26	T25				
B6	VREFB6N0	CLK6	LVDSCLK3p/input*(3)*		P25	T24				
B5	VREFB5N3	CLK5	LVDSCLK2n/input*(3)*		N26	R28				
B5	VREFB5N3	CLK4	LVDSCLK2p/input*(3)*		N25	R29				
B5	VREFB5N3	IO	LVDS163n		N24	T23				
B5	VREFB5N3	IO	LVDS163p		N23	T22	DPCLK7/DQS0R	DPCLK7/DQS0R	DPCLK7/DQS0R	DPCLK7/DQS0R
B5	VREFB5N3	IO			N21	R24				
B5	VREFB5N3	GND								
B5	VREFB5N3	IO	LVDS162n		M25	R26	DM0R	DM1R1/BWS#1R1	DQ0R7	DQ1R16
B5	VREFB5N3	VCCIO5								
B5	VREFB5N3	IO	LVDS162p		M24	R27		DQ1R17	DQ0R6	DQ1R15
B5	VREFB5N3	IO	LVDS161n			R23			DQ0R5	DQ1R14
B5	VREFB5N3	IO	LVDS161p			R22				
B5	VREFB5N3	IO	VREFB5N3		M21	R25				
B5	VREFB5N3	GND								
B5	VREFB5N3	IO	LVDS160n			P29			DQ0R4	DQ1R13
B5	VREFB5N3	GND								
B5	VREFB5N3	IO	LVDS160p		N20	P30	DQ0R7	DQ1R16	DQ0R3	DQ1R12
B5	VREFB5N3	IO	LVDS159n			P28				
B5	VREFB5N3	IO	LVDS159p			P27			DQ0R2	DQ1R11
B5	VREFB5N3	IO	LVDS158n		M20	P26	DQ0R6	DQ1R15	DQ0R1	DQ1R10
B5	VREFB5N3	IO	LVDS158p		M19	P25	DQ0R5	DQ1R14	DQ0R0	DQ1R9

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F672	F896	DQS for x8/x9 in F672	DQS for x16/x18 in F672	DQS for x8/x9 in F896	DQS for x16/x18 in F896
B5	VREFB5N3	VCCIO5								
B5	VREFB5N3	IO	LVDS157n		M23	P24	DQ0R4	DQ1R13		
B5	VREFB5N3	IO	LVDS157p		M22	P23	DQ0R3	DQ1R12		
B5	VREFB5N3	IO	LVDS156n		K26	N28	DQ0R2	DQ1R11		
B5	VREFB5N3	GND								
B5	VREFB5N3	IO	LVDS156p		K25	N29	DQ0R1	DQ1R10		
B5	VREFB5N2	GND								
B5	VREFB5N2	IO	LVDS155n			N25				
B5	VREFB5N2	IO	LVDS155p			N24				
B5	VREFB5N2	IO	LVDS154n			M29				
B5	VREFB5N2	IO	LVDS154p			M30				
B5	VREFB5N2	IO			L19	P22	DQ0R0	DQ1R9		DM1R0/BWS#1R0
B5	VREFB5N2	IO	LVDS153n		L25	N22				DQ1R8
B5	VREFB5N2	IO	LVDS153p		L24	N21				DQ1R7
B5	VREFB5N2	VCCIO5								
B5	VREFB5N2	IO	VREFB5N2		L23	M28				
B5	VREFB5N2	IO	LVDS152n		J26	L29				
B5	VREFB5N2	GND								
B5	VREFB5N2	IO	LVDS152p		J25	L30				DQ1R6
B5	VREFB5N2	GND								
B5	VREFB5N2	IO	LVDS151n		L20	K29				DQ1R5
B5	VREFB5N2	IO	LVDS151p		L21	K30				
B5	VREFB5N2	IO	LVDS150n		K24	L28	DM2R	DM1R0/BWS#1R0	DM2R	DQ1R4
B5	VREFB5N2	IO	LVDS150p		K23	L27		DQ1R8		DQ1R3
B5	VREFB5N2	IO			K21	M26	DQ2R7	DQ1R7	DQ2R7	DQ1R2
B5	VREFB5N2	IO			K19	M27	DQ2R6	DQ1R6	DQ2R6	DQ1R1
B5	VREFB5N2	IO	LVDS149n		H26	J29	DQ2R5	DQ1R5	DQ2R5	DQ1R0
B5	VREFB5N2	VCCIO5								
B5	VREFB5N2	IO	LVDS149p		H25	J30	DQ2R4	DQ1R4	DQ2R4	
B5	VREFB5N2	IO	LVDS148n			M21				
B5	VREFB5N2	IO	LVDS148p			M22				
B5	VREFB5N2	GND								
B5	VREFB5N2	IO	LVDS147n		J24	M23	DQ2R3	DQ1R3	DQ2R3	
B5	VREFB5N2	IO	LVDS147p		J23	N23	DQ2R2	DQ1R2	DQ2R2	
B5	VREFB5N2	IO	LVDS146n		H24	K27	DQ2R1	DQ1R1	DQ2R1	
B5	VREFB5N2	IO	LVDS146p		H23	K28	DQ2R0	DQ1R0	DQ2R0	
B5	VREFB5N1	IO	LVDS145n		G26	M25				
B5	VREFB5N1	IO	LVDS145p		G25	M24	CDPCLK5/DQS2R	CDPCLK5/DQS2R	CDPCLK5/DQS2R	CDPCLK5/DQS2R
B5	VREFB5N1	IO			K22	L26				
B5	VREFB5N1	VCCIO5								

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F672	F896	DQS for x8/x9 in F672	DQS for x16/x18 in F672	DQS for x8/x9 in F896	DQS for x16/x18 in F896
B5	VREFB5N1	IO	LVDS144n		G24	L22				
B5	VREFB5N1	IO	LVDS144p		G23	L21				
B5	VREFB5N1	IO				K26				
B5	VREFB5N1	GND								
B5	VREFB5N1	IO	LVDS143n		F26	H29				
B5	VREFB5N1	GND								
B5	VREFB5N1	IO	LVDS143p		F25	H30				
B5	VREFB5N1	IO				K23				
B5	VREFB5N1	IO	LVDS142n		J20	L24				
B5	VREFB5N1	IO	LVDS142p		J21	L25				
B5	VREFB5N1	IO	LVDS141n		F23	G29				
B5	VREFB5N1	IO	LVDS141p		F24	G30				
B5	VREFB5N1	VCCIO5								
B5	VREFB5N1	IO	VREFB5N1		J22	J26				
B5	VREFB5N1	IO	LVDS140n			K24				
B5	VREFB5N1	IO	LVDS140p			K25				
B5	VREFB5N1	IO	LVDS139n		E25	F29				
B5	VREFB5N1	IO	LVDS139p		E26	F30				
B5	VREFB5N1	GND								
B5	VREFB5N1	IO				H26				
B5	VREFB5N1	IO	LVDS138n		D25	H27				
B5	VREFB5N1	IO	LVDS138p		D26	H28				
B5	VREFB5N1	IO	LVDS137n			G27				
B5	VREFB5N1	IO	LVDS137p			G28				
B5	VREFB5N1	IO	LVDS136n		C24	E29				
B5	VREFB5N1	IO	LVDS136p		C25	E30				
B5	VREFB5N1	VCCIO5								
B5	VREFB5N0	IO	LVDS135n			C30				
B5	VREFB5N0	IO	LVDS135p			C29				
B5	VREFB5N0	IO	LVDS134n		B25	D29				
B5	VREFB5N0	IO	LVDS134p		B24	D28				
B5	VREFB5N0	IO				F27				
B5	VREFB5N0	GND								
B5	VREFB5N0	IO	LVDS133n		E24	E28				
B5	VREFB5N0	IO	LVDS133p		E23	E27				
B5	VREFB5N0	IO	LVDS132n			J25				
B5	VREFB5N0	IO	LVDS132p			J24				
B5	VREFB5N0	IO	VREFB5N0		H21	F28				
B5	VREFB5N0	VCCIO5								
B5	VREFB5N0	IO	LVDS131n		G22	G25				

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F672	F896	DQS for x8/x9 in F672	DQS for x16/x18 in F672	DQS for x8/x9 in F896	DQS for x16/x18 in F896
B5	VREFB5N0	IO	LVDS131p		G21	G26				
B5	VREFB5N0	IO	LVDS130n		D23	H25				
B5	VREFB5N0	IO	LVDS130p		E22	H24				
B5	VREFB5N0	IO	PLL2_OUTp		F21	G24				
B5	VREFB5N0	IO	PLL2_OUTn		F20	H23				
B5	VREFB5N0	GND								
B5	VREFB5N0	GND_PLL2			G20	K22				
B5	VREFB5N0	VCCD_PLL2			H20	J22				
B5	VREFB5N0	GND_PLL2			E21	K21				
B4	VREFB4N0	VCCA_PLL2			G19	H22				
B4	VREFB4N0	GNDA_PLL2			F19	G23				
B4	VREFB4N0	GND								
B4	VREFB4N0	IO	LVDS129n		C23	F23				
B4	VREFB4N0	IO	LVDS129p		C22	G22				
B4	VREFB4N0	IO	LVDS128n		C21	E24				
B4	VREFB4N0	IO	LVDS128p		D21	F24				
B4	VREFB4N0	IO	LVDS127n		B23	C28				
B4	VREFB4N0	IO	LVDS127p		A23	B29				
B4	VREFB4N0	VCCIO4								
B4	VREFB4N0	IO	LVDS126n		A22	D26				
B4	VREFB4N0	IO	LVDS126p		B22	D27	CDPCLK6/DQS0T	CDPCLK6/DQS0T	CDPCLK6/DQS0T	CDPCLK6/DQS0T
B4	VREFB4N0	GND								
B4	VREFB4N0	IO	LVDS125n		B21	B28	DQ0T0		DQ0T0	
B4	VREFB4N0	VCCIO4								
B4	VREFB4N0	IO	LVDS125p		A21	A28	DQ0T1		DQ0T1	
B4	VREFB4N0	IO	LVDS124n			C27			DQ0T2	
B4	VREFB4N0	IO	LVDS124p			B27			DQ0T3	
B4	VREFB4N0	IO	LVDS123n			G21			DQ0T4	
B4	VREFB4N0	IO	LVDS123p			H21			DQ0T5	
B4	VREFB4N0	GND								
B4	VREFB4N0	GND								
B4	VREFB4N0	IO	LVDS122n			B26			DQ0T6	
B4	VREFB4N0	VCCIO4								
B4	VREFB4N0	IO	LVDS122p		D20	A26	DQ0T2			
B4	VREFB4N0	IO	VREFB4N0		E20	C26				
B4	VREFB4N0	IO	LVDS121n			E23				
B4	VREFB4N0	IO	LVDS121p			E22			DQ0T7	
B4	VREFB4N0	IO	LVDS120n			D25			DM0T	
B4	VREFB4N0	IO	LVDS120p			D24				
B4	VREFB4N0	GND								

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F672	F896	DQS for x8/x9 in F672	DQS for x16/x18 in F672	DQS for x8/x9 in F896	DQS for x16/x18 in F896
B4	VREFB4N0	IO	LVDS119n		B20	B25				
B4	VREFB4N0	GND								
B4	VREFB4N0	IO	LVDS119p		A20	A25	DQ0T3			
B4	VREFB4N0	VCCIO4								
B4	VREFB4N1	IO	LVDS118n		C19	G20	DQ0T4			
B4	VREFB4N1	IO	LVDS118p		D19	H20	DQ0T5			
B4	VREFB4N1	IO	LVDS117n		B19	B24	DQ0T6			
B4	VREFB4N1	IO	LVDS117p		A19	A24	DQ0T7			
B4	VREFB4N1	IO	LVDS116n		E18	D23				
B4	VREFB4N1	IO	LVDS116p		D18	C24	DM0T			
B4	VREFB4N1	GND								
B4	VREFB4N1	IO	LVDS115n			B23				
B4	VREFB4N1	GND								
B4	VREFB4N1	IO	LVDS115p			A23				
B4	VREFB4N1	VCCIO4								
B4	VREFB4N1	IO	LVDS114n		G18	D22				
B4	VREFB4N1	IO	LVDS114p			C22				
B4	VREFB4N1	IO				G19				
B4	VREFB4N1	IO	VREFB4N1		F18	C21				
B4	VREFB4N1	IO	LVDS113n			J19				
B4	VREFB4N1	IO	LVDS113p			H19				
B4	VREFB4N1	GND								
B4	VREFB4N1	GND								
B4	VREFB4N1	VCCIO4								
B4	VREFB4N1	IO	LVDS112n		F17	E21				
B4	VREFB4N1	IO	LVDS112p		G17	D21				
B4	VREFB4N2	IO	LVDS111n		D17	B22				
B4	VREFB4N2	IO	LVDS111p		C17	A22	DPCLK8/DQS2T	DPCLK8/DQS2T	DPCLK8/DQS2T	DPCLK8/DQS2T
B4	VREFB4N2	IO	LVDS110n			F20				
B4	VREFB4N2	IO	LVDS110p			E20			DQ2T0	
B4	VREFB4N2	GND								
B4	VREFB4N2	IO	LVDS109n		B18	B21			DQ2T1	
B4	VREFB4N2	GND								
B4	VREFB4N2	IO	LVDS109p		A18	A21	DQ2T0	DQ5T0	DQ2T2	
B4	VREFB4N2	VCCIO4								
B4	VREFB4N2	IO	LVDS108n		G16	F19	DQ2T1	DQ5T1	DQ2T3	
B4	VREFB4N2	IO	LVDS108p		F16	E19	DQ2T2	DQ5T2	DQ2T4	
B4	VREFB4N2	IO	LVDS107n		F15	H18	DQ2T3	DQ5T3		
B4	VREFB4N2	IO	LVDS107p		G15	J18	DQ2T4	DQ5T4	DQ2T5	
B4	VREFB4N2	IO	LVDS106n			D19			DQ2T6	

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F672	F896	DQS for x8/x9 in F672	DQS for x16/x18 in F672	DQS for x8/x9 in F896	DQS for x16/x18 in F896
B4	VREFB4N2	GND								
B4	VREFB4N2	IO	LVDS106p			C19			DQ2T7	
B4	VREFB4N2	GND								
B4	VREFB4N2	IO	LVDS105n		B17	B20	DQ2T5	DQ5T5		
B4	VREFB4N2	VCCIO4								
B4	VREFB4N2	IO	LVDS105p		A17	A20	DQ2T6	DQ5T6	DM2T	
B4	VREFB4N2	IO	VREFB4N2		D16	D18				
B4	VREFB4N2	IO	LVDS104n		E15	G18	DQ2T7	DQ5T7		
B4	VREFB4N2	IO	LVDS104p		D15	F18		DQ5T8		
B4	VREFB4N2	GND								
B4	VREFB4N2	GND								
B4	VREFB4N2	IO	LVDS103n			B19				
B4	VREFB4N2	VCCIO4								
B4	VREFB4N2	IO	LVDS103p			A19			DQ4T0	DQ5T0
B4	VREFB4N2	IO	LVDS102n			C18			DQ4T1	DQ5T1
B4	VREFB4N2	IO	LVDS102p			B18			DQ4T2	DQ5T2
B4	VREFB4N3	IO	LVDS101n		C16	B17	DM2T	DM5T0/BWS#5T0	DQ4T3	DQ5T3
B4	VREFB4N3	GND								
B4	VREFB4N3	IO	LVDS101p		B16	A17	DQ4T0	DQ5T9	DQ4T4	DQ5T4
B4	VREFB4N3	GND								
B4	VREFB4N3	IO				E17			DQ4T5	DQ5T5
B4	VREFB4N3	VCCIO4								
B4	VREFB4N3	IO	LVDS100n		B15	G17	DQ4T1	DQ5T10	DQ4T6	DQ5T6
B4	VREFB4N3	IO	LVDS100p		C15	H17	DQ4T2	DQ5T11	DQ4T7	DQ5T7
B4	VREFB4N3	IO			G13	D17	DQ4T3	DQ5T12		
B4	VREFB4N3	IO	VREFB4N3		F13	C17				
B4	VREFB4N3	IO	LVDS99n		G14	G16	DQ4T4	DQ5T13		
B4	VREFB4N3	IO	LVDS99p		F14	F16	DQ4T5	DQ5T14		DQ5T8
B4	VREFB4N3	GND								
B4	VREFB4N3	IO			D14	H16	DQ4T6	DQ5T15	DM4T	DM5T0/BWS#5T0
B4	VREFB4N3	GND								
B4	VREFB4N3	IO	LVDS98n		A14	C16				
B4	VREFB4N3	VCCIO4								
B4	VREFB4N3	IO	LVDS98p		B14	B16	DPCLK9/DQS4T	DPCLK9/DQS4T	DPCLK9/DQS4T	DPCLK9/DQS4T
B4	VREFB4N3	CLK8	LVDSCLK4n/input*(3)*		B13	E16				
B4	VREFB4N3	CLK9	LVDSCLK4p/input*(3)*		A13	D16				
B3	VREFB3N0	CLK10	LVDSCLK5n/input*(3)*		C13	G15				
B3	VREFB3N0	CLK11	LVDSCLK5p/input*(3)*		D13	H15				
B3	VREFB3N0	IO	LVDS97n		B12	C15				
B3	VREFB3N0	GND								

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F672	F896	DQS for x8/x9 in F672	DQS for x16/x18 in F672	DQS for x8/x9 in F896	DQS for x16/x18 in F896
B3	VREFB3N0	IO	LVDS97p		C12	B15	DPCLK10/DQS5T	DPCLK10/DQS5T	DPCLK10/DQS5T	DPCLK10/DQS5T
B3	VREFB3N0	IO	LVDS96n			E15			DQ5T0	DQ5T9
B3	VREFB3N0	GND								
B3	VREFB3N0	IO	LVDS96p			D15			DQ5T1	DQ5T10
B3	VREFB3N0	VCCIO3								
B3	VREFB3N0	IO	LVDS95n		B11	B14	DQ4T7	DQ5T16	DQ5T2	DQ5T11
B3	VREFB3N0	IO	LVDS95p		C11	A14		DQ5T17	DQ5T3	DQ5T12
B3	VREFB3N0	GND								
B3	VREFB3N0	IO	LVDS94n		G12	E14	DM4T	DM5T1/BWS#5T1	DQ5T4	DQ5T13
B3	VREFB3N0	IO	LVDS94p		F12	D14	DQ5T0	DQ3T0	DQ5T5	DQ5T14
B3	VREFB3N0	GND								
B3	VREFB3N0	IO	LVDS93n			C13			DQ5T6	DQ5T15
B3	VREFB3N0	VCCIO3								
B3	VREFB3N0	IO	LVDS93p			B13			DQ5T7	DQ5T16
B3	VREFB3N0	IO				H14			DQ5T8	DQ5T17
B3	VREFB3N0	IO	VREFB3N0		D11	C14				
B3	VREFB3N0	GND								
B3	VREFB3N0	IO				G14			DM5T/BWS#5T	DM5T1/BWS#5T1
B3	VREFB3N0	IO	LVDS92n		D12	B12	DQ5T1	DQ3T1		
B3	VREFB3N0	GND								
B3	VREFB3N0	IO	LVDS92p		E12	A12	DQ5T2	DQ3T2		
B3	VREFB3N0	VCCIO3								
B3	VREFB3N0	IO	LVDS91n		A10	E13	DQ5T4	DQ3T4		DQ3T0
B3	VREFB3N0	IO	LVDS91p		B10	F13	DQ5T5	DQ3T5		DQ3T1
B3	VREFB3N0	IO			G11	J13	DQ5T3	DQ3T3		
B3	VREFB3N1	GND								
B3	VREFB3N1	IO				G13				DQ3T2
B3	VREFB3N1	IO	LVDS90n		D10	D12	DQ5T6	DQ3T6		DQ3T3
B3	VREFB3N1	IO	LVDS90p		C10	C12	DQ5T7	DQ3T7		DQ3T4
B3	VREFB3N1	GND								
B3	VREFB3N1	VCCIO3								
B3	VREFB3N1	IO	LVDS89n		A9	B11	DQ5T8	DQ3T8		DQ3T5
B3	VREFB3N1	IO	LVDS89p		B9	A11	DM5T/BWS#5T	DM3T0/BWS#3T0		DQ3T6
B3	VREFB3N1	IO				H13				
B3	VREFB3N1	IO	VREFB3N1		E10	D13				
B3	VREFB3N1	GND								
B3	VREFB3N1	IO	LVDS88n			E12				
B3	VREFB3N1	IO	LVDS88p		F11	F12	DQ3T0	DQ3T9		DQ3T7
B3	VREFB3N1	IO	LVDS87n			B10				DQ3T8
B3	VREFB3N1	GND								

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F672	F896	DQS for x8/x9 in F672	DQS for x16/x18 in F672	DQS for x8/x9 in F896	DQS for x16/x18 in F896
B3	VREFB3N1	IO	LVDS87p			A10				DM3T0/BWS#3T0
B3	VREFB3N1	VCCIO3								
B3	VREFB3N1	IO	LVDS86n		A8	B9				
B3	VREFB3N1	IO	LVDS86p		B8	A9	DPCLK11/DQS3T	DPCLK11/DQS3T	DPCLK11/DQS3T	DPCLK11/DQS3T
B3	VREFB3N1	IO	LVDS85n			F11				
B3	VREFB3N1	IO	LVDS85p			E11			DQ3T0	DQ3T9
B3	VREFB3N1	GND								
B3	VREFB3N1	IO	LVDS84n			G12			DQ3T1	DQ3T10
B3	VREFB3N1	IO	LVDS84p			H12			DQ3T2	DQ3T11
B3	VREFB3N1	GND								
B3	VREFB3N2	IO	LVDS83n		C9	D10	DQ3T1	DQ3T10	DQ3T3	DQ3T12
B3	VREFB3N2	VCCIO3								
B3	VREFB3N2	IO	LVDS83p		D9	C10	DQ3T2	DQ3T11	DQ3T4	DQ3T13
B3	VREFB3N2	IO	LVDS82n		G10	J12	DQ3T3	DQ3T12	DQ3T5	DQ3T14
B3	VREFB3N2	IO	LVDS82p		F10	H11	DQ3T4	DQ3T13	DQ3T6	DQ3T15
B3	VREFB3N2	GND								
B3	VREFB3N2	IO	LVDS81n		C8	C9	DQ3T5	DQ3T14	DQ3T7	DQ3T16
B3	VREFB3N2	IO	LVDS81p		D8	D9	DQ3T6	DQ3T15	DQ3T8	DQ3T17
B3	VREFB3N2	IO	LVDS80n		A7	B8	DQ3T7	DQ3T16		
B3	VREFB3N2	GND								
B3	VREFB3N2	IO	LVDS80p		B7	A8	DQ3T8	DQ3T17	DM3T/BWS#3T	DM3T1/BWS#3T1
B3	VREFB3N2	VCCIO3								
B3	VREFB3N2	IO			D6	E10	DM3T/BWS#3T	DM3T1/BWS#3T1		
B3	VREFB3N2	IO	LVDS79n		C7	D8	DQ1T0			
B3	VREFB3N2	IO	LVDS79p		D7	E9	DQ1T1			
B3	VREFB3N2	IO			F9	G11	DQ1T2			
B3	VREFB3N2	GND								
B3	VREFB3N2	IO	LVDS78n		G9	B7	DQ1T3			
B3	VREFB3N2	GND								
B3	VREFB3N2	IO	LVDS78p			A7				
B3	VREFB3N2	VCCIO3								
B3	VREFB3N2	IO	VREFB3N2		E8	C7				
B3	VREFB3N2	IO	LVDS77n			B6				
B3	VREFB3N2	IO	LVDS77p			A6				
B3	VREFB3N2	GND								
B3	VREFB3N2	IO	LVDS76n			D7				
B3	VREFB3N2	IO	LVDS76p			D6			DQ1T0	
B3	VREFB3N3	IO	LVDS75n			B5			DQ1T1	
B3	VREFB3N3	GND								
B3	VREFB3N3	IO	LVDS75p			A5			DQ1T2	

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F672	F896	DQS for x8/x9 in F672	DQS for x16/x18 in F672	DQS for x8/x9 in F896	DQS for x16/x18 in F896
B3	VREFB3N3	VCCIO3								
B3	VREFB3N3	IO	LVDS74n			C4			DQ1T3	
B3	VREFB3N3	IO	LVDS74p			B4			DQ1T4	
B3	VREFB3N3	IO	LVDS73n			H10			DQ1T5	
B3	VREFB3N3	IO	LVDS73p			G10				
B3	VREFB3N3	GND								
B3	VREFB3N3	IO	VREFB3N3		D5	C5				
B3	VREFB3N3	IO			C4	G9	DQ1T4			
B3	VREFB3N3	IO	LVDS72n		A6	B3				
B3	VREFB3N3	GND								
B3	VREFB3N3	IO	LVDS72p		B6	A3	CDPCLK7/DQS1T	CDPCLK7/DQS1T	CDPCLK7/DQS1T	CDPCLK7/DQS1T
B3	VREFB3N3	VCCIO3								
B3	VREFB3N3	IO	LVDS71n		B5	E8	DQ1T5		DQ1T6	
B3	VREFB3N3	IO	LVDS71p		A5	F8	DQ1T6		DQ1T7	
B3	VREFB3N3	IO	LVDS70n		B4	E7	DQ1T7		DM1T	
B3	VREFB3N3	IO	LVDS70p		A4	F7	DM1T			
B3	VREFB3N3	IO	LVDS69p		C6	D5				
B3	VREFB3N3	IO	LVDS69n	DEV_CLRn	C5	D4				
B3	VREFB3N3	GND								
B3	VREFB3N3	GNDA_PLL3			F8	G8				
B3	VREFB3N3	VCCA_PLL3			G8	H9				
		VCCINT			H10	AA13				
		VCCINT			H11	AA14				
		VCCINT			H15	AA17				
		VCCINT			H16	AA18				
		VCCINT			H17	K13				
		VCCINT			H19	K14				
		VCCINT			J9	K17				
		VCCINT			J18	K18				
		VCCINT			K9	L13				
		VCCINT			K10	L14				
		VCCINT			K11	L15				
		VCCINT			K12	L16				
		VCCINT			K13	L17				
		VCCINT			K14	L18				
		VCCINT			K15	L19				
		VCCINT			K18	M12				
		VCCINT			L9	M13				
		VCCINT			L11	M14				
		VCCINT			L16	M15				

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F672	F896	DQS for x8/x9 in F672	DQS for x16/x18 in F672	DQS for x8/x9 in F896	DQS for x16/x18 in F896
		VCCINT			L17	M17				
		VCCINT			L18	M18				
		VCCINT			M10	M19				
		VCCINT			M11	N11				
		VCCINT			M16	N12				
		VCCINT			M17	N19				
		VCCINT			N10	N20				
		VCCINT			N17	P11				
		VCCINT			P10	P12				
		VCCINT			P17	P19				
		VCCINT			R8	P20				
		VCCINT			R10	R12				
		VCCINT			R11	R19				
		VCCINT			R16	T12				
		VCCINT			R19	T19				
		VCCINT			T8	U11				
		VCCINT			T9	U12				
		VCCINT			T11	U19				
		VCCINT			T16	U20				
		VCCINT			T18	V11				
		VCCINT			T19	V12				
		VCCINT			U9	V19				
		VCCINT			U11	V20				
		VCCINT			U13	W12				
		VCCINT			U14	W13				
		VCCINT			U15	W14				
		VCCINT			U16	W16				
		VCCINT			U18	W17				
		VCCINT			V9	W18				
		VCCINT			V10	W19				
		VCCINT			V16	Y12				
		VCCINT			V18	Y13				
		VCCINT			W10	Y14				
		VCCINT			W11	Y15				
		VCCINT			W15	Y16				
		VCCINT			W16	Y17				
		VCCINT			W17	Y18				
		VCCIO2			C1	D1				
		VCCIO2			F5	F5				
		VCCIO2			L1	J3				

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F672	F896	DQS for x8/x9 in F672	DQS for x16/x18 in F672	DQS for x8/x9 in F896	DQS for x16/x18 in F896
		VCCIO2			M9	L11				
		VCCIO2				N5				
		VCCIO2			N5	R1				
		VCCIO2				R10				
		VCCIO1			AB5	AB3				
		VCCIO1			AD1	AE5				
		VCCIO1			P5	AG1				
		VCCIO1			R9	T1				
		VCCIO1			T1	T10				
		VCCIO1				V5				
		VCCIO1			V8	Y11				
		VCCIO8			AB6	AB11				
		VCCIO8			AB9	AB15				
		VCCIO8				AE10				
		VCCIO8			AB13	AF6				
		VCCIO8			AF3	AF13				
		VCCIO8				AH8				
		VCCIO8			AF11	AH11				
		VCCIO8			V12	AK4				
		VCCIO8			W9	AK15				
		VCCIO7			AB14	AB16				
		VCCIO7			AB17	AB20				
		VCCIO7			AB22	AE21				
		VCCIO7			AD20	AF19				
		VCCIO7			AF16	AF25				
		VCCIO7			AF24	AH21				
		VCCIO7			V15	AH23				
		VCCIO7				AK16				
		VCCIO7			W18	AK27				
		VCCIO6			AA22	AB28				
		VCCIO6			AD26	AE26				
		VCCIO6				AG30				
		VCCIO6			P22	T21				
		VCCIO6			R18	T30				
		VCCIO6			T26	V26				
		VCCIO6			V19	Y20				
		VCCIO5			C26	D30				
		VCCIO5				F26				
		VCCIO5			F22	J23				
		VCCIO5			J19	J28				

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F672	F896	DQS for x8/x9 in F672	DQS for x16/x18 in F672	DQS for x8/x9 in F896	DQS for x16/x18 in F896
		VCCIO5			L26	L20				
		VCCIO5			M18	N27				
		VCCIO5				R21				
		VCCIO5			N22	R30				
		VCCIO4			A16	A16				
		VCCIO4				A27				
		VCCIO4			A24	C20				
		VCCIO4			C20	C23				
		VCCIO4			D22	E18				
		VCCIO4			E14	E25				
		VCCIO4			E17	F21				
		VCCIO4			H18	J16				
		VCCIO4			J15	J20				
		VCCIO3			A3	A4				
		VCCIO3			A11	A15				
		VCCIO3			E6	C8				
		VCCIO3				C11				
		VCCIO3			E9	E6				
		VCCIO3			E13	F10				
		VCCIO3				F15				
		VCCIO3			H9	J11				
		VCCIO3			J12	J15				
		GND			H8	AA11				
		GND			H12	AA12				
		GND			J10	AA15				
		GND			J11	AA16				
		GND			J13	AA19				
		GND			J14	AA20				
		GND			J16	K11				
		GND			J17	K12				
		GND			K16	K15				
		GND			K17	K16				
		GND			L10	K19				
		GND			L12	K20				
		GND			L13	L12				
		GND			L14	M16				
		GND			L15	N13				
		GND			M12	N14				
		GND			M13	N15				
		GND			M14	N16				

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F672	F896	DQS for x8/x9 in F672	DQS for x16/x18 in F672	DQS for x8/x9 in F896	DQS for x16/x18 in F896
		GND			M15	N17				
		GND			N9	N18				
		GND			N11	P13				
		GND			N12	P14				
		GND			N13	P15				
		GND			N14	P16				
		GND			N15	P17				
		GND			N16	P18				
		GND			N18	R11				
		GND			P9	R13				
		GND			P11	R14				
		GND			P12	R15				
		GND			P13	R16				
		GND			P14	R17				
		GND			P15	R18				
		GND			P16	R20				
		GND			P18	T11				
		GND			R12	T13				
		GND			R13	T14				
		GND			R14	T15				
		GND			R15	T16				
		GND			R17	T17				
		GND			T10	T18				
		GND			T12	T20				
		GND			T13	U13				
		GND			T14	U14				
		GND			T15	U15				
		GND			T17	U16				
		GND			U10	U17				
		GND			U12	U18				
		GND			U17	V13				
		GND			V11	V14				
		GND			V13	V15				
		GND			V14	V16				
		GND			V17	V17				
		GND			W8	V18				
		GND			W12	W15				
		GND			W19	Y19				
		GND			A2	A2				
		GND			A12	A13				

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F672	F896	DQS for x8/x9 in F672	DQS for x16/x18 in F672	DQS for x8/x9 in F896	DQS for x16/x18 in F896
		GND			A15	A18				
		GND			A25	A29				
		GND				AB4				
		GND			AB7	AB10				
		GND				AB14				
		GND			AB11	AB17				
		GND			AB16	AB21				
		GND			AB19	AB27				
		GND			AC4	AE6				
		GND				AE9				
		GND			AD9	AE14				
		GND			AD14	AE18				
		GND			AD18	AE22				
		GND			AE1	AE25				
		GND				AF5				
		GND			AE26	AF26				
		GND			AF2	AG11				
		GND				AG21				
		GND			AF12	AH6				
		GND			AF15	AH25				
		GND			AF25	AJ1				
		GND			B1	AJ30				
		GND			B26	AK2				
		GND			C14	AK13				
		GND			C18	AK18				
		GND			D4	AK29				
		GND			D24	B1				
		GND			E7	B30				
		GND				C6				
		GND			E11	C25				
		GND			E16	D11				
		GND			E19	D20				
		GND			H5	E5				
		GND			H13	E26				
		GND				F6				
		GND			H14	F9				
		GND			H22	F14				
		GND			K20	F17				
		GND				F22				
		GND			L5	F25				

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F672	F896	DQS for x8/x9 in F672	DQS for x16/x18 in F672	DQS for x8/x9 in F896	DQS for x16/x18 in F896
		GND			L22	J4				
		GND			M1	J10				
		GND				J14				
		GND			M26	J17				
		GND			N8	J21				
		GND			N19	J27				
		GND				L23				
		GND			P8	M11				
		GND			P19	M20				
		GND			R1	N1				
		GND			R21	N6				
		GND			R26	N26				
		GND			T5	N30				
		GND			U8	P10				
		GND			U19	P21				
		GND			W5	U10				
		GND			W13	U21				
		GND				V1				
		GND			W14	V6				
		GND			W22	V25				
		GND				V30				
		GND			Y9	W11				
		GND			Y17	W20				

Notes:

(1) The optional functions (e.g. LVDS, DDR) are not available for some pins in certain packages.
For example, for the EP2C8 device, the LVDS70 pair is available for the Q208 and F256 packages, but not for the T144 package.

(2) The DQS0T, DQS1T, DQS0B, and DQS1B pin functions are only available in the F672 and F896 packages.

(3) If the dedicated CLK pins are not used to feed the global clock networks, they can be used as general-purpose input pins to feed the core logic.
The dedicated CLK pins do not support the I/O register.

Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description	Connection Guidelines
		Supply and Reference Pins	
VCCINT	Power	These are internal logic array voltage supply pins. VCCINT also supplies power to the input buffers used for the LVPECL, LVDS (regular I/O and CLK pins), differential HSTL, and differential SSTL I/O standards.	Connect all VCCINT pins to 1.2 V. Decoupling depends on the design decoupling requirements of the specific board. *(Note 2)*
VCCIO[1..8]	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O standards. VCCIO also supplies power to the input buffers used for the LVTTL, LVCMOS, 1.5-V, 1.8-V, 2.5-V, 3.3-V PCI, and 3.3-V PCI-X, differential SSTL, differential HSTL, and LVDS (regular I/O) I/O standards.	Verify that the VCCIO voltage level connected is consistent with the **.pin** report from the Quartus® II software. Decoupling depends on the design decoupling requirements of the specific board. *(Note 2)*
GND	Ground	Device ground pins.	Connect all GND pins to the board GND plane.
VREFB[1..8]N[0..3]	I/O	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-referenced pins for the bank.	If voltage-referenced I/O standards are not used in the bank, the VREF pins are available as user I/O pins. Decoupling depends on the design decoupling requirements of the specific board. *(Note 2)*
VCCA_PLL[1..4]*(Note 4)*	Power	Analog power for PLLs[1..4].	Connect these pins to 1.2 V, even if the PLL is not used. Use an isolated linear supply for better jitter performance. You can connect all VCCA_PLL pins to a single linear supply to minimize cost. Power on the PLLs should be decoupled. Decoupling depends on the design decoupling requirements of the specific board *(Note 2)* . For more information on this pin, refer to the *PLLs in Cyclone II Devices* chapter in the Cyclone II Device Handbook.
VCCD_PLL[1..4]*(Note 4)*	Power	Digital power for PLLs[1..4].	Connect these pins to the quietest digital supply on board (1.2 V), which is also supplied to the VCCINT, even if the PLL is not used. Power on the PLLs should be decoupled. Decoupling depends on the design decoupling requirements of the specific board *(Note 2)* . For more information on this pin, refer to the *PLLs in Cyclone II Devices* chapter in the Cyclone II Device Handbook.
GNDA_PLL[1..4]*(Note 4)*	Ground	Analog ground for PLLs[1..4].	Connect these pins directly to the same ground plane as the digital ground of the device, even if the PLL is not used. For more information on this pin, refer to the *PLLs in Cyclone II Devices* chapter in the Cyclone II Device Handbook.
GND_PLL[1..4]*(Note 4)*	Ground	Ground for PLLs[1..4].	Connect these pins to the GND plane on the board.
NC	No Connect	No Connect	Do not drive signals into these pins.
		Dedicated Configuration/JTAG Pins	
DCLK	Input (PS) Output (AS)	Dedicated configuration clock pin. In PS configuration, DCLK is used to clock configuration data from an external source into the Cyclone II device. In AS mode, DCLK is an output from the Cyclone II device that provides timing for the configuration interface. The input buffer on this pin supports hysteresis using the Schmitt trigger circuitry.	DCLK should not be left floating. You should drive it high or low, whichever is more convenient on the board.
DATA0	Input	Dedicated configuration data input pin. In serial configuration modes, bit-wide configuration data is received through this pin. In AS mode, DATA0 has an internal pull-up resistor that is always active. The input buffer on this pin supports hysteresis using the Schmitt trigger circuitry.	DATA0 should not be left floating. You should drive it high or low, whichever is more convenient on the board.
MSEL[0..1]	Input	Configuration input pins that set the Cyclone II device configuration scheme.	These pins must be hardwired to VCCIO of the bank they reside in or GND. Do not leave these pins floating. When these pins are unused, connect them to GND. For MSEL pin settings for different configuration schemes, refer to the Configuring Cyclone II Devices chapter in the Cyclone II Device Handbook.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled. The input buffer on this pin supports hysteresis using the Schmitt trigger circuitry.	In a multi-device configuration, nCE of the first device is tied low while its nCEO pin drives the nCE of the next device in the chain. In a single-device configuration, nCE is tied low.
nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user mode causes the FPGA to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic high level initiates reconfiguration. The input buffer on this pin supports hysteresis using the Schmitt trigger circuitry.	nCONFIG should be pulled high by an external 10-kΩ pull-up resistor to a 3.3-V supply. If the configuration scheme uses an enhanced configuration device or EPC2, nCONFIG can be tied directly to the nINIT_CONF pin of the configuration device. If this pin is not used, this pin can be connected through a resistor to VCCIO.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration status pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode. It is not available as a user I/O pin. The input buffer on this pin supports hysteresis using the Schmitt trigger circuitry.	CONF_DONE should be pulled high by an external 10-kΩ pull-up resistor to a 3.3-V supply. If internal pull-up resistors on the enhanced configuration device are used, external 10-kΩ pull-up resistors should not be used on this pin.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization. It is not available as a user I/O pin. The input buffer on this pin supports hysteresis using the Schmitt trigger circuitry.	nSTATUS should be pulled high by an external 10-kΩ pull-up resistor to a 3.3-V supply.
TCK	Input	Dedicated JTAG clock input pin. This pin has weak internal pull-down resistors. The input buffer on this pin supports hysteresis using the Schmitt trigger circuitry.	Connect this pin to GND via a 1-kΩ resistor. If the JTAG circuitry is not used, connect TCK to GND.

Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description	Connection Guidelines
TMS	Input	Dedicated JTAG input pin that provides the control signal to determine the transitions of the TAP controller state machine. This pin has weak internal pull-up resistors. The input buffer on this pin supports hysteresis using the Schmitt trigger circuitry.	Connect this pin to a 1-kΩ resistor via the VCCIO of the bank it resides in. If the JTAG circuitry is not used, connect TMS to VCCIO.
TDI	Input	Dedicated JTAG test data input pin for instructions, and test and programming data. This pin has weak internal pull-up resistors. The input buffer on this pin supports hysteresis using the Schmitt trigger circuitry.	Connect this pin to a 1-kΩ resistor via the VCCIO of the bank it resides in. If the JTAG circuitry is not used, connect TDI to VCCIO.
TDO	Output	Dedicated JTAG data output pin for instructions, and test and programming data.	When not in JTAG mode, this pin should be left unconnected.
Clock and PLL Pins			
CLK[0,2,4,6,8,10,12,14], LVDSCLK[0..7]p	Clock, Input	Dedicated global clock input pins that can also be used for the positive terminal inputs for differential global clock input or user input pins.	Connect unused pins to GND.
CLK[1,3,5,7,9,11,13,15], LVDSCLK[0..7]n	Clock, Input	Dedicated global clock input pins that can also be used for the negative terminal inputs for differential global clock input or user input pins.	Connect unused pins to GND.
PLL[1..4]_OUTp *(Note 4)*	I/O, Output	Optional positive terminal for external clock outputs from PLLs[1..4]. These pins can only use the differential I/O standard if it is being fed by a PLL output.	When not used as PLL output pins, these pins can be used as user I/O pins. When these pins are not used, they may be left floating.
PLL[1..4]_OUTn *(Note 4)*	I/O, Output	Optional negative terminal for external clock outputs from PLLs[1..4]. These pins can only use the differential I/O standard if it is being fed by a PLL output.	When not used as PLL output pins, these pins can be used as user I/O pins. When these pins are not used, they may be left floating.
Optional/Dual-Purpose Configuration Pins			
nCEO	I/O, Output	Output that drives low when device configuration is complete.	During a multi-device configuration, this pin feeds the nCE pin of a subsequent device and must be pulled high to VCCIO by an external 10-kΩ pull-up resistor. During a single-device configuration and for the last device in a multi-device configuration, this pin can be left unconnected or used as an user I/O after configuration.
nCSO	I/O, Output	Output control signal from the Cyclone II FPGA to the nCS pin of the serial configuration device in AS mode that enables the configuration device by driving it low. In AS mode, the nCSO has internal weak pull-up resistor, which is always active.	When not programming the device in AS mode, the nCSO pin can be used as user I/O. When this pin is not used as an I/O, Altera recommends that you leave the pin unconnected.
ASDO	I/O, Output	Output control signal from the Cyclone II FPGA to the serial configuration device in AS mode used to read out configuration data. In AS mode, the ASDO has internal weak pull-up resistor, which is always active.	When not programming the device in AS mode, the ASDO pin can be used as user I/O. When this pin is not used as an I/O, Altera recommends that you leave the pin unconnected.
CRC_ERROR	I/O, Output	Active-high signal that indicates the error-detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error-detection circuit is enabled.	When the dedicated output for CRC_ERROR is not used and this pin is not used as an I/O, Altera recommends that you leave the pin unconnected.
DEV_CLRn	I/O (when option off), Input (when option on)	Optional chip-wide reset pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed. The DEV_CLRn pin does not affect JTAG boundary-scan or programming operations. This pin is enabled by turning on the Enable device-wide reset (DEV_CLRn) option in the Quartus II software.	When the dedicated output for DEV_CLRn is not used and this pin is not used as an I/O, Altera recommends that you tie this pin to the VCCIO of the bank that it resides in or ground. *(Note 6)*
DEV_OE	I/O (when option off), Input (when option on)	Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design. This pin is enabled by turning on the Enable device-wide output enable (DEV_OE) option in the Quartus II software.	When the dedicated output for DEV_OE is not used and this pin is not used as an I/O, Altera recommends that you tie this pin to the VCCIO of the bank that it resides in or ground. *(Note 6)*
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose status pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration. This pin is enabled by turning on the Enable INIT_DONE output option in the Quartus II software.	When INIT_DONE is enabled, connect this pin to a 10-kΩ resistor via the VCCIO of the bank that it resides in.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin. This pin is enabled by turning on the Enable user-supplied start-up clock (CLKUSR) option in the Quartus II software.	If the CLKUSR pin is not used as a configuration clock input and the pin is not used as an I/O, Altera recommends that you connect this pin to ground.
Dual-Purpose Differential & External Memory Interface Pins			
LVDS[0-256][p,n] *(Note 3)*	I/O, TX/RX channel	Dual-purpose differential transmitter/receiver channels 0 to 256. These channels can be used for transmitting or receiving LVDS-compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	When these pins are not used, they can be tied to the VCCIO of the bank that they reside in or GND. *(Note 6)*
DPCLK[0..11]/ DQS[[0,1]L,[3,5,4,2]B,[1,0]R,[2,4,5,3]T] *(Note 5)*	I/O, DPCLK/DQS	Dual-purpose DPCLK/DQS pins can connect to the global clock network for high-fanout control signals such as clocks, asynchronous clears, presets, and clock enables. It can also be used as optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase-shift circuitry, which allows for the fine-tuning of the phase shift for input clocks or strobes to properly align clock edges needed to capture data.	When these pins are not used, they can be tied to the VCCIO of the bank that they reside in or GND. *(Note 6)*

Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description	Connection Guidelines
CDPCLK[0..7]/ DQS[[2,3]L,[1,0]B,[3,2]R,[0,1]T]*(Note 5)*	I/O, CDPCLK/DQS	Dual-purpose CDPCLK/DQS pins can connect to the global clock network for high-fanout control signals such as clocks, asynchronous clears, presets, and clock enables. Only one of the two CDPCLK in each corner can feed the clock control block at a time. The other pin can be used as a general-purpose I/O pin. The CDPCLK signals incur more delay to the clock block control because they are multiplexed before being driven into the clock block control. It can also be used as optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase-shift circuitry, which allows for the fine-tuning of the phase shift for input clocks or strobes to properly align clock edges needed to capture data.	When these pins are not used, they can be tied to the VCCIO of the bank that they reside in or GND. *(Note 6)*
DQ[[[1,3][L,R]],[[3,5][B,T]]][0..17]*(Note 5)*	I/O, DQ	Optional data signal for use in external memory interfacing in the x16 or x18 modes.	When these pins are not used, they can be tied to the VCCIO of the bank that they reside in or GND. *(Note 6)*
DQ[[[0..3][L,R]],[[0..5][B,T]]][0..8]*(Note 5)*	I/O, DQ	Optional data signal for use in external memory interfacing in the x8 or x9 modes.	When these pins are not used, they can be tied to the VCCIO of the bank that they reside in or GND. *(Note 6)*
DM[[[0..3][L,R]],[[0..5][B,T]]]*(Note 5)*	I/O, DM	Optional data mask pins for x8/x9 modes are required when writing to DDR SDRAM and DDR2 SDRAM devices. A low signal indicates that the write is valid. If the DM signal is high, the memory masks the DQ signals. Each group of DQ and DQS signals requires a DM pin.	When these pins are not used, they can be tied to the VCCIO of the bank that they reside in or GND. *(Note 6)*
DM[[[1,3][L,R]],[[3,5][B,T]]][0,1]*(Note 5)*	I/O, DM	Optional data mask pins for x16/x18 modes are required when writing to DDR SDRAM and DDR2 SDRAM devices. A low signal indicates that the write is valid. If the DM signal is high, the memory masks the DQ signals. Each group of DQ and DQS signals requires a DM pin.	When these pins are not used, they can be tied to the VCCIO of the bank that they reside in or GND. *(Note 6)*
DM[[[0..3][L,R]],[[0..5][B,T]]]*(Note 5)*	I/O, BWS	Byte Write Select is an active-low pin. When asserted active, BWS selects which byte is written into the device during write operation. Bytes not written remain unchanged. Deselecting BWS causes write data to be ignored and not written into device.	When these pins are not used, they can be tied to the VCCIO of the bank that they reside in or GND. *(Note 6)*
DM[[[1,3][L,R]],[[3,5][B,T]]][0,1]*(Note 5)*	I/O, BWS	Byte Write Select is an active-low pin. When asserted active, BWS selects which byte is written into the device during write operation. Bytes not written remain unchanged. Deselecting BWS causes write data to be ignored and not written into device.	When these pins are not used, they can be tied to the VCCIO of the bank that they reside in or GND. *(Note 6)*

Altera provides these guidelines only as recommendations. It is the responsibility of the designer to apply simulation results to the design to verify proper device functionality.

Notes:

1) These pin connection guidelines are created based on the largest Cyclone II device, EP2C70F896. Refer to the pin list for the availability of pins in each density.

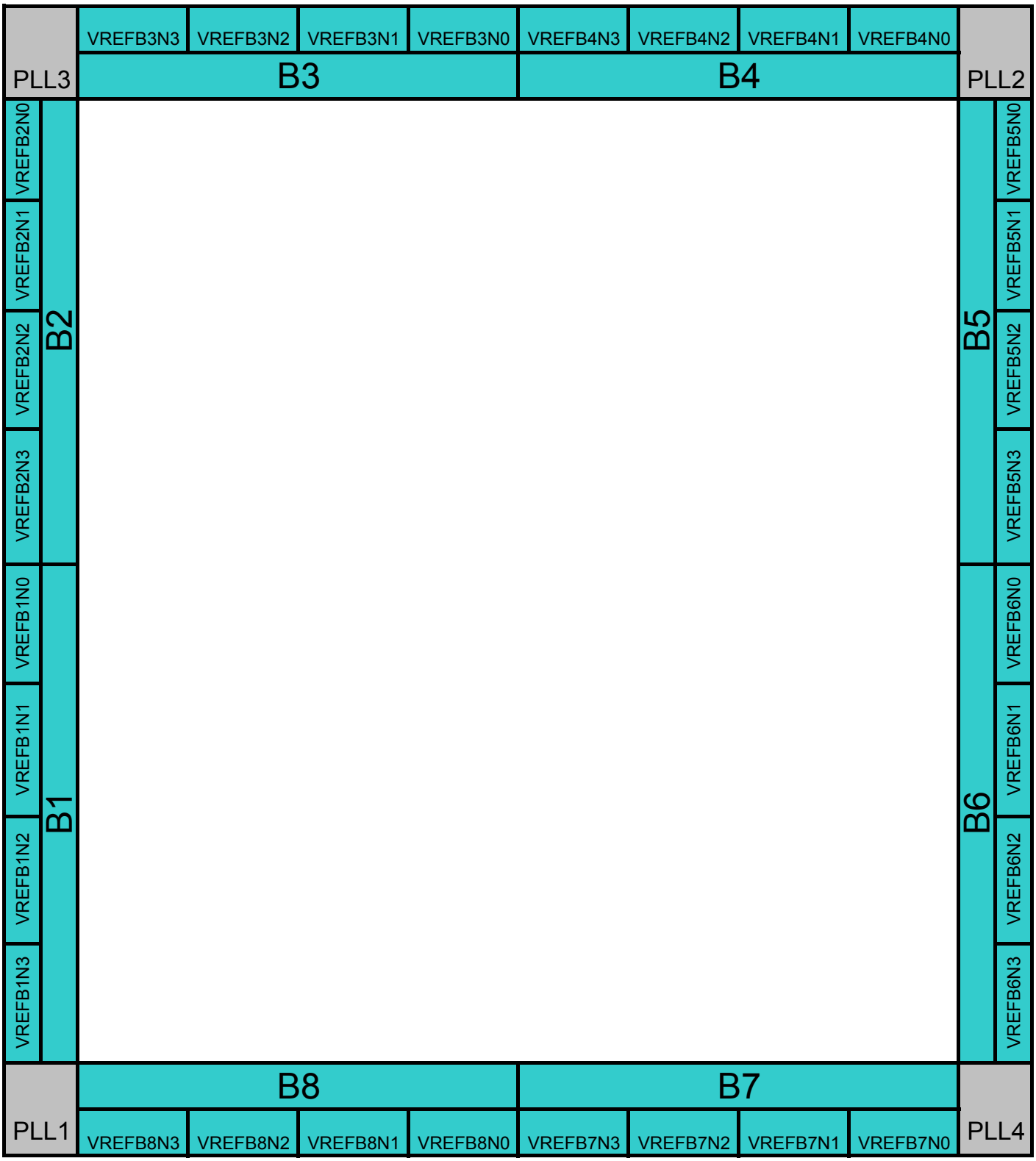
2) Capacitance values for the power supply should be selected after considering the amount of power they need to supply over the frequency of operation of the particular circuit being decoupled. A target impedance for the power plane should be calculated based on current draw and voltage droop requirements of the device or supply. The power plane should then be decoupled using the appropriate number of capacitors. On-board capacitors do not decouple higher than 100 MHz due to “Equivalent Series Inductance” of the mounting of the packages. Proper board design techniques such as interplaning capacitance with low inductance should be considered for higher frequency decoupling.

3) The differential transmitter/receiver channel count for each device and package is different; smaller packages may contain less than the maximum number of differential transmitter/receiver channels. For details on the differential transmitter/receiver channel count for each device, refer to the corresponding pin-out from www.altera.com.

4) The EP2C5, EP2C8, and EP2C8A devices have only PLL1 and PLL2.

5) The DQ, DQS, DM, and BWS# bus mode count for each device and package is different. Smaller packages may contain less than the maximum number of DQ, DQS, DM, and BWS# bus modes. For details on the DQ, DQS, DM, and BWS# bus mode count for each device, refer to the corresponding pin-out from www.altera.com.

6) Make sure that unused pins are set to input tristated in the Quartus II software. For instructions on how to set this, refer to the Quartus II Handbook.



Notes:

1. This is a top view of the silicon die.
2. This is only a pictorial representation to get an idea of placement on the device. Refer to the pin list and the Quartus® II software for exact locations.

Pin Information for the Cyclone® II EP2C70 Device
Version 1.7

Version Number	Date	Changes Made
1.0	10/5/2004	Initial version.
1.1	2/24/2005	Modified Pin Definitions for DATA0 pin.
1.2	3/18/2005	Added CRC_ERROR pin in Pin List and Pin Definition.
		Changed pin name from GNDD_PLL and GNDG_PLL to GND_PLL.
1.3	6/2/2005	Modified Pin Type column in Pin Definitions for VREFB[1..8]N[0..1] pins.
1.4	2/10/2006	Added footnote for pins that do not support Optional Functions (e.g. LVDS, DDR).
		Added footnote for DQS0T, DQS1T, DQS0B, and DQS1B pins.
		Modified Pin Definition for NC pins.
		Modified Pin Description of VREFB[1..8]N[0..3] pins.
		Modified Pin Description of VCCA_PLL[1..4] and VCCD_PLL[1..4] pins.
		Added Pin Description for BWS pins.
1.5	3/1/2006	Added comment for PLL_OUT pins in Pin Definitions.
1.6	6/16/2006	Added "I/O" to pin type of nCEO, nCSO, and ASDO pins.
		Modified Pin Description of VCCIO and VCCINT.
		Modified Pin Description for NCONFIG, NCE, DATA0, TMS, TCK, TDI, NSTATUS, CONDONE, and DCLK pins.
		Moved nCEO Discription from section "Dedicated Configuration/JTAG Pins" to section "Optional/Dual-Purpose Configuration Pins".
1.7	4/18/2008	Incorporated pin connection guidelines into pin definitions worksheet.