Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	F484	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 1)	DQS for X16/X18 for F780(Note 1)	DQS for X4 for F484	DQS for X8/X9 for F484(Note 1)
		NC					E25	E16					
		TDI		TDI			F24	E17					
		TMS		TMS			H22	D17					
		TRST		TRST			D26	F18					
		TCK		TCK			C26	D18					
		TDO		TDO			G24	A18					
1A	VREF1A	IO			DIFFIO_TX_L1n	DIFFOUT_L1n	F26	B19					
1A	VREF1A	IO			DIFFIO_TX_L1p	DIFFOUT_L1p	F25	C19					
1A	VREF1A	IO	RDN1A		DIFFIO_RX_L1n	DIFFOUT_L2n	C28	A20					
1A	VREF1A	IO	RUP1A		DIFFIO_RX_L1p	DIFFOUT_L2p	D27	A19					
1A	VREF1A	IO			DIFFIO_TX_L2n	DIFFOUT_L3n	G26	G17	DQ1L	DQ1L	DQ1L	DQ1L	DQ1L
1A	VREF1A	IO			DIFFIO_TX_L2p	DIFFOUT_L3p	G25	G16	DQ1L	DQ1L	DQ1L	DQ1L	DQ1L
1A	VREF1A	IO			DIFFIO_RX_L2n	DIFFOUT_L4n	B28	B20	DQSn1L	DQ1L	DQ1L	DQSn1L	DQ1L
1A	VREF1A	IO			DIFFIO_RX_L2p	DIFFOUT_L4p	C27	C20	DQS1L	DQ1L/CQn1L	DQ1L	DQS1L	DQ1L/CQn1L
1A	VREF1A	IO			DIFFIO_TX_L3n	DIFFOUT_L5n	H25	D19	DQ1L	DQ1L	DQ1L	DQ1L	DQ1L
1A	VREF1A	IO			DIFFIO_TX_L3p	DIFFOUT_L5p	J24	E19	DQ1L	DQ1L	DQ1L	DQ1L	DQ1L
1A	VREF1A	IO			DIFFIO_RX_L3n	DIFFOUT_L6n	D28	A22	DQSn2L	DQSn1L/DQ1L	DQ1L	DQSn2L	DQSn1L/DQ1L
1A	VREF1A	IO			DIFFIO_RX_L3p	DIFFOUT_L6p	E28	A21	DQS2L	DQS1L/CQ1L	DQ1L/CQn1L	DQS2L	DQS1L/CQ1L
1A	VREF1A	IO			DIFFIO_TX_L4n	DIFFOUT_L7n	J23	D20	DQ2L	DQ1L	DQ1L	DQ2L	DQ1L
1A	VREF1A	IO			DIFFIO_TX_L4p	DIFFOUT_L7p	J22	E20	DQ2L	DQ1L	DQ1L	DQ2L	DQ1L
1A	VREF1A	IO			DIFFIO_RX_L4n	DIFFOUT_L8n	F28	B22	DQ2L	DQ1L	DQ1L	DQ2L	DQ1L
1A	VREF1A	IO			DIFFIO_RX_L4p	DIFFOUT_L8p	F27	C22	DQ2L	DQ1L	DQ1L	DQ2L	DQ1L
1A	VREF1A	IO			DIFFIO_TX_L5n	DIFFOUT_L9n	K21	F16	DQ3L	DQ2L	DQ1L	DQ3L	
1A	VREF1A	IO			DIFFIO_TX_L5p	DIFFOUT_L9p	K20	F15	DQ3L	DQ2L	DQ1L	DQ3L	
1A	VREF1A	IO			DIFFIO_RX_L5n	DIFFOUT_L10n	G28	C21	DQSn3L	DQ2L	DQSn1L/DQ1L	DQSn3L	
1A	VREF1A	IO			DIFFIO_RX_L5p	DIFFOUT_L10p	G27	D21	DQS3L	DQ2L/CQn2L	DQS1L/CQ1L	DQS3L	
1A	VREF1A	IO			DIFFIO_TX_L6n	DIFFOUT_L11n	K26	H16	DQ3L	DQ2L	DQ1L	DQ3L	
1A	VREF1A	IO			DIFFIO_TX_L6p	DIFFOUT_L11p	K25	G15	DQ3L	DQ2L	DQ1L	DQ3L	
1A	VREF1A	IO			DIFFIO_RX_L6n	DIFFOUT_L12n	J26	D22	DQSn4L	DQSn2L/DQ2L	DQ1L		
1A	VREF1A	IO			DIFFIO_RX_L6p	DIFFOUT_L12p	J25	E22	DQS4L	DQS2L/CQ2L	DQ1L		
1A	VREF1A	IO			DIFFIO_TX_L7n	DIFFOUT_L13n	K24		DQ4L	DQ2L	DQ1L		
1A	VREF1A	IO			DIFFIO_TX_L7p	DIFFOUT_L13p	K23		DQ4L	DQ2L	DQ1L		
1A	VREF1A	IO			DIFFIO_RX_L7n	DIFFOUT_L14n	H28		DQ4L	DQ2L	DQ1L		
1A	VREF1A	IO			DIFFIO_RX_L7p	DIFFOUT_L14p	J27		DQ4L	DQ2L	DQ1L		
1A	VREF1A	IO			DIFFIO_TX_L8n	DIFFOUT_L15n	L23						
1A	VREF1A	IO			DIFFIO_TX_L8p	DIFFOUT_L15p	L22						
1A	VREF1A	IO			DIFFIO_RX_L8n	DIFFOUT_L16n	J28						
1A	VREF1A	IO			DIFFIO_RX_L8p	DIFFOUT_L16p	K27						
1C	VREF1C	IO			DIFFIO_TX_L9n	DIFFOUT_L17n	M23	G19					
1C	VREF1C	IO			DIFFIO_TX_L9p	DIFFOUT_L17p	M22	H19					
1C	VREF1C	IO			DIFFIO_RX_L9n	DIFFOUT_L18n	L26	F20	DQSn5L			DQSn5L	
1C	VREF1C	IO			DIFFIO_RX_L9p	DIFFOUT_L18p	L25	G20	DQS5L			DQS5L	
1C	VREF1C	IO		CLKUSR	DIFFIO_TX_L10n	DIFFOUT_L19n	M21	H20	DQ5L			DQ5L	
1C	VREF1C	IO			DIFFIO_TX_L10p	DIFFOUT_L19p	M20	J19	DQ5L			DQ5L	
1C	VREF1C	IO			DIFFIO_RX_L10n	DIFFOUT_L20n	K28	F22	DQ5L			DQ5L	
1C	VREF1C	IO			DIFFIO_RX_L10p	DIFFOUT_L20p	L28	F21	DQ5L			DQ5L	
1C	VREF1C	IO		DATA0	DIFFIO_TX_L11n	DIFFOUT_L21n	N21	J18	DQ6L	DQ5L		DQ6L	DQ5L
1C	VREF1C	IO		DATA1	DIFFIO_TX_L11p	DIFFOUT_L21p	N20	J17	DQ6L	DQ5L		DQ6L	DQ5L
1C	VREF1C	IO		DATA2	DIFFIO_RX_L11n	DIFFOUT_L22n	M26	K20	DQSn6L	DQ5L		DQSn6L	DQ5L
1C	VREF1C	IO		DATA3	DIFFIO_RX_L11p	DIFFOUT_L22p	M25	K19	DQS6L	DQ5L/CQn5L		DQS6L	DQ5L/CQn5L
1C	VREF1C	IO		DATA4	DIFFIO_TX_L12n	DIFFOUT_L23n	N25	H17	DQ6L	DQ5L		DQ6L	DQ5L
1C	VREF1C	IO		DATA5	DIFFIO_TX_L12p	DIFFOUT_L23p	M24	J16	DQ6L	DQ5L		DQ6L	DQ5L
1C	VREF1C	IO		DATA6	DIFFIO_RX_L12n	DIFFOUT_L24n	M28	J21	DQSn7L	DQSn5L/DQ5L		DQSn7L	DQSn5L/DQ5L
1C	VREF1C	IO		DATA7	DIFFIO_RX_L12p	DIFFOUT_L24p	M27	J20	DQS7L	DQS5L/CQ5L		DQS7L	DQS5L/CQ5L
1C	VREF1C	IO		INIT_DONE	DIFFIO_TX_L13n	DIFFOUT_L25n	N23	K16	DQ7L	DQ5L		DQ7L	DQ5L
1C	VREF1C	IO		CRC_ERROR	DIFFIO_TX_L13p	DIFFOUT_L25p	P23	L16	DQ7L	DQ5L		DQ7L	DQ5L
1C	VREF1C	IO		DEV_OE	DIFFIO_RX_L13n	DIFFOUT_L26n	P25	G22	DQ7L	DQ5L		DQ7L	DQ5L
1C	VREF1C	IO		DEV_CLRn	DIFFIO_RX_L13p	DIFFOUT_L26p	N24	G21	DQ7L	DQ5L		DQ7L	DQ5L
1C	VREF1C	IO	PLL_L2_CLKOUT0n		DIFFIO_TX_L14n	DIFFOUT_L27n	P20	L20					
1C	VREF1C	IO	PLL_L2_FB_CLKOUT0p		DIFFIO_TX_L14p	DIFFOUT_L27p	P19	L19					
1C	VREF1C	IO	CLK0n		DIFFIO_RX_L14n	DIFFOUT_L28n	N27	J22					
1C	VREF1C	IO	CLK0p		DIFFIO_RX_L14p	DIFFOUT_L28p	N26	K21					

1C	VREF1C	CLK1n	CLK1n				N28	K22					
1C	VREF1C	CLK1p	CLK1p				P28	L22					
		VCCA_PLL_L2					R22	M18					
		VCCD_PLL_L2					P22	M17					
2C	VREF2C	CLK3p	CLK3p				R27	M19					
2C	VREF2C	CLK3n	CLK3n				R28	M20					
2C	VREF2C	IO	CLK2p		DIFFIO_RX_L15p	DIFFOUT_L29p	U28	M21					
2C	VREF2C	IO	CLK2n		DIFFIO_RX_L15n	DIFFOUT_L29n	T28	M22					
2C	VREF2C	IO			DIFFIO_TX_L15p	DIFFOUT_L30p	R20	M15					
2C	VREF2C	IO			DIFFIO_TX_L15n	DIFFOUT_L30n	R21	M16					
2C	VREF2C	IO			DIFFIO_RX_L16p	DIFFOUT_L31p	R26	N21	DQ8L	DQ10L		DQ8L	DQ10L
2C	VREF2C	IO			DIFFIO_RX_L16n	DIFFOUT_L31n	T27	N22	DQ8L	DQ10L		DQ8L	DQ10L
2C	VREF2C	IO			DIFFIO_TX_L16p	DIFFOUT_L32p	T25	P16	DQ8L	DQ10L		DQ8L	DQ10L
2C	VREF2C	IO			DIFFIO_TX_L16n	DIFFOUT_L32n	R25	P17	DQ8L	DQ10L		DQ8L	DQ10L
2C	VREF2C	IO			DIFFIO_RX_L17p	DIFFOUT_L33p	V27	N19	DQS8L	DQS10L/CQ10L		DQS8L	DQS10L/CQ10L
2C	VREF2C	IO			DIFFIO_RX_L17n	DIFFOUT_L33n	V28	N20	DQSn8L	DQSn10L/DQ10L		DQSn8L	DQSn10L/DQ10L
2C	VREF2C	IO			DIFFIO_TX_L17p	DIFFOUT_L34p	T20	N16	DQ9L	DQ10L		DQ9L	DQ10L
2C	VREF2C	IO			DIFFIO_TX_L17n	DIFFOUT_L34n	T21	N17	DQ9L	DQ10L		DQ9L	DQ10L
2C	VREF2C	IO			DIFFIO_RX_L18p	DIFFOUT_L35p	V26	R21	DQS9L	DQ10L/CQn10L		DQS9L	DQ10L/CQn10L
2C	VREF2C	IO			DIFFIO_RX_L18n	DIFFOUT_L35n	U26	R22	DQSn9L	DQ10L		DQSn9L	DQ10L
2C	VREF2C	IO			DIFFIO_TX_L18p	DIFFOUT_L36p	T24	P19	DQ9L	DQ10L		DQ9L	DQ10L
2C	VREF2C	IO			DIFFIO_TX_L18n	DIFFOUT_L36n	U25	P20	DQ9L	DQ10L		DQ9L	DQ10L
2C	VREF2C	IO			DIFFIO_RX_L19p	DIFFOUT_L37p	W27	U22	DQ10L			DQ10L	
2C	VREF2C	IO			DIFFIO_RX_L19n	DIFFOUT_L37n	W28	T22	DQ10L			DQ10L	
2C	VREF2C	IO			DIFFIO_TX_L19p	DIFFOUT_L38p	T22	R19	DQ10L			DQ10L	
2C	VREF2C	IO			DIFFIO_TX_L19n	DIFFOUT_L38n	T23	R20	DQ10L			DQ10L	
2C	VREF2C	IO			DIFFIO_RX_L20p	DIFFOUT_L39p	V24	T20	DQS10L			DQS10L	
2C	VREF2C	IO			DIFFIO_RX_L20n	DIFFOUT_L39n	V25	T21	DQSn10L			DQSn10L	
2C	VREF2C	IO			DIFFIO_TX_L20p	DIFFOUT_L40p	V23	R18					
2C	VREF2C	IO			DIFFIO_TX_L20n	DIFFOUT_L40n	U23	T19					
2A	VREF2A	IO			DIFFIO_RX_L21p	DIFFOUT_L41p	AA27						
2A	VREF2A	IO			DIFFIO_RX_L21n	DIFFOUT_L41n	Y28						
2A	VREF2A	IO			DIFFIO_TX_L21p	DIFFOUT_L42p	W22						
2A	VREF2A	IO			DIFFIO_TX_L21n	DIFFOUT_L42n	W23						
2A	VREF2A	IO			DIFFIO_RX_L22p	DIFFOUT_L43p	AB27		DQ11L	DQ13L	DQ14L		
2A	VREF2A	IO			DIFFIO_RX_L22n	DIFFOUT_L43n	AA28		DQ11L	DQ13L	DQ14L		
2A	VREF2A	IO			DIFFIO_TX_L22p	DIFFOUT_L44p	W24		DQ11L	DQ13L	DQ14L		
2A	VREF2A	IO			DIFFIO_TX_L22n	DIFFOUT_L44n	W25		DQ11L	DQ13L	DQ14L		
2A	VREF2A	IO			DIFFIO_RX_L23p	DIFFOUT_L45p	Y25	V21	DQS11L	DQS13L/CQ13L	DQ14L		
2A	VREF2A	IO			DIFFIO_RX_L23n	DIFFOUT_L45n	Y26	V22	DQSn11L	DQSn13L/DQ13L	DQ14L		
2A	VREF2A	IO			DIFFIO_TX_L23p	DIFFOUT_L46p	V20	U15	DQ12L	DQ13L	DQ14L	DQ12L	
2A	VREF2A	IO			DIFFIO_TX_L23n	DIFFOUT_L46n	V21	T15	DQ12L	DQ13L	DQ14L	DQ12L	
2A	VREF2A	IO			DIFFIO_RX_L24p	DIFFOUT_L47p	AC28	Y22	DQS12L	DQ13L/CQn13L	DQS14L/CQ14L	DQS12L	
2A	VREF2A	IO			DIFFIO_RX_L24n	DIFFOUT_L47n	AB28	W22	DQSn12L	DQ13L	DQSn14L/DQ14L	DQSn12L	
2A	VREF2A	IO			DIFFIO_TX_L24p	DIFFOUT_L48p	AA25	U16	DQ12L	DQ13L	DQ14L	DQ12L	
2A	VREF2A	IO			DIFFIO_TX_L24n	DIFFOUT_L48n	AA26	T17	DQ12L	DQ13L	DQ14L	DQ12L	
2A	VREF2A	IO			DIFFIO_RX_L25p	DIFFOUT_L49p	AB25	W20	DQ13L	DQ14L	DQ14L	DQ13L	DQ14L
2A	VREF2A	IO			DIFFIO_RX_L25n	DIFFOUT_L49n	AB26	W21	DQ13L	DQ14L	DQ14L	DQ13L	DQ14L
2A	VREF2A	IO			DIFFIO_TX_L25p	DIFFOUT_L50p	AC25	U19	DQ13L	DQ14L	DQ14L	DQ13L	DQ14L
2A	VREF2A	IO			DIFFIO_TX_L25n	DIFFOUT_L50n	AC26	U20	DQ13L	DQ14L	DQ14L	DQ13L	DQ14L
2A	VREF2A	IO			DIFFIO_RX_L26p	DIFFOUT_L51p	AD27	AA21	DQS13L	DQS14L/CQ14L	DQ14L/CQn14L	DQS13L	DQS14L/CQ14L
2A	VREF2A	IO			DIFFIO_RX_L26n	DIFFOUT_L51n	AD28	AA22	DQSn13L	DQSn14L/DQ14L	DQ14L	DQSn13L	DQSn14L/DQ14L
2A	VREF2A	IO			DIFFIO_TX_L26p	DIFFOUT_L52p	W20	V19	DQ14L	DQ14L	DQ14L	DQ14L	DQ14L
2A	VREF2A	IO			DIFFIO_TX_L26n	DIFFOUT_L52n	W21	V20	DQ14L	DQ14L	DQ14L	DQ14L	DQ14L
2A	VREF2A	IO			DIFFIO_RX_L27p	DIFFOUT_L53p	AG28	AB20	DQS14L	DQ14L/CQn14L	DQ14L	DQS14L	DQ14L/CQn14L
2A	VREF2A	IO			DIFFIO_RX_L27n	DIFFOUT_L53n	AF28	AB21	DQSn14L	DQ14L	DQ14L	DQSn14L	DQ14L
2A	VREF2A	IO			DIFFIO_TX_L27p	DIFFOUT_L54p	Y23	V16	DQ14L	DQ14L	DQ14L	DQ14L	DQ14L
2A	VREF2A	IO			DIFFIO_TX_L27n	DIFFOUT_L54n	AA24	W17	DQ14L	DQ14L	DQ14L	DQ14L	DQ14L
2A	VREF2A	IO	RUP2A		DIFFIO_RX_L28p	DIFFOUT_L55p	AE27	AB18					
2A	VREF2A	IO	RDN2A		DIFFIO_RX_L28n	DIFFOUT_L55n	AE28	AB19					
2A	VREF2A	IO			DIFFIO_TX_L28p	DIFFOUT_L56p	AA23	AA19					
2A	VREF2A	IO			DIFFIO_TX_L28n	DIFFOUT_L56n	AB24	Y19					
		nCONFIG		nCONFIG			W19	AB17					
		nSTATUS		nSTATUS			AD25	W18					

		CONF_DONE		CONF_DONE			AE26	V18					
		PORSEL		PORSEL			AB23	Y18					
		nCE		nCE			Y20	Y17					
		NC					AB22	AA18					
3A	VREF3A	IO				DIFFOUT_B1n	AF26		DQ1B	DQ1B	DQ1B		
3A	VREF3A	IO				DIFFOUT_B1p	AH27		DQ1B	DQ1B	DQ1B		
3A	VREF3A	IO	RDN3A		DIFFIO_RX_B1n	DIFFOUT_B2n	AH25		DQSn1B	DQ1B	DQ1B		
3A	VREF3A	IO	RUP3A		DIFFIO_RX_B1p	DIFFOUT_B2p	AG25		DQS1B	DQ1B/CQn1B	DQ1B		
3A	VREF3A	IO				DIFFOUT_B3n	AG27		DQ1B	DQ1B	DQ1B		
3A	VREF3A	IO				DIFFOUT_B3p	AH26		DQ1B	DQ1B	DQ1B		
3A	VREF3A	IO			DIFFIO_RX_B2n	DIFFOUT_B4n	AE22		DQSn2B	DQSn1B/DQ1B	DQ1B		
3A	VREF3A	IO			DIFFIO_RX_B2p	DIFFOUT_B4p	AD22		DQS2B	DQS1B/CQ1B	DQ1B/CQn1B		
3A	VREF3A	IO				DIFFOUT_B5n	AB20		DQ2B	DQ1B	DQ1B		
3A	VREF3A	IO				DIFFOUT_B5p	AB21		DQ2B	DQ1B	DQ1B		
3A	VREF3A	IO			DIFFIO_RX_B3n	DIFFOUT_B6n	AD21		DQ2B	DQ1B	DQ1B		
3A	VREF3A	IO			DIFFIO_RX_B3p	DIFFOUT_B6p	AC21		DQ2B	DQ1B	DQ1B		
3A	VREF3A	IO				DIFFOUT_B7n	AD24		DQ3B	DQ2B	DQ1B		
3A	VREF3A	IO				DIFFOUT_B7p	AE23		DQ3B	DQ2B	DQ1B		
3A	VREF3A	IO			DIFFIO_RX_B4n	DIFFOUT_B8n	AF24		DQSn3B	DQ2B	DQSn1B/DQ1B		
3A	VREF3A	IO			DIFFIO_RX_B4p	DIFFOUT_B8p	AE24		DQS3B	DQ2B/CQn2B	DQS1B/CQ1B		
3A	VREF3A	IO				DIFFOUT_B9n	AF23		DQ3B	DQ2B	DQ1B		
3A	VREF3A	IO				DIFFOUT_B9p	AG24		DQ3B	DQ2B	DQ1B		
3A	VREF3A	IO			DIFFIO_RX_B5n	DIFFOUT_B10n	AH24		DQSn4B	DQSn2B/DQ2B	DQ1B		
3A	VREF3A	IO			DIFFIO_RX_B5p	DIFFOUT_B10p	AH23		DQS4B	DQS2B/CQ2B	DQ1B		
3A	VREF3A	IO				DIFFOUT_B11n	AH20		DQ4B	DQ2B	DQ1B		
3A	VREF3A	IO				DIFFOUT_B11p	AH21		DQ4B	DQ2B	DQ1B		
3A	VREF3A	IO			DIFFIO_RX_B6n	DIFFOUT_B12n	AH22		DQ4B	DQ2B	DQ1B		
3A	VREF3A	IO			DIFFIO_RX_B6p	DIFFOUT_B12p	AG22		DQ4B	DQ2B	DQ1B		
3A	VREF3A	IO				DIFFOUT_B13n	AC20		DQ5B	DQ3B			
3A	VREF3A	IO				DIFFOUT_B13p	AG21		DQ5B	DQ3B			
3A	VREF3A	IO			DIFFIO_RX_B7n	DIFFOUT_B14n	AF21		DQSn5B	DQ3B			
3A	VREF3A	IO			DIFFIO_RX_B7p	DIFFOUT_B14p	AE21		DQS5B	DQ3B/CQn3B			
3A	VREF3A	IO				DIFFOUT_B15n	AF20		DQ5B	DQ3B			
3A	VREF3A	IO				DIFFOUT_B15p	AE20		DQ5B	DQ3B			
3A	VREF3A	IO			DIFFIO_RX_B8n	DIFFOUT_B16n	AD19		DQSn6B	DQSn3B/DQ3B			
3A	VREF3A	IO			DIFFIO_RX_B8p	DIFFOUT_B16p	AC19		DQS6B	DQS3B/CQ3B			
3A	VREF3A	IO				DIFFOUT_B17n	AB19		DQ6B	DQ3B			
3A	VREF3A	IO				DIFFOUT_B17p	AA19		DQ6B	DQ3B			
3A	VREF3A	IO			DIFFIO_RX_B9n	DIFFOUT_B18n	AE19		DQ6B	DQ3B			
3A	VREF3A	IO			DIFFIO_RX_B9p	DIFFOUT_B18p	AD18		DQ6B	DQ3B			
3A	VREF3A	IO				DIFFOUT_B19n	Y19						
3A	VREF3A	IO				DIFFOUT_B19p	AA18						
3A	VREF3A	IO			DIFFIO_RX_B10n	DIFFOUT_B20n	Y18						
3A	VREF3A	IO			DIFFIO_RX_B10p	DIFFOUT_B20p	Y17						
3C	VREF3C	IO				DIFFOUT_B21n	AF19	W16	DQ7B	DQ7B		DQ7B	DQ7B
3C	VREF3C	IO				DIFFOUT_B21p	AG19	V15	DQ7B	DQ7B		DQ7B	DQ7B
3C	VREF3C	IO			DIFFIO_RX_B11n	DIFFOUT_B22n	AH19	Y14	DQSn7B	DQ7B		DQSn7B	DQ7B
3C	VREF3C	IO			DIFFIO_RX_B11p	DIFFOUT_B22p	AG18	W14	DQS7B	DQ7B/CQn7B		DQS7B	DQ7B/CQn7B
3C	VREF3C	IO				DIFFOUT_B23n	AH17	Y15	DQ7B	DQ7B		DQ7B	DQ7B
3C	VREF3C	IO				DIFFOUT_B23p	AH18	W15	DQ7B	DQ7B		DQ7B	DQ7B
3C	VREF3C	IO			DIFFIO_RX_B12n	DIFFOUT_B24n	AF17	AB16	DQSn8B	DQSn7B/DQ7B		DQSn8B	DQSn7B/DQ7B
3C	VREF3C	IO			DIFFIO_RX_B12p	DIFFOUT_B24p	AE18	AA16	DQS8B	DQS7B/CQ7B		DQS8B	DQS7B/CQ7B
3C	VREF3C	IO				DIFFOUT_B25n	AE16	Y16	DQ8B	DQ7B		DQ8B	DQ7B
3C	VREF3C	IO				DIFFOUT_B25p	AD16	AB14	DQ8B	DQ7B		DQ8B	DQ7B
3C	VREF3C	IO			DIFFIO_RX_B13n	DIFFOUT_B26n	AF16	AB15	DQ8B	DQ7B		DQ8B	DQ7B
3C	VREF3C	IO			DIFFIO_RX_B13p	DIFFOUT_B26p	AE17	AA15	DQ8B	DQ7B		DQ8B	DQ7B
3C	VREF3C	IO	PLL_B1_CLKOUT4			DIFFOUT_B27n	AC17	T13					
3C	VREF3C	IO	PLL_B1_CLKOUT3			DIFFOUT_B27p	AB17	R13					
3C	VREF3C	IO			DIFFIO_RX_B14n	DIFFOUT_B28n	AC16	W13					
3C	VREF3C	IO			DIFFIO_RX_B14p	DIFFOUT_B28p	AB16	V13					
3C	VREF3C	IO	PLL_B1_CLKOUT0n			DIFFOUT_B29n	AA15	Y12					
3C	VREF3C	IO	PLL_B1_CLKOUT0p			DIFFOUT_B29p	Y15	W12					
3C	VREF3C	IO	PLL_B1_FBn/CLKOUT2		DIFFIO_RX_B15n	DIFFOUT_B30n	AH16	U14					
3C	VREF3C	IO	PLL_B1_FBp/CLKOUT1		DIFFIO_RX_B15p	DIFFOUT_B30p	AG16	U13					

3C	VREF3C	IO	CLK5n			DIFFOUT_B31n	AH15	AB12					
3C	VREF3C	IO	CLK5p			DIFFOUT_B31p	AG15	AA12					
3C	VREF3C	IO	CLK4n		DIFFIO_RX_B16n	DIFFOUT_B32n	AF15	AB13					
3C	VREF3C	IO	CLK4p		DIFFIO_RX_B16p	DIFFOUT_B32p	AE15	AA13					
		VCC_CLKIN3C					AB14	T12					
		VCCA_PLL_B1					AC14	U11					
		VCCD_PLL_B1					AB15	U12					
		VCC_CLKIN4C					AC13	U10					
4C	VREF4C	IO	CLK6p		DIFFIO_RX_B17p	DIFFOUT_B33p	AE14	Y10					
4C	VREF4C	IO	CLK6n		DIFFIO_RX_B17n	DIFFOUT_B33n	AF14	AA10					
4C	VREF4C	IO	CLK7p			DIFFOUT_B34p	AG13	AB10					
4C	VREF4C	IO	CLK7n			DIFFOUT_B34n	AH14	AB11					
4C	VREF4C	IO			DIFFIO_RX_B18p	DIFFOUT_B35p	AG12	W11					
4C	VREF4C	IO			DIFFIO_RX_B18n	DIFFOUT_B35n	AH13	Y11					
4C	VREF4C	IO				DIFFOUT_B36p	Y13	T10	DQ9B			DQ9B	
4C	VREF4C	IO				DIFFOUT_B36n	Y14	R10	DQ9B			DQ9B	
4C	VREF4C	IO			DIFFIO_RX_B19p	DIFFOUT_B37p	AD13	U9	DQS9B			DQS9B	
4C	VREF4C	IO			DIFFIO_RX_B19n	DIFFOUT_B37n	AE13	V9	DQSn9B			DQSn9B	
4C	VREF4C	IO				DIFFOUT_B38p	AA13	R9	DQ9B			DQ9B	
4C	VREF4C	IO				DIFFOUT_B38n	AB13	T9	DQ9B			DQ9B	
4C	VREF4C	IO			DIFFIO_RX_B20p	DIFFOUT_B39p	AG10	AA9	DQ10B	DQ11B		DQ10B	DQ11B
4C	VREF4C	IO			DIFFIO_RX_B20n	DIFFOUT_B39n	AH10	AB9	DQ10B	DQ11B		DQ10B	DQ11B
4C	VREF4C	IO				DIFFOUT_B40p	AH11	W8	DQ10B	DQ11B		DQ10B	DQ11B
4C	VREF4C	IO				DIFFOUT_B40n	AH12	AB8	DQ10B	DQ11B		DQ10B	DQ11B
4C	VREF4C	IO			DIFFIO_RX_B21p	DIFFOUT_B41p	AF10	W9	DQS10B	DQS11B/CQ11B		DQS10B	DQS11B/CQ11B
4C	VREF4C	IO			DIFFIO_RX_B21n	DIFFOUT_B41n	AF11	Y9	DQSn10B	DQSn11B/DQ11B		DQSn10B	DQSn11B/DQ11B
4C	VREF4C	IO				DIFFOUT_B42p	AF12	Y7	DQ11B	DQ11B		DQ11B	DQ11B
4C	VREF4C	IO				DIFFOUT_B42n	AC12	W7	DQ11B	DQ11B		DQ11B	DQ11B
4C	VREF4C	IO			DIFFIO_RX_B22p	DIFFOUT_B43p	AD12	AA7	DQS11B	DQ11B/CQn11B		DQS11B	DQ11B/CQn11B
4C	VREF4C	IO			DIFFIO_RX_B22n	DIFFOUT_B43n	AE12	AB7	DQSn11B	DQ11B		DQSn11B	DQ11B
4C	VREF4C	IO				DIFFOUT_B44p	AC11	AB6	DQ11B	DQ11B		DQ11B	DQ11B
4C	VREF4C	IO				DIFFOUT_B44n	AE11	AA6	DQ11B	DQ11B		DQ11B	DQ11B
4A	VREF4A	IO			DIFFIO_RX_B23p	DIFFOUT_B45p	AB11						
4A	VREF4A	IO			DIFFIO_RX_B23n	DIFFOUT_B45n	AC10						
4A	VREF4A	IO				DIFFOUT_B46p	Y10						
4A	VREF4A	IO				DIFFOUT_B46n	Y11						
4A	VREF4A	IO			DIFFIO_RX_B24p	DIFFOUT_B47p	AG9		DQ12B	DQ15B			
4A	VREF4A	IO			DIFFIO_RX_B24n	DIFFOUT_B47n	AH8		DQ12B	DQ15B			
4A	VREF4A	IO				DIFFOUT_B48p	AE10		DQ12B	DQ15B			
4A	VREF4A	IO				DIFFOUT_B48n	AH9		DQ12B	DQ15B			
4A	VREF4A	IO			DIFFIO_RX_B25p	DIFFOUT_B49p	AE9		DQS12B	DQS15B/CQ15B			
4A	VREF4A	IO			DIFFIO_RX_B25n	DIFFOUT_B49n	AF9		DQSn12B	DQSn15B/DQ15B			
4A	VREF4A	IO				DIFFOUT_B50p	AF8		DQ13B	DQ15B			
4A	VREF4A	IO				DIFFOUT_B50n	AE8		DQ13B	DQ15B			
4A	VREF4A	IO			DIFFIO_RX_B26p	DIFFOUT_B51p	AG7		DQS13B	DQ15B/CQn15B			
4A	VREF4A	IO			DIFFIO_RX_B26n	DIFFOUT_B51n	AH7		DQSn13B	DQ15B			
4A	VREF4A	IO				DIFFOUT_B52p	AG6		DQ13B	DQ15B			
4A	VREF4A	IO				DIFFOUT_B52n	AH6		DQ13B	DQ15B			
4A	VREF4A	IO			DIFFIO_RX_B27p	DIFFOUT_B53p	AG4		DQ14B	DQ16B	DQ17B		
4A	VREF4A	IO			DIFFIO_RX_B27n	DIFFOUT_B53n	AH3		DQ14B	DQ16B	DQ17B		
4A	VREF4A	IO				DIFFOUT_B54p	AH4		DQ14B	DQ16B	DQ17B		
4A	VREF4A	IO				DIFFOUT_B54n	AH5		DQ14B	DQ16B	DQ17B		
4A	VREF4A	IO			DIFFIO_RX_B28p	DIFFOUT_B55p	AG3		DQS14B	DQS16B/CQ16B	DQ17B		
4A	VREF4A	IO			DIFFIO_RX_B28n	DIFFOUT_B55n	AH2		DQSn14B	DQSn16B/DQ16B	DQ17B		
4A	VREF4A	IO				DIFFOUT_B56p	AD9		DQ15B	DQ16B	DQ17B		
4A	VREF4A	IO				DIFFOUT_B56n	AC9		DQ15B	DQ16B	DQ17B		
4A	VREF4A	IO			DIFFIO_RX_B29p	DIFFOUT_B57p	AA9		DQS15B	DQ16B/CQn16B	DQS17B/CQ17B		
4A	VREF4A	IO			DIFFIO_RX_B29n	DIFFOUT_B57n	AB9		DQSn15B	DQ16B	DQSn17B/DQ17B		
4A	VREF4A	IO				DIFFOUT_B58p	Y9		DQ15B	DQ16B	DQ17B		
4A	VREF4A	IO				DIFFOUT_B58n	AA10		DQ15B	DQ16B	DQ17B		
4A	VREF4A	IO			DIFFIO_RX_B30p	DIFFOUT_B59p	AE6		DQ16B	DQ17B	DQ17B		
4A	VREF4A	IO			DIFFIO_RX_B30n	DIFFOUT_B59n	AF6		DQ16B	DQ17B	DQ17B		
4A	VREF4A	IO				DIFFOUT_B60p	AE4		DQ16B	DQ17B	DQ17B		
4A	VREF4A	IO				DIFFOUT_B60n	AE7		DQ16B	DQ17B	DQ17B		

4A	VREF4A	IO			DIFFIO_RX_B31p	DIFFOUT_B61p	AE5		DQS16B	DQS17B/CQ17B	DQ17B/CQn17B		
4A	VREF4A	IO			DIFFIO_RX_B31n	DIFFOUT_B61n	AF5		DQSn16B	DQSn17B/DQ17B	DQ17B		
4A	VREF4A	IO				DIFFOUT_B62p	AB8		DQ17B	DQ17B	DQ17B		
4A	VREF4A	IO				DIFFOUT_B62n	AC8		DQ17B	DQ17B	DQ17B		
4A	VREF4A	IO	RUP4A		DIFFIO_RX_B32p	DIFFOUT_B63p	AC7		DQS17B	DQ17B/CQn17B	DQ17B		
4A	VREF4A	IO	RDN4A		DIFFIO_RX_B32n	DIFFOUT_B63n	AD7		DQSn17B	DQ17B	DQ17B		
4A	VREF4A	IO				DIFFOUT_B64p	AB7		DQ17B	DQ17B	DQ17B		
4A	VREF4A	IO				DIFFOUT_B64n	AD6		DQ17B	DQ17B	DQ17B		
		NC					W10	W6					
		GND					AF3	AB5					
		nIO_PULLUP		nIO_PULLUP			AE3	AB4					
		nCEO		nCEO			AB5	U5					
		DCLK		DCLK			AC5	Y4					
		nCSO		nCSO			AD4	Y6					
		ASDO		ASDO			AA6	Y3					
5A	VREF5A	IO			DIFFIO_TX_R1n	DIFFOUT_R1n	AC3	W4					
5A	VREF5A	IO			DIFFIO_TX_R1p	DIFFOUT_R1p	AC4	W5					
5A	VREF5A	IO	RDN5A		DIFFIO_RX_R1n	DIFFOUT_R2n	AF1	AA3					
5A	VREF5A	IO	RUP5A		DIFFIO_RX_R1p	DIFFOUT_R2p	AE2	AA4					
5A	VREF5A	IO			DIFFIO_TX_R2n	DIFFOUT_R3n	AB3	V6	DQ1R	DQ1R	DQ1R	DQ1R	DQ1R
5A	VREF5A	IO			DIFFIO_TX_R2p	DIFFOUT_R3p	AB4	V7	DQ1R	DQ1R	DQ1R	DQ1R	DQ1R
5A	VREF5A	IO			DIFFIO_RX_R2n	DIFFOUT_R4n	AG1	AB2	DQSn1R	DQ1R	DQ1R	DQSn1R	DQ1R
5A	VREF5A	IO			DIFFIO_RX_R2p	DIFFOUT_R4p	AF2	AB3	DQS1R	DQ1R/CQn1R	DQ1R	DQS1R	DQ1R/CQn1R
5A	VREF5A	IO			DIFFIO_TX_R3n	DIFFOUT_R5n	Y6	U4	DQ1R	DQ1R	DQ1R	DQ1R	DQ1R
5A	VREF5A	IO			DIFFIO_TX_R3p	DIFFOUT_R5p	Y7	T4	DQ1R	DQ1R	DQ1R	DQ1R	DQ1R
5A	VREF5A	IO			DIFFIO_RX_R3n	DIFFOUT_R6n	AE1	AB1	DQSn2R	DQSn1R/DQ1R	DQ1R	DQSn2R	DQSn1R/DQ1R
5A	VREF5A	IO			DIFFIO_RX_R3p	DIFFOUT_R6p	AD1	AA1	DQS2R	DQS1R/CQ1R	DQ1R/CQn1R	DQS2R	DQS1R/CQ1R
5A	VREF5A	IO			DIFFIO_TX_R4n	DIFFOUT_R7n	AA4	V3	DQ2R	DQ1R	DQ1R	DQ2R	DQ1R
5A	VREF5A	IO			DIFFIO_TX_R4p	DIFFOUT_R7p	Y5	V4	DQ2R	DQ1R	DQ1R	DQ2R	DQ1R
5A	VREF5A	IO			DIFFIO_RX_R4n	DIFFOUT_R8n	AC1	W2	DQ2R	DQ1R	DQ1R	DQ2R	DQ1R
5A	VREF5A	IO			DIFFIO_RX_R4p	DIFFOUT_R8p	AC2	W3	DQ2R	DQ1R	DQ1R	DQ2R	DQ1R
5A	VREF5A	IO			DIFFIO_TX_R5n	DIFFOUT_R9n	Y3	U7	DQ3R	DQ2R	DQ1R	DQ3R	
5A	VREF5A	IO			DIFFIO_TX_R5p	DIFFOUT_R9p	Y4	U8	DQ3R	DQ2R	DQ1R	DQ3R	
5A	VREF5A	IO			DIFFIO_RX_R5n	DIFFOUT_R10n	AB1	Y1	DQSn3R	DQ2R	DQSn1R/DQ1R	DQSn3R	
5A	VREF5A	IO			DIFFIO_RX_R5p	DIFFOUT_R10p	AB2	Y2	DQS3R	DQ2R/CQn2R	DQS1R/CQ1R	DQS3R	
5A	VREF5A	IO			DIFFIO_TX_R6n	DIFFOUT_R11n	W8	T7	DQ3R	DQ2R	DQ1R	DQ3R	
5A	VREF5A	IO			DIFFIO_TX_R6p	DIFFOUT_R11p	W9	T8	DQ3R	DQ2R	DQ1R	DQ3R	
5A	VREF5A	IO			DIFFIO_RX_R6n	DIFFOUT_R12n	AA1	W1	DQSn4R	DQSn2R/DQ2R	DQ1R		
5A	VREF5A	IO			DIFFIO_RX_R6p	DIFFOUT_R12p	Y2	V1	DQS4R	DQS2R/CQ2R	DQ1R		
5A	VREF5A	IO			DIFFIO_TX_R7n	DIFFOUT_R13n	W5		DQ4R	DQ2R	DQ1R		
5A	VREF5A	IO			DIFFIO_TX_R7p	DIFFOUT_R13p	W6		DQ4R	DQ2R	DQ1R		
5A	VREF5A	IO			DIFFIO_RX_R7n	DIFFOUT_R14n	Y1		DQ4R	DQ2R	DQ1R		
5A	VREF5A	IO			DIFFIO_RX_R7p	DIFFOUT_R14p	W2		DQ4R	DQ2R	DQ1R		
5A	VREF5A	IO			DIFFIO_TX_R8n	DIFFOUT_R15n	V6						
5A	VREF5A	IO			DIFFIO_TX_R8p	DIFFOUT_R15p	V7						
5A	VREF5A	IO			DIFFIO_RX_R8n	DIFFOUT_R16n	W3						
5A	VREF5A	IO			DIFFIO_RX_R8p	DIFFOUT_R16p	W4						
5C	VREF5C	IO			DIFFIO_TX_R9n	DIFFOUT_R17n	U6	R6					
5C	VREF5C	IO			DIFFIO_TX_R9p	DIFFOUT_R17p	U7	P7					
5C	VREF5C	IO			DIFFIO_RX_R9n	DIFFOUT_R18n	V3	R3	DQSn5R			DQSn5R	
5C	VREF5C	IO			DIFFIO_RX_R9p	DIFFOUT_R18p	V4	R4	DQS5R			DQS5R	
5C	VREF5C	IO			DIFFIO_TX_R10n	DIFFOUT_R19n	U8	P3	DQ5R			DQ5R	
5C	VREF5C	IO			DIFFIO_TX_R10p	DIFFOUT_R19p	U9	P4	DQ5R			DQ5R	
5C	VREF5C	IO			DIFFIO_RX_R10n	DIFFOUT_R20n	W1	U3	DQ5R			DQ5R	
5C	VREF5C	IO			DIFFIO_RX_R10p	DIFFOUT_R20p	V1	T3	DQ5R			DQ5R	
5C	VREF5C	IO			DIFFIO_TX_R11n	DIFFOUT_R21n	T4	P6	DQ6R	DQ5R		DQ6R	DQ5R
5C	VREF5C	IO			DIFFIO_TX_R11p	DIFFOUT_R21p	U5	N6	DQ6R	DQ5R		DQ6R	DQ5R
5C	VREF5C	IO			DIFFIO_RX_R11n	DIFFOUT_R22n	U3	U1	DQSn6R	DQ5R		DQSn6R	DQ5R
5C	VREF5C	IO			DIFFIO_RX_R11p	DIFFOUT_R22p	U4	U2	DQS6R	DQ5R/CQn5R		DQS6R	DQ5R/CQn5R
5C	VREF5C	IO			DIFFIO_TX_R12n	DIFFOUT_R23n	T8	N4	DQ6R	DQ5R		DQ6R	DQ5R
5C	VREF5C	IO			DIFFIO_TX_R12p	DIFFOUT_R23p	T9	N5	DQ6R	DQ5R		DQ6R	DQ5R
5C	VREF5C	IO			DIFFIO_RX_R12n	DIFFOUT_R24n	T2	T1	DQSn7R	DQSn5R/DQ5R		DQSn7R	DQSn5R/DQ5R
5C	VREF5C	IO			DIFFIO_RX_R12p	DIFFOUT_R24p	T3	T2	DQS7R	DQS5R/CQ5R		DQS7R	DQS5R/CQ5R
5C	VREF5C	IO			DIFFIO_TX_R13n	DIFFOUT_R25n	T6	M6	DQ7R	DQ5R		DQ7R	DQ5R

5C	VREF5C	IO			DIFFIO_TX_R13p	DIFFOUT_R25p	R6	M7	DQ7R	DQ5R		DQ7R	DQ5R
5C	VREF5C	IO			DIFFIO_RX_R13n	DIFFOUT_R26n	R4	P1	DQ7R	DQ5R		DQ7R	DQ5R
5C	VREF5C	IO			DIFFIO_RX_R13p	DIFFOUT_R26p	T5	P2	DQ7R	DQ5R		DQ7R	DQ5R
5C	VREF5C	IO			DIFFIO_TX_R14n	DIFFOUT_R27n	R9	M3					
5C	VREF5C	IO			DIFFIO_TX_R14p	DIFFOUT_R27p	R10	M4					
5C	VREF5C	IO	CLK9n		DIFFIO_RX_R14n	DIFFOUT_R28n	U1	N2					
5C	VREF5C	IO	CLK9p		DIFFIO_RX_R14p	DIFFOUT_R28p	U2	N3					
5C	VREF5C	CLK8n	CLK8n				T1	N1					
5C	VREF5C	CLK8p	CLK8p				R1	M1					
		VCCD_PLL_R2					P7	L6					
		VCCA_PLL_R2					R7	L5					
6C	VREF6C	CLK10p	CLK10p				P2	L2					
6C	VREF6C	CLK10n	CLK10n				P1	L1					
6C	VREF6C	IO	CLK11p		DIFFIO_RX_R15p	DIFFOUT_R29p	M1	K2					
6C	VREF6C	IO	CLK11n		DIFFIO_RX_R15n	DIFFOUT_R29n	N1	K1					
6C	VREF6C	IO	PLL_R2_FB_CLKOUT0p		DIFFIO_TX_R15p	DIFFOUT_R30p	P9	L4					
6C	VREF6C	IO	PLL_R2_CLKOUT0n		DIFFIO_TX_R15n	DIFFOUT_R30n	P8	L3					
6C	VREF6C	IO			DIFFIO_RX_R16p	DIFFOUT_R31p	N4	H1	DQ8R	DQ10R		DQ8R	DQ10R
6C	VREF6C	IO			DIFFIO_RX_R16n	DIFFOUT_R31n	P4	J1	DQ8R	DQ10R		DQ8R	DQ10R
6C	VREF6C	IO			DIFFIO_TX_R16p	DIFFOUT_R32p	N7	K8	DQ8R	DQ10R		DQ8R	DQ10R
6C	VREF6C	IO			DIFFIO_TX_R16n	DIFFOUT_R32n	N6	K7	DQ8R	DQ10R		DQ8R	DQ10R
6C	VREF6C	IO			DIFFIO_RX_R17p	DIFFOUT_R33p	P3	K4	DQS8R	DQS10R/CQ10R		DQS8R	DQS10R/CQ10R
6C	VREF6C	IO			DIFFIO_RX_R17n	DIFFOUT_R33n	N2	K3	DQSn8R	DQSn10R/DQ10R		DQSn8R	DQSn10R/DQ10R
6C	VREF6C	IO			DIFFIO_TX_R17p	DIFFOUT_R34p	N5	H7	DQ9R	DQ10R		DQ9R	DQ10R
6C	VREF6C	IO			DIFFIO_TX_R17n	DIFFOUT_R34n	M4	J7	DQ9R	DQ10R		DQ9R	DQ10R
6C	VREF6C	IO			DIFFIO_RX_R18p	DIFFOUT_R35p	L2	F1	DQS9R	DQ10R/CQn10R		DQS9R	DQ10R/CQn10R
6C	VREF6C	IO			DIFFIO_RX_R18n	DIFFOUT_R35n	L1	G1	DQSn9R	DQ10R		DQSn9R	DQ10R
6C	VREF6C	IO			DIFFIO_TX_R18p	DIFFOUT_R36p	N9	J4	DQ9R	DQ10R		DQ9R	DQ10R
6C	VREF6C	IO			DIFFIO_TX_R18n	DIFFOUT_R36n	N8	J3	DQ9R	DQ10R		DQ9R	DQ10R
6C	VREF6C	IO			DIFFIO_RX_R19p	DIFFOUT_R37p	L3	H3	DQ10R			DQ10R	
6C	VREF6C	IO			DIFFIO_RX_R19n	DIFFOUT_R37n	M3	H2	DQ10R			DQ10R	
6C	VREF6C	IO			DIFFIO_TX_R19p	DIFFOUT_R38p	L5	H5	DQ10R			DQ10R	
6C	VREF6C	IO			DIFFIO_TX_R19n	DIFFOUT_R38n	L4	H4	DQ10R			DQ10R	
6C	VREF6C	IO			DIFFIO_RX_R20p	DIFFOUT_R39p	K2	G4	DQS10R			DQS10R	
6C	VREF6C	IO			DIFFIO_RX_R20n	DIFFOUT_R39n	K1	G3	DQSn10R			DQSn10R	
6C	VREF6C	IO			DIFFIO_TX_R20p	DIFFOUT_R40p	L6	H6					
6C	VREF6C	IO			DIFFIO_TX_R20n	DIFFOUT_R40n	M6	J6					
6A	VREF6A	IO			DIFFIO_RX_R21p	DIFFOUT_R41p	H2						
6A	VREF6A	IO			DIFFIO_RX_R21n	DIFFOUT_R41n	J1						
6A	VREF6A	IO			DIFFIO_TX_R21p	DIFFOUT_R42p	K7						
6A	VREF6A	IO			DIFFIO_TX_R21n	DIFFOUT_R42n	K6						
6A	VREF6A	IO			DIFFIO_RX_R22p	DIFFOUT_R43p	G2		DQ11R	DQ13R	DQ14R		
6A	VREF6A	IO			DIFFIO_RX_R22n	DIFFOUT_R43n	H1		DQ11R	DQ13R	DQ14R		
6A	VREF6A	IO			DIFFIO_TX_R22p	DIFFOUT_R44p	K5		DQ11R	DQ13R	DQ14R		
6A	VREF6A	IO			DIFFIO_TX_R22n	DIFFOUT_R44n	K4		DQ11R	DQ13R	DQ14R		
6A	VREF6A	IO			DIFFIO_RX_R23p	DIFFOUT_R45p	F1	E2	DQS11R	DQS13R/CQ13R	DQ14R		
6A	VREF6A	IO			DIFFIO_RX_R23n	DIFFOUT_R45n	G1	E1	DQSn11R	DQSn13R/DQ13R	DQ14R		
6A	VREF6A	IO			DIFFIO_TX_R23p	DIFFOUT_R46p	J4	F8	DQ12R	DQ13R	DQ14R	DQ12R	
6A	VREF6A	IO			DIFFIO_TX_R23n	DIFFOUT_R46n	J3	G8	DQ12R	DQ13R	DQ14R	DQ12R	
6A	VREF6A	IO			DIFFIO_RX_R24p	DIFFOUT_R47p	E2	D2	DQS12R	DQ13R/CQn13R	DQS14R/CQ14R	DQS12R	
6A	VREF6A	IO			DIFFIO_RX_R24n	DIFFOUT_R47n	E1	D1	DQSn12R	DQ13R	DQSn14R/DQ14R	DQSn12R	
6A	VREF6A	IO			DIFFIO_TX_R24p	DIFFOUT_R48p	L9	F7	DQ12R	DQ13R	DQ14R	DQ12R	
6A	VREF6A	IO			DIFFIO_TX_R24n	DIFFOUT_R48n	L8	G6	DQ12R	DQ13R	DQ14R	DQ12R	
6A	VREF6A	IO			DIFFIO_RX_R25p	DIFFOUT_R49p	H4	B1	DQ13R	DQ14R	DQ14R	DQ13R	DQ14R
6A	VREF6A	IO			DIFFIO_RX_R25n	DIFFOUT_R49n	H3	C1	DQ13R	DQ14R	DQ14R	DQ13R	DQ14R
6A	VREF6A	IO			DIFFIO_TX_R25p	DIFFOUT_R50p	K9	F4	DQ13R	DQ14R	DQ14R	DQ13R	DQ14R
6A	VREF6A	IO			DIFFIO_TX_R25n	DIFFOUT_R50n	K8	F3	DQ13R	DQ14R	DQ14R	DQ13R	DQ14R
6A	VREF6A	IO			DIFFIO_RX_R26p	DIFFOUT_R51p	D2	A2	DQS13R	DQS14R/CQ14R	DQ14R/CQn14R	DQS13R	DQS14R/CQ14R
6A	VREF6A	IO			DIFFIO_RX_R26n	DIFFOUT_R51n	D1	B2	DQSn13R	DQSn14R/DQ14R	DQ14R	DQSn13R	DQSn14R/DQ14R
6A	VREF6A	IO			DIFFIO_TX_R26p	DIFFOUT_R52p	J6	E5	DQ14R	DQ14R	DQ14R	DQ14R	DQ14R
6A	VREF6A	IO			DIFFIO_TX_R26n	DIFFOUT_R52n	H5	E4	DQ14R	DQ14R	DQ14R	DQ14R	DQ14R
6A	VREF6A	IO			DIFFIO_RX_R27p	DIFFOUT_R53p	F4	D3	DQS14R	DQ14R/CQn14R	DQ14R	DQS14R	DQ14R/CQn14R
6A	VREF6A	IO			DIFFIO_RX_R27n	DIFFOUT_R53n	F3	E3	DQSn14R	DQ14R	DQ14R	DQSn14R	DQ14R
6A	VREF6A	IO			DIFFIO_TX_R27p	DIFFOUT_R54p	G4	B4	DQ14R	DQ14R	DQ14R	DQ14R	DQ14R

6A	VREF6A	IO			DIFFIO_TX_R27n	DIFFOUT_R54n	G3	C4	DQ14R	DQ14R	DQ14R	DQ14R	DQ14R
6A	VREF6A	IO	RUP6A		DIFFIO_RX_R28p	DIFFOUT_R55p	B1	A4					
6A	VREF6A	IO	RDN6A		DIFFIO_RX_R28n	DIFFOUT_R55n	C1	A3					
6A	VREF6A	IO			DIFFIO_TX_R28p	DIFFOUT_R56p	H6	B5					
6A	VREF6A	IO			DIFFIO_TX_R28n	DIFFOUT_R56n	G5	C5					
		MSEL2		MSEL2			G7	G7					
		MSEL1		MSEL1			J9	C6					
		MSEL0		MSEL0			H8	E7					
		TEMPDIODEn					D4	A6					
		TEMPDIODEp					D3	A5					
		NC					E4	D6					
7A	VREF7A	IO				DIFFOUT_T1n	A2		DQ1T	DQ1T	DQ1T		
7A	VREF7A	IO				DIFFOUT_T1p	C3		DQ1T	DQ1T	DQ1T		
7A	VREF7A	IO	RDN7A		DIFFIO_RX_T1n	DIFFOUT_T2n	A4		DQSn1T	DQ1T	DQ1T		
7A	VREF7A	IO	RUP7A		DIFFIO_RX_T1p	DIFFOUT_T2p	B4		DQS1T	DQ1T/CQn1T	DQ1T		
7A	VREF7A	IO				DIFFOUT_T3n	A3		DQ1T	DQ1T	DQ1T		
7A	VREF7A	IO				DIFFOUT_T3p	B2		DQ1T	DQ1T	DQ1T		
7A	VREF7A	IO			DIFFIO_RX_T2n	DIFFOUT_T4n	D7		DQSn2T	DQSn1T/DQ1T	DQ1T		
7A	VREF7A	IO			DIFFIO_RX_T2p	DIFFOUT_T4p	E7		DQS2T	DQS1T/CQ1T	DQ1T/CQn1T		
7A	VREF7A	IO				DIFFOUT_T5n	G8		DQ2T	DQ1T	DQ1T		
7A	VREF7A	IO				DIFFOUT_T5p	G9		DQ2T	DQ1T	DQ1T		
7A	VREF7A	IO			DIFFIO_RX_T3n	DIFFOUT_T6n	E8		DQ2T	DQ1T	DQ1T		
7A	VREF7A	IO			DIFFIO_RX_T3p	DIFFOUT_T6p	F8		DQ2T	DQ1T	DQ1T		
7A	VREF7A	IO				DIFFOUT_T7n	D6		DQ3T	DQ2T	DQ1T		
7A	VREF7A	IO				DIFFOUT_T7p	E5		DQ3T	DQ2T	DQ1T		
7A	VREF7A	IO			DIFFIO_RX_T4n	DIFFOUT_T8n	C5		DQSn3T	DQ2T	DQSn1T/DQ1T		
7A	VREF7A	IO			DIFFIO_RX_T4p	DIFFOUT_T8p	D5		DQS3T	DQ2T/CQn2T	DQS1T/CQ1T		
7A	VREF7A	IO				DIFFOUT_T9n	B5		DQ3T	DQ2T	DQ1T		
7A	VREF7A	IO				DIFFOUT_T9p	C6		DQ3T	DQ2T	DQ1T		
7A	VREF7A	IO			DIFFIO_RX_T5n	DIFFOUT_T10n	A5		DQSn4T	DQSn2T/DQ2T	DQ1T		
7A	VREF7A	IO			DIFFIO_RX_T5p	DIFFOUT_T10p	A6		DQS4T	DQS2T/CQ2T	DQ1T		
7A	VREF7A	IO				DIFFOUT_T11n	A8		DQ4T	DQ2T	DQ1T		
7A	VREF7A	IO				DIFFOUT_T11p	A9		DQ4T	DQ2T	DQ1T		
7A	VREF7A	IO			DIFFIO_RX_T6n	DIFFOUT_T12n	A7		DQ4T	DQ2T	DQ1T		
7A	VREF7A	IO			DIFFIO_RX_T6p	DIFFOUT_T12p	B7		DQ4T	DQ2T	DQ1T		
7A	VREF7A	IO				DIFFOUT_T13n	B8		DQ5T	DQ3T			
7A	VREF7A	IO				DIFFOUT_T13p	F9		DQ5T	DQ3T			
7A	VREF7A	IO			DIFFIO_RX_T7n	DIFFOUT_T14n	C8		DQSn5T	DQ3T			
7A	VREF7A	IO			DIFFIO_RX_T7p	DIFFOUT_T14p	D8		DQS5T	DQ3T/CQn3T			
7A	VREF7A	IO				DIFFOUT_T15n	D9		DQ5T	DQ3T			
7A	VREF7A	IO				DIFFOUT_T15p	C9		DQ5T	DQ3T			
7A	VREF7A	IO			DIFFIO_RX_T8n	DIFFOUT_T16n	E10		DQSn6T	DQSn3T/DQ3T			
7A	VREF7A	IO			DIFFIO_RX_T8p	DIFFOUT_T16p	F10		DQS6T	DQS3T/CQ3T			
7A	VREF7A	IO				DIFFOUT_T17n	H10		DQ6T	DQ3T			
7A	VREF7A	IO				DIFFOUT_T17p	G10		DQ6T	DQ3T			
7A	VREF7A	IO			DIFFIO_RX_T9n	DIFFOUT_T18n	D10		DQ6T	DQ3T			
7A	VREF7A	IO			DIFFIO_RX_T9p	DIFFOUT_T18p	E11		DQ6T	DQ3T			
7A	VREF7A	IO				DIFFOUT_T19n	H11						
7A	VREF7A	IO				DIFFOUT_T19p	J10						
7A	VREF7A	IO			DIFFIO_RX_T10n	DIFFOUT_T20n	J11						
7A	VREF7A	IO			DIFFIO_RX_T10p	DIFFOUT_T20p	J12						
7C	VREF7C	IO				DIFFOUT_T21n	B10	D7	DQ7T	DQ7T		DQ7T	DQ7T
7C	VREF7C	IO				DIFFOUT_T21p	C10	D9	DQ7T	DQ7T		DQ7T	DQ7T
7C	VREF7C	IO			DIFFIO_RX_T11n	DIFFOUT_T22n	A10	C10	DQSn7T	DQ7T		DQSn7T	DQ7T
7C	VREF7C	IO			DIFFIO_RX_T11p	DIFFOUT_T22p	B11	D10	DQS7T	DQ7T/CQn7T		DQS7T	DQ7T/CQn7T
7C	VREF7C	IO				DIFFOUT_T23n	A11	D8	DQ7T	DQ7T		DQ7T	DQ7T
7C	VREF7C	IO				DIFFOUT_T23p	A12	C9	DQ7T	DQ7T		DQ7T	DQ7T
7C	VREF7C	IO			DIFFIO_RX_T12n	DIFFOUT_T24n	C12	A7	DQSn8T	DQSn7T/DQ7T		DQSn8T	DQSn7T/DQ7T
7C	VREF7C	IO			DIFFIO_RX_T12p	DIFFOUT_T24p	D11	B7	DQS8T	DQS7T/CQ7T		DQS8T	DQS7T/CQ7T
7C	VREF7C	IO				DIFFOUT_T25n	E13	A9	DQ8T	DQ7T		DQ8T	DQ7T
7C	VREF7C	IO				DIFFOUT_T25p	D13	C7	DQ8T	DQ7T		DQ8T	DQ7T
7C	VREF7C	IO			DIFFIO_RX_T13n	DIFFOUT_T26n	C13	A8	DQ8T	DQ7T		DQ8T	DQ7T
7C	VREF7C	IO			DIFFIO_RX_T13p	DIFFOUT_T26p	D12	B8	DQ8T	DQ7T		DQ8T	DQ7T
7C	VREF7C	IO				DIFFOUT_T27n	G12	F10	DQ9T			DQ9T	

7C	VREF7C	IO				DIFFOUT_T27p	F12	G10	DQ9T			DQ9T	
7C	VREF7C	IO			DIFFIO_RX_T14n	DIFFOUT_T28n	F13	F9	DQSn9T			DQSn9T	
7C	VREF7C	IO			DIFFIO_RX_T14p	DIFFOUT_T28p	G13	G9	DQS9T			DQS9T	
7C	VREF7C	IO				DIFFOUT_T29n	H14	H10	DQ9T			DQ9T	
7C	VREF7C	IO				DIFFOUT_T29p	J14	G11	DQ9T			DQ9T	
7C	VREF7C	IO			DIFFIO_RX_T15n	DIFFOUT_T30n	A13	C11					
7C	VREF7C	IO			DIFFIO_RX_T15p	DIFFOUT_T30p	B13	D11					
7C	VREF7C	IO	CLK13n			DIFFOUT_T31n	A14	A11					
7C	VREF7C	IO	CLK13p			DIFFOUT_T31p	B14	B11					
7C	VREF7C	IO	CLK12n		DIFFIO_RX_T16n	DIFFOUT_T32n	C14	A10					
7C	VREF7C	IO	CLK12p		DIFFIO_RX_T16p	DIFFOUT_T32p	D14	B10					
		VCC_CLKIN7C					F14	E11					
		VCCD_PLL_T1					G15	G12					
		VCCA_PLL_T1					F15	F12					
		VCC_CLKIN8C					F16	F13					
8C	VREF8C	IO	CLK14p		DIFFIO_RX_T17p	DIFFOUT_T33p	D15	A13					
8C	VREF8C	IO	CLK14n		DIFFIO_RX_T17n	DIFFOUT_T33n	C15	A12					
8C	VREF8C	IO	CLK15p			DIFFOUT_T34p	B16	D12					
8C	VREF8C	IO	CLK15n			DIFFOUT_T34n	A15	C12					
8C	VREF8C	IO	PLL_T1_FBp/CLKOUT1		DIFFIO_RX_T18p	DIFFOUT_T35p	B17	C13					
8C	VREF8C	IO	PLL_T1_FBn/CLKOUT2		DIFFIO_RX_T18n	DIFFOUT_T35n	A16	B13					
8C	VREF8C	IO	PLL_T1_CLKOUT0p			DIFFOUT_T36p	J16	H14					
8C	VREF8C	IO	PLL_T1_CLKOUT0n			DIFFOUT_T36n	J15	G14					
8C	VREF8C	IO			DIFFIO_RX_T19p	DIFFOUT_T37p	E16	D14					
8C	VREF8C	IO			DIFFIO_RX_T19n	DIFFOUT_T37n	D16	D13					
8C	VREF8C	IO	PLL_T1_CLKOUT3			DIFFOUT_T38p	G16	E14					
8C	VREF8C	IO	PLL_T1_CLKOUT4			DIFFOUT_T38n	H16	F14					
8C	VREF8C	IO			DIFFIO_RX_T20p	DIFFOUT_T39p	B19	A15	DQ10T	DQ11T		DQ10T	DQ11T
8C	VREF8C	IO			DIFFIO_RX_T20n	DIFFOUT_T39n	A19	A14	DQ10T	DQ11T		DQ10T	DQ11T
8C	VREF8C	IO				DIFFOUT_T40p	A17	B14	DQ10T	DQ11T		DQ10T	DQ11T
8C	VREF8C	IO				DIFFOUT_T40n	A18	D15	DQ10T	DQ11T		DQ10T	DQ11T
8C	VREF8C	IO			DIFFIO_RX_T21p	DIFFOUT_T41p	C19	C15	DQS10T	DQS11T/CQ11T		DQS10T	DQS11T/CQ11T
8C	VREF8C	IO			DIFFIO_RX_T21n	DIFFOUT_T41n	C18	C14	DQSn10T	DQSn11T/DQ11T		DQSn10T	DQSn11T/DQ11T
8C	VREF8C	IO				DIFFOUT_T42p	F17	C17	DQ11T	DQ11T		DQ11T	DQ11T
8C	VREF8C	IO				DIFFOUT_T42n	C17	B17	DQ11T	DQ11T		DQ11T	DQ11T
8C	VREF8C	IO			DIFFIO_RX_T22p	DIFFOUT_T43p	E17	A17	DQS11T	DQ11T/CQn11T		DQS11T	DQ11T/CQn11T
8C	VREF8C	IO			DIFFIO_RX_T22n	DIFFOUT_T43n	D17	A16	DQSn11T	DQ11T		DQSn11T	DQ11T
8C	VREF8C	IO				DIFFOUT_T44p	D18	D16	DQ11T	DQ11T		DQ11T	DQ11T
8C	VREF8C	IO				DIFFOUT_T44n	F18	C16	DQ11T	DQ11T		DQ11T	DQ11T
8A	VREF8A	IO			DIFFIO_RX_T23p	DIFFOUT_T45p	G18						
8A	VREF8A	IO			DIFFIO_RX_T23n	DIFFOUT_T45n	F19						
8A	VREF8A	IO				DIFFOUT_T46p	J18						
8A	VREF8A	IO				DIFFOUT_T46n	J19						
8A	VREF8A	IO			DIFFIO_RX_T24p	DIFFOUT_T47p	B20		DQ12T	DQ15T			
8A	VREF8A	IO			DIFFIO_RX_T24n	DIFFOUT_T47n	A21		DQ12T	DQ15T			
8A	VREF8A	IO				DIFFOUT_T48p	A20		DQ12T	DQ15T			
8A	VREF8A	IO				DIFFOUT_T48n	D19		DQ12T	DQ15T			
8A	VREF8A	IO			DIFFIO_RX_T25p	DIFFOUT_T49p	D20		DQS12T	DQS15T/CQ15T			
8A	VREF8A	IO			DIFFIO_RX_T25n	DIFFOUT_T49n	C20		DQSn12T	DQSn15T/DQ15T			
8A	VREF8A	IO				DIFFOUT_T50p	D21		DQ13T	DQ15T			
8A	VREF8A	IO				DIFFOUT_T50n	C21		DQ13T	DQ15T			
8A	VREF8A	IO			DIFFIO_RX_T26p	DIFFOUT_T51p	B22		DQS13T	DQ15T/CQn15T			
8A	VREF8A	IO			DIFFIO_RX_T26n	DIFFOUT_T51n	A22		DQSn13T	DQ15T			
8A	VREF8A	IO				DIFFOUT_T52p	A23		DQ13T	DQ15T			
8A	VREF8A	IO				DIFFOUT_T52n	B23		DQ13T	DQ15T			
8A	VREF8A	IO			DIFFIO_RX_T27p	DIFFOUT_T53p	B25		DQ14T	DQ16T	DQ17T		
8A	VREF8A	IO			DIFFIO_RX_T27n	DIFFOUT_T53n	A26		DQ14T	DQ16T	DQ17T		
8A	VREF8A	IO				DIFFOUT_T54p	A24		DQ14T	DQ16T	DQ17T		
8A	VREF8A	IO				DIFFOUT_T54n	A25		DQ14T	DQ16T	DQ17T		
8A	VREF8A	IO			DIFFIO_RX_T28p	DIFFOUT_T55p	B26		DQS14T	DQS16T/CQ16T	DQ17T		
8A	VREF8A	IO			DIFFIO_RX_T28n	DIFFOUT_T55n	A27		DQSn14T	DQSn16T/DQ16T	DQ17T		
8A	VREF8A	IO				DIFFOUT_T56p	F20		DQ15T	DQ16T	DQ17T		
8A	VREF8A	IO				DIFFOUT_T56n	E20		DQ15T	DQ16T	DQ17T		
8A	VREF8A	IO			DIFFIO_RX_T29p	DIFFOUT_T57p	H20		DQS15T	DQ16T/CQn16T	DQS17T/CQ17T		

8A	VREF8A	IO			DIFFIO_RX_T29n	DIFFOUT_T57n	G20		DQSn15T	DQ16T	DQSn17T/DQ17T		
8A	VREF8A	IO				DIFFOUT_T58p	H19		DQ15T	DQ16T	DQ17T		
8A	VREF8A	IO				DIFFOUT_T58n	J20		DQ15T	DQ16T	DQ17T		
8A	VREF8A	IO			DIFFIO_RX_T30p	DIFFOUT_T59p	D23		DQ16T	DQ17T	DQ17T		
8A	VREF8A	IO			DIFFIO_RX_T30n	DIFFOUT_T59n	C23		DQ16T	DQ17T	DQ17T		
8A	VREF8A	IO				DIFFOUT_T60p	D22		DQ16T	DQ17T	DQ17T		
8A	VREF8A	IO				DIFFOUT_T60n	D25		DQ16T	DQ17T	DQ17T		
8A	VREF8A	IO			DIFFIO_RX_T31p	DIFFOUT_T61p	D24		DQS16T	DQS17T/CQ17T	DQ17T/CQn17T		
8A	VREF8A	IO			DIFFIO_RX_T31n	DIFFOUT_T61n	C24		DQSn16T	DQSn17T/DQ17T	DQ17T		
8A	VREF8A	IO				DIFFOUT_T62p	F21		DQ17T	DQ17T	DQ17T		
8A	VREF8A	IO				DIFFOUT_T62n	G21		DQ17T	DQ17T	DQ17T		
8A	VREF8A	IO	RUP8A		DIFFIO_RX_T32p	DIFFOUT_T63p	F22		DQS17T	DQ17T/CQn17T	DQ17T		
8A	VREF8A	IO	RDN8A		DIFFIO_RX_T32n	DIFFOUT_T63n	E22		DQSn17T	DQ17T	DQ17T		
8A	VREF8A	IO				DIFFOUT_T64p	E23		DQ17T	DQ17T	DQ17T		
8A	VREF8A	IO				DIFFOUT_T64n	G22		DQ17T	DQ17T	DQ17T		
		VCCIO1A					E26	C18					
		VCCIO1A					H23	F19					
		VCCIO1A					H26						
		VCCIO1C					P26	H22					
		VCCIO1C					R23	K17					
		VCCIO2C					T26	P22					
		VCCIO2C					V22	R17					
		VCCIO2A					W26	R16					
		VCCIO2A					AD26	Y20					
		VCCIO2A					AA22						
		VCCIO3A					AC22						
		VCCIO3A					AF22						
		VCCIO3A					AF25						
		VCCIO3A					AC18						
		VCCIO3C					AF18	T14					
		VCCIO3C					AC15	Y13					
		VCCIO4C					AB12	W10					
		VCCIO4C					AF13	Y8					
		VCCIO4A					AC6						
		VCCIO4A					AF4						
		VCCIO4A					AF7						
		VCCIO4A					AD10						
		VCCIO5A					AA7	R7					
		VCCIO5A					AD3	Y5					
		VCCIO5A					AA3						
		VCCIO5C					P6	N7					
		VCCIO5C					R3	R1					
		VCCIO6C					L7	G2					
		VCCIO6C					N3	K6					
		VCCIO6A					E3	D5					
		VCCIO6A					K3	C3					
		VCCIO6A					H7						
		VCCIO7A					C7						
		VCCIO7A					F7						
		VCCIO7A					F11						
		VCCIO7A					C4						
		VCCIO7C					C11	E8					
		VCCIO7C					G14	C8					
		VCCIO8C					C16	B16					
		VCCIO8C					G17	G13					
		VCCIO8A					C25						
		VCCIO8A					F23						
		VCCIO8A					E19						
		VCCIO8A					C22						
		VCCL					R15	L11					
		VCCL					L17	K14					
		VCCL					V14	P12					
		VCCL					V18	N13					
		VCCL					U11	N11					

		VCCL					U13	N9					
		VCCL					U15	M12					
		VCCL					U17	M10					
		VCCL					T12	L13					
		VCCL					T14	K12					
		VCCL					T16	K10					
		VCCL					R13	J13					
		VCCL					R17	J11					
		VCCL					P12						
		VCCL					P14						
		VCCL					P16						
		VCCL					P18						
		VCCL					N13						
		VCCL					N15						
		VCCL					N17						
		VCCL					M12						
		VCCL					M14						
		VCCL					M16						
		VCCL					L11						
		VCC					T18	J9					
		VCC					V12	P14					
		VCC					V16	M14					
		VCC					R11	L9					
		VCC					N11						
		VCC					M18						
		VCC					L13						
		VCC					L15						
		GND					R14	M11					
		DNU					P15	L12					
		GND					K11	H18					
		GND					B24	AB22					
		GND					AG2	AA20					
		GND					AG5	AA17					
		GND					AG8	AA14					
		GND					AG11	AA11					
		GND					AG14	AA8					
		GND					AG17	AA5					
		GND					AG20	AA2					
		GND					AG23	Y21					
		GND					AG26	V17					
		GND					AF27	V14					
		GND					AD2	V11					
		GND					AD5	V8					
		GND					AD8	V5					
		GND					AD11	V2					
		GND					AD14	U21					
		GND					AD17	U18					
		GND					AD20	R14					
		GND					AD23	R11					
		GND					AC24	R8					
		GND					AC27	R5					
		GND					AA2	R2					
		GND					AA5	P21					
		GND					AA8	P18					
		GND					AA11	P15					
		GND					AA14	P13					
		GND					AA17	P11					
		GND					AA20	P9					
		GND					Y12	N14					
		GND					Y16	N12					
		GND					Y21	N10					
		GND					Y24	M13					
		GND					Y27	M9					
		GND					W12	M8					

		GND					W14	M5					
		GND					W16	M2					
		GND					W18	L21					
		GND					V2	L18					
		GND					V5	L15					
		GND					V8	L14					
		GND					V11	L10					
		GND					V13	K13					
		GND					V15	K11					
		GND					V17	K9					
		GND					V19	J14					
		GND					U10	J12					
		GND					U12	J10					
		GND					U14	J8					
		GND					U16	J5					
		GND					U18	J2					
		GND					U21	H21					
		GND					U24	H15					
		GND					U27	H12					
		GND					T11	H9					
		GND					T13	F5					
		GND					T15	F2					
		GND					T17	E21					
		GND					T19	E18					
		GND					R2	E15					
		GND					R5	E12					
		GND					R8	E9					
		GND					R12	E6					
		GND					R16	C2					
		GND					R18	B21					
		GND					P11	B18					
		GND					P13	B15					
		GND					P17	B12					
		GND					P21	B9					
		GND					P24	B6					
		GND					P27	B3					
		GND					N10	A1					
		GND					N12						
		GND					N14						
		GND					N16						
		GND					N18						
		GND					M2						
		GND					M5						
		GND					M8						
		GND					M11						
		GND					M13						
		GND					M15						
		GND					M17						
		GND					M19						
		GND					L10						
		GND					L12						
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		GND					L21						
		GND					L24						
		GND					L27						
		GND					K13						
		GND					K15						
		GND					K17						
		GND					K19						
		GND					J2						
		GND					J5						
		GND					J8						

		GND					J13						
		GND					J17						
		GND					H9						
		GND					H12						
		GND					H15						
		GND					H18						
		GND					H21						
		GND					H24						
		GND					H27						
		GND					F2						
		GND					F5						
		GND					E6						
		GND					E9						
		GND					E12						
		GND					E15						
		GND					E18						
		GND					E21						
		GND					E24						
		GND					E27						
		GND					C2						
		GND					B3						
		GND					B6						
		GND					B9						
		GND					B12						
		GND					B15						
		GND					B18						
		GND					B21						
		GND					B27						
		VCCPD1A					L19	J15					
		VCCPD1C					N19	K15					
		VCCPD2C					R19	N15					
		VCCPD2A					U19	R15					
		VCCPD3A					W17						
		VCCPD3C					W15	R12					
		VCCPD4C					W13	P10					
		VCCPD4A					W11						
		VCCPD5A					V10	P8					
		VCCPD5C					T10	N8					
		VCCPD6C					P10	L8					
		VCCPD6A					M10	H8					
		VCCPD7A					K12						
		VCCPD7C					K14	H11					
		VCCPD8C					K16	H13					
		VCCPD8A					K18						
	VREF1A	VREF1A	VREF1A				K22	G18					
	VREF1C	VREF1C	VREF1C				N22	K18					
	VREF2C	VREF2C	VREF2C				U22	N18					
	VREF2A	VREF2A	VREF2A				Y22	T18					
	VREF3A	VREF3A	VREF3A				AB18						
	VREF3C	VREF3C	VREF3C				AA16	V12					
	VREF4C	VREF4C	VREF4C				AA12	V10					
	VREF4A	VREF4A	VREF4A				AB10						
	VREF5A	VREF5A	VREF5A				W7	T5					
	VREF5C	VREF5C	VREF5C				T7	P5					
	VREF6C	VREF6C	VREF6C				M7	K5					
	VREF6A	VREF6A	VREF6A				J7	G5					
	VREF7A	VREF7A	VREF7A				G11						
	VREF7C	VREF7C	VREF7C				H13	E10					
	VREF8C	VREF8C	VREF8C				H17	E13					
	VREF8A	VREF8A	VREF8A				G19						
		VCCPT					G23	F17					
		VCCPT					R24	L17					
		VCCPT					AC23	U17					
		VCCPT					AD15	T11					

		VCCPT					AB6	U6					
		VCCPT					P5	L7					
		VCCPT					G6	F6					
		VCCPT					E14	F11					
		VCCPGM					AA21	T16					
		VCCPGM					Y8	T6					
		VCCBAT					F6	D4					
		NC					V9	W19					
		NC					AE25						
		NC					U20						
		NC					M9						
		NC					L20						
		NC					K10						
		NC					J21						

Note:
(1) When not used as clocks, the CQn and DQSn pins can be used as DQ pins.

Pin Name	Pin Type (1st and 2nd Function)	Pin Description
	Supply and Reference Pins	
VCCL	Power	VCCL supplies power to the core voltage power supply pins.
VCC	Power	VCC supplies power to the peripheral circuitry.
RUP[1..8]A	I/O, Input	Reference pins for I/O banks. The RUP pins share the same VCCIO with the I/O bank where they are located. The external precision resistor RUP must be connected to the designated RUP pin within the bank. If not required, this pin is a regular I/O pin.
RDN[1..8]A	I/O, Input	Reference pins for I/O banks. The RDN pins share the same GND with the I/O bank where they are located. The external precision resistor RDN must be connected to the designated RDN pin within the bank. If not required, this pin is a regular I/O pin.
VCCIO[1..8][A,B,C]	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all LVDS, LVCMOS(1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V, 3.3 V), HSTL(12, 15, 18), SSTL(15, 18, 2), 3.0-V PCI/PCI-X I/O, and LVTTL(3.0 V, 3.3 V) I/O standards. VCCIO also supplies power to the input buffers used for LVCMOS(1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V, 3.3 V), 3.0-V PCI/PCI-X and LVTTL(3.0 V, 3.3 V) I/O standards.
VREF[1..8][A,B,C]	Power	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-referenced pins for the bank.
VCCA_PLL[L[1:4],R[1:4],T[1:2],B[1:2]]	Power	Analog power for PLLs[L[1:4],R[1:4],T[1:2],B[1:2]]. You must connect these pins to 2.5 V, even if the PLL is not used. You are advised to keep this pin isolated from other VCC for better jitter performance.
VCCD_PLL[L[1:4],R[1:4],T[1:2],B[1:2]]	Power	Digital power for PLLs[L[1:4],R[1:4],T[1:2],B[1:2]]. You must connect these pins to 1.1 V, even if the PLL is not used.
VCCPT	Power	Power supply for the programmable power technology. Connect to 2.5 V.
VCCPGM	Power	Power supply for configuration pins. Can be connected to 1.8 V, 2.5 V, 3.0 V, or 3.3 V depending on the particular design.
VCCPD[1..8][A,B,C]	Power	Dedicated power pins. This supply is used to power the I/O pre-drivers. This can be connected to 3.3 V, 3.0 V, or 2.5 V. VCCPD for 3.3-V I/O standard is 3.3 V, VCCPD for 3.0-V I/O standard is 3.0 V, and VCCPD for 2.5-V/1.8-V/1.2-V I/O standards is 2.5 V.
VCCBAT	Power	Battery back-up power supply for design security volatile key register. Connect to 2.5 V.
VCC_CLKIN[3,4,7,8]	Power	Differential clock input power supply for top and bottom I/O banks. Connect to 2.5 V.
GND	Ground	Device ground pins.
DNU	Do Not Use	Do not connect to power or ground or any other signal; must be left floating.
NC	No Connect	Do not drive signals into these pins.
	Dedicated Configuration/JTAG Pins	
nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-ups on the user I/O pins and dual-purpose I/O pins (nCSO, ASDO, DATA[7..0], CLKUSR, INIT_DONE, DEV_OE, DEV_CLRn) are on or off before and during configuration. A logic high (1.5 V, 1.8 V, 2.5 V, 3.0 V, or 3.3 V) turns off the weak pull-up, while a logic low turns them on.
TEMPDIODEp	Input	Pin used in conjunction with the temperature-sensing diode (bias-high input) inside the Stratix III device.
TEMPDIODEn	Input	Pin used in conjunction with the temperature-sensing diode (bias-low input) inside the Stratix III device.
MSEL[3..0]	Input	Configuration input pins that set the Stratix III device configuration scheme.

Pin Name	Pin Type (1st and 2nd Function)	Pin Description
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user mode will cause the FPGA to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic high level will initiate reconfiguration.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration Done pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode. It is not available as a user I/O pin.
nCEO	Output	Output that drives low when device configuration is complete.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization. It is not available as a user I/O pin.
PORSEL	Input	Dedicated input that selects between a POR time of 12 ms or 100 ms. A logic high (1.5 V, 1.8 V, 2.5 V, 3.0 V, 3.3 V) selects a POR time of 12 ms and a logic low selects a POR time of 100 ms.
TCK	Input	Dedicated JTAG input pin. Connect TCK to GND if the JTAG circuitry is not used.
TMS	Input	Dedicated JTAG input pin. Connect TMS to VCCPD if the JTAG circuitry is not used.
TDI	Input	Dedicated JTAG input pin. Connect TDI to VCCPD if the JTAG circuitry is not used.
TDO	Output	Dedicated JTAG output pin.
TRST	Input	Dedicated active-low JTAG input pin. TRST is used to asynchronously reset the JTAG boundary-scan circuit.
Clock and PLL Pins		
CLK[1,3,8,10]p	Clock, Input	Dedicated high-speed clock input pins 1, 3, 8, and 10 that can also be used for data inputs. OCT Rd is not supported on these pins.
CLK[1,3,8,10]n	Clock, Input	Dedicated negative clock input pins for differential clock input that can also be used for data inputs. OCT Rd is not supported on these pins.
CLK[0,2,9,11]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is supported on these pins.
CLK[0,2,9,11]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is supported on these pins.
CLK[4..7,12..15]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is not supported on these pins.
CLK[4..7,12..15]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is not supported on these pins.
PLL_[L1,L4,R1,R4]_CLKp	Clock, Input	Dedicated clock input pins to PLL L1, L4, R1, and R4 respectively.
PLL_[L1,L4,R1,R4]_CLKn	Clock, Input	Dedicated negative clock input pins for dfferential clock input to PLL L1, L4, R1, and R4 respectively.
PLL_[L2,L3,R2,R3]_CLKOUT0n	I/O, Clock	Each left and right PLL supports 2 clock I/O pins, configured either as 2 single-ended I/O or one differential I/O pair. When using both pins as single-ended I/Os, PLL_#_CLKOUT0n can be the clock output while the PLL_#_FB_CLKOUT0p is the external feedback input pin.
PLL_[L2,L3,R2,R3]_FB_CLKOUT0p	I/O, Clock	
PLL_[T1,T2,B1,B2]_FBp/CLKOUT1	I/O, Clock	Dual-purpose I/O pins that can be used as two single-ended outputs or one differential external feedback input pin.
PLL_[T1,T2,B1,B2]_FBn/CLKOUT2	I/O, Clock	
PLL_[T1,T2,B1,B2]_CLKOUT[3,4]	I/O, Clock	These pins can be used as I/O pins or two single-ended clock ouput pins.
PLL_[T1,T2,B1,B2]_CLKOUT0[p,n]	I/O, Clock	I/O pins that be used as two single-ended clock output pins or one differential clock output pair.

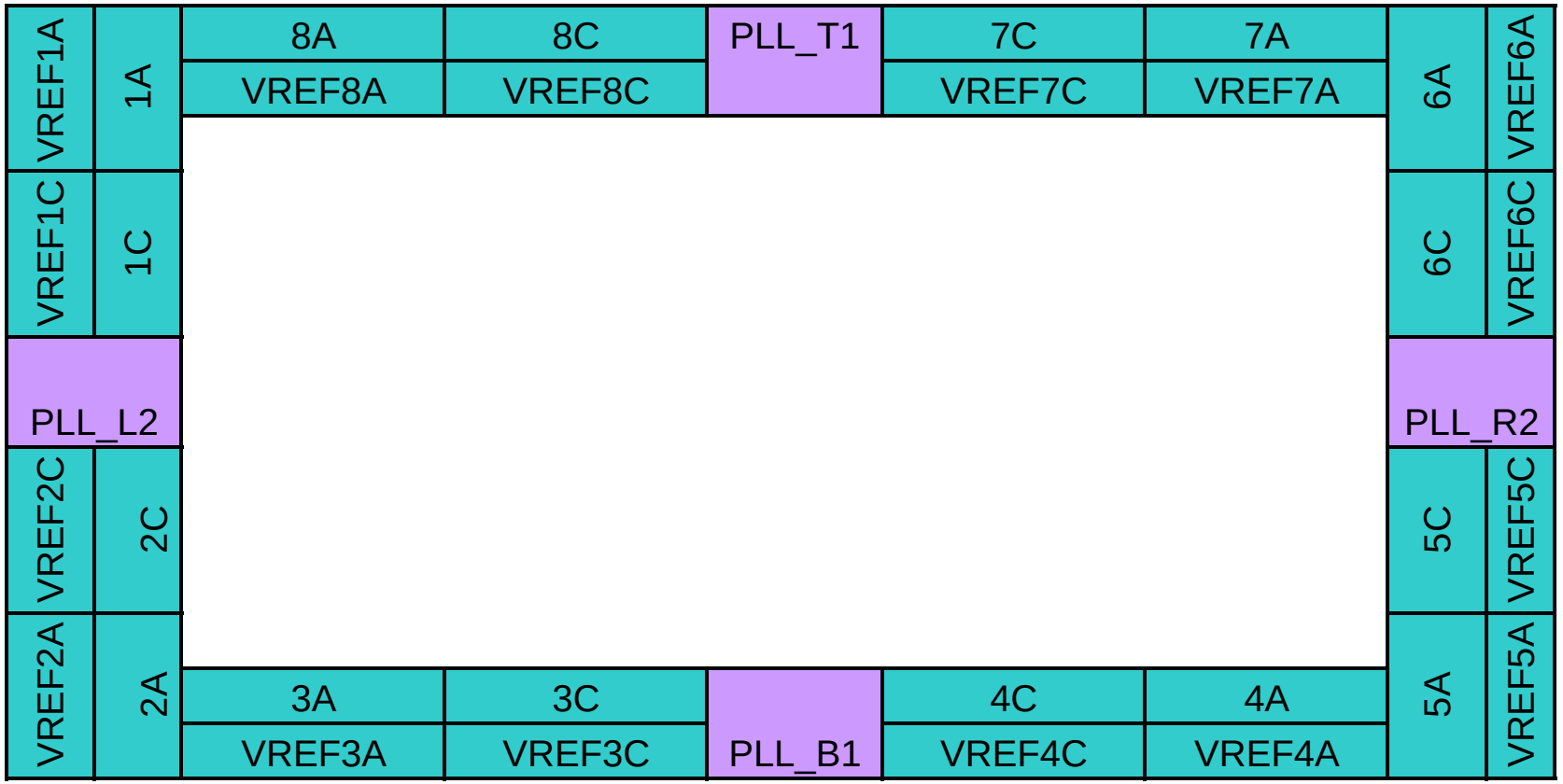
Pin Name	Pin Type (1st and 2nd Function)	Pin Description
	Optional/Dual-Purpose Configuration Pins	
nCSO	I/O, Output	Dedicated output control signal from the Stratix III FPGA to the serial configuration device in AS mode that enables the configuration device.
ASDO	I/O, Output	Control signal from the Stratix III FPGA to the serial configuration device in AS mode used to read out configuration data.
DCLK	Input (PS, FPP) Output (AS)	Dedicated configuration clock pin. In PS and FPP configuration modes, DCLK is used to clock configuration data from an external source into the Stratix III device. In AS mode, DCLK is an output from the Stratix III device that provides timing for the configuration interface.
CRC_ERROR	I/O, Output	Active-high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled.
DEV_CLRn	I/O, Input	Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high (VCCPGM), all registers behave as programmed.
DEV_OE	I/O, Input	Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high (VCCPGM), all I/O pins behave as defined in the design.
DATA0	I/O, Input	Dual-purpose configuration data input pin. The DATA0 pin can be used for bit-wide configuration or as an I/O pin after configuration is complete.
DATA[7..1]	I/O, Input	Dual-purpose configuration data input pins. The DATA[7..1] pins can be used for byte-wide configuration or as regular I/O pins. These pins can also be used as user I/O pins after configuration.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin.
	Differential I/O Pins	
DIFFIO_RX[##]p/n	I/O, RX channel	These are true LVDS receiver channels on side and column I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_TX[##]p/n	I/O, TX channel	These are true LVDS transmitter channels on side I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFOUT_[##]p/n	I/O, TX channel	These are emulated LVDS output channels. On column I/O banks, there are true LVDS input buffers, but no true LVDS output buffers. However, all column user I/Os, including I/Os with true LVDS input buffers, can be configured as emulated LVDS output buffers. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
	External Memory Interface Pins	
DQS[1..44][T,B], DQS[1..40][L,R]	I/O, DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase-shift circuitry. The shifted DQS signal can also drive to internal logic.
DQSn[1..44][T,B], DQSn[1..40][L,R]	I/O, DQSn	Optional complementary data strobe signal for use in QDRII SRAM. These pins drive to dedicated DQS phase-shift circuitry.

Pin Name	Pin Type (1st and 2nd Function)	Pin Description
DQ[1..44][T,B],DQ[1..40][L,R]	I/O, DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.
CQ[1..44][T,B], CQ[1..40][L,R]	DQS	Optional data strobe signal for use in QDRII SRAM. These are the pins for echo clocks.
CQn[1..44][T,B], CQ[1..40][L,R]	DQS	Optional complementary data strobe signal for use in QDRII SRAM. These are the pins for echo clocks.

Notes:

(1) The pin definitions are prepared based on the device with the largest density, EP3SL340. Refer to the pin list for the availability of pins in each density.

(2) Some of the pull-up or pull-down resistors mentioned in the table above may not be required, depending on the exact device configuration scheme.
Should you be required to use a different configuration scheme, the ability to NC or short them may be valuable during the debug phase.
For more information, refer to the *Configuring Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook* .



Note:

1. This is only a pictorial representation to provide an idea of placement on the device. Refer to the pin list and the Quartus® II software for exact locations.

Version Number	Date	Changes Made
1.0	11/23/2007	Initial Release