



## Pin Information For The Stratix™ GX EP1SGX10D Device, ver 1.7

Bank Number	VREF Bank	Pin Name/Function	Optionn Function(s)	Configuration Function	F672	DQS for x32
B2	VREF0B2	INPUT	DIFFIO_RX21p		F25	
B2	VREF0B2	INPUT	DIFFIO_RX21n		F26	
B2	VREF0B2	IO	DIFFIO_TX21p		H19	
B2	VREF0B2	IO	DIFFIO_TX21n		H20	
B2	VREF0B2	INPUT	DIFFIO_RX20p/RUP2		G25	
B2	VREF0B2	INPUT	DIFFIO_RX20n/RDN2		G26	
B2	VREF0B2	IO	DIFFIO_TX20p		J21	
B2	VREF0B2	IO	DIFFIO_TX20n		J22	
B2	VREF0B2	INPUT	DIFFIO_RX19p		H25	
B2	VREF0B2	INPUT	DIFFIO_RX19n		H26	
B2	VREF0B2	IO	DIFFIO_TX19p		K21	
B2	VREF0B2	IO	DIFFIO_TX19n		K22	
B2	VREF0B2	VREF0B2			L17	
B2	VREF0B2	INPUT	DIFFIO_RX18p		J23	
B2	VREF0B2	INPUT	DIFFIO_RX18n		J24	
B2	VREF0B2	IO	DIFFIO_TX18p		J19	
B2	VREF0B2	IO	DIFFIO_TX18n		J20	
B2	VREF0B2	INPUT	DIFFIO_RX17p		H23	
B2	VREF0B2	INPUT	DIFFIO_RX17n		H24	
B2	VREF0B2	IO	DIFFIO_TX17p		K19	
B2	VREF0B2	IO	DIFFIO_TX17n		K20	
B2	VREF0B2	INPUT	DIFFIO_RX16p		J25	
B2	VREF0B2	INPUT	DIFFIO_RX16n		J26	
B2	VREF0B2	IO	DIFFIO_TX16p		L21	
B2	VREF0B2	IO	DIFFIO_TX16n		L22	
B2	VREF1B2	INPUT	DIFFIO_RX15p		K25	
B2	VREF1B2	INPUT	DIFFIO_RX15n		K26	
B2	VREF1B2	IO	DIFFIO_TX15p		K17	
B2	VREF1B2	IO	DIFFIO_TX15n		K18	
B2	VREF1B2	INPUT	DIFFIO_RX14p		K23	
B2	VREF1B2	INPUT	DIFFIO_RX14n		K24	
B2	VREF1B2	IO	DIFFIO_TX14p		L19	
B2	VREF1B2	IO	DIFFIO_TX14n		L20	
B2	VREF1B2	INPUT	DIFFIO_RX13p		L23	
B2	VREF1B2	INPUT	DIFFIO_RX13n		L24	
B2	VREF1B2	IO	DIFFIO_TX13p		M21	
B2	VREF1B2	IO	DIFFIO_TX13n		M22	
B2	VREF1B2	VREF1B2			L18	
B2	VREF1B2	INPUT	DIFFIO_RX12p		M23	
B2	VREF1B2	INPUT	DIFFIO_RX12n		M24	
B2	VREF1B2	IO	DIFFIO_TX12p		M19	
B2	VREF1B2	IO	DIFFIO_TX12n		M20	
B2	VREF1B2	INPUT	DIFFIO_RX11p		L25	
B2	VREF1B2	INPUT	DIFFIO_RX11n		M25	
B2	VREF1B2	IO	DIFFIO_TX11p		M17	
B2	VREF1B2	IO	DIFFIO_TX11n		M18	
B2	VREF1B2	CLK0n			N26	
B2	VREF1B2	CLK0p			N25	
B2	VREF1B2	IO	CLK1n		N24	
B2	VREF1B2	CLK1p			N23	
		VCCA_PLL1			N20	



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Bank Number	VREF Bank	Pin Name/Function	Optionn Function(s)	Configuration Function	F672	DQS for x32
		GND				
		GND_A_PLL1			N22	
		VCCG_PLL1			N21	
		GNDG_PLL1			N19	
		VCCA_PLL2			P21	
		GND				
		GND_A_PLL2			P22	
		VCCG_PLL2			P20	
		GNDG_PLL2			P19	
B1	VREF0B1	CLK2p			P25	
B1	VREF0B1	CLK2n			P26	
B1	VREF0B1	CLK3p			P23	
B1	VREF0B1	IO	CLK3n		P24	
B1	VREF0B1	INPUT	DIFFIO_RX10p		R25	
B1	VREF0B1	INPUT	DIFFIO_RX10n		T25	
B1	VREF0B1	IO	DIFFIO_TX10p		R17	
B1	VREF0B1	IO	DIFFIO_TX10n		R18	
B1	VREF0B1	INPUT	DIFFIO_RX9p		U25	
B1	VREF0B1	INPUT	DIFFIO_RX9n		U26	
B1	VREF0B1	IO	DIFFIO_TX9p		R19	
B1	VREF0B1	IO	DIFFIO_TX9n		R20	
B1	VREF0B1	VREF0B1			R16	
B1	VREF0B1	INPUT	DIFFIO_RX8p		R23	
B1	VREF0B1	INPUT	DIFFIO_RX8n		R24	
B1	VREF0B1	IO	DIFFIO_TX8p		R21	
B1	VREF0B1	IO	DIFFIO_TX8n		R22	
B1	VREF0B1	INPUT	DIFFIO_RX7p		V25	
B1	VREF0B1	INPUT	DIFFIO_RX7n		V26	
B1	VREF0B1	IO	DIFFIO_TX7p		T19	
B1	VREF0B1	IO	DIFFIO_TX7n		T20	
B1	VREF0B1	INPUT	DIFFIO_RX6p		T23	
B1	VREF0B1	INPUT	DIFFIO_RX6n		T24	
B1	VREF0B1	IO	DIFFIO_TX6p		T21	
B1	VREF0B1	IO	DIFFIO_TX6n		T22	
B1	VREF1B1	INPUT	DIFFIO_RX5p		W25	
B1	VREF1B1	INPUT	DIFFIO_RX5n		W26	
B1	VREF1B1	IO	DIFFIO_TX5p		U17	
B1	VREF1B1	IO	DIFFIO_TX5n		U18	
B1	VREF1B1	INPUT	DIFFIO_RX4p		U23	
B1	VREF1B1	INPUT	DIFFIO_RX4n		U24	
B1	VREF1B1	IO	DIFFIO_TX4p		U19	
B1	VREF1B1	IO	DIFFIO_TX4n		U20	
B1	VREF1B1	INPUT	DIFFIO_RX3p		W23	
B1	VREF1B1	INPUT	DIFFIO_RX3n		W24	
B1	VREF1B1	IO	DIFFIO_TX3p		V19	
B1	VREF1B1	IO	DIFFIO_TX3n		V20	
B1	VREF1B1	VREF1B1			T18	
B1	VREF1B1	INPUT	DIFFIO_RX2p		V23	
B1	VREF1B1	INPUT	DIFFIO_RX2n		V24	
B1	VREF1B1	IO	DIFFIO_TX2p		U21	
B1	VREF1B1	IO	DIFFIO_TX2n		U22	



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Bank Number	VREF Bank	Pin Name/Function	Optionn Function(s)	Configuration Function	F672	DQS for x32
B1	VREF1B1	INPUT	DIFFIO_RX1p/RUP1		Y25	
B1	VREF1B1	INPUT	DIFFIO_RX1n/RDN1		Y26	
B1	VREF1B1	IO	DIFFIO_TX1p		V21	
B1	VREF1B1	IO	DIFFIO_TX1n		V22	
B1	VREF1B1	INPUT	DIFFIO_RX0p		Y23	
B1	VREF1B1	INPUT	DIFFIO_RX0n		Y24	
B1	VREF1B1	IO	DIFFIO_TX0p		W19	
B1	VREF1B1	IO	DIFFIO_TX0n		W20	
B8	VREF0B8	IO	DQ9B7		AF23	DQ1B31
B8	VREF0B8	IO	DQ9B6		AE22	DQ1B30
B8	VREF0B8	IO	DQ9B5		AD22	DQ1B29
B8	VREF0B8	IO	DQ9B4		AF22	DQ1B28
B8	VREF0B8	IO	DQ9B3		AF21	DQ1B27
B8	VREF0B8	IO	DQS9B		AE21	
B8	VREF0B8	IO	DQ9B2		AD21	DQ1B26
B8	VREF0B8	IO	DQ8B7		AF20	DQ1B23
B8	VREF0B8	IO	DQ9B1		AD20	DQ1B25
B8	VREF0B8	IO	DQ8B6		AE19	DQ1B22
B8	VREF0B8	IO	DQ9B0		AE20	DQ1B24
B8	VREF0B8	IO	DQ8B5		AD18	DQ1B21
B8	VREF0B8	VREF0B8			V18	
B8	VREF0B8	IO	DQ8B4		AD19	DQ1B20
B8	VREF0B8	IO	DQ8B3		AF19	DQ1B19
B8	VREF0B8	IO	DQS8B		AE18	
B8	VREF0B8	IO	DQ8B2		AF17	DQ1B18
B8	VREF0B8	IO	DQ8B1		AC18	DQ1B17
B8	VREF0B8	IO	DQ8B0		AF18	DQ1B16
B8	VREF0B8	IO	DQ7B2		AB17	DQ1B10
B8	VREF0B8	IO	DQ7B7		Y18	DQ1B15
B8	VREF0B8	IO	DQ7B6		AA18	DQ1B14
B8	VREF0B8	IO	DQ7B5		AB18	DQ1B13
B8	VREF0B8	IO	DQ7B4		W18	DQ1B12
B8	VREF0B8	IO	DQ7B3		AB16	DQ1B11
B8	VREF0B8	IO	DQS7B		AA17	DQS1B
B8	VREF0B8	IO			Y16	
B8	VREF0B8	IO	DQ7B1		W17	DQ1B9
B8	VREF0B8	IO			AA16	
B8	VREF0B8	IO	DQ7B0		Y17	DQ1B8
B8	VREF0B8	IO	DQ6B7		AE17	DQ1B7
B8	VREF1B8	IO	DQ6B6		AD17	DQ1B6
B8	VREF1B8	IO	DQ6B5		AD15	DQ1B5
B8	VREF1B8	IO	DQ6B4		AE16	DQ1B4
B8	VREF1B8	IO		PGM2	T15	
B8	VREF1B8	IO	FCLK3		T16	
B8	VREF1B8	IO	FCLK2		U16	
B8	VREF1B8	IO	DQ6B3		AC17	DQ1B3
B8	VREF1B8	IO	DQS6B		AD16	
B8	VREF1B8	IO	DQ6B2		AC15	DQ1B2
B8	VREF1B8	IO		CRC_ERROR	U15	
B8	VREF1B8	IO	DQ6B1		AC16	DQ1B1
B8	VREF1B8	IO	DQ6B0		AE15	DQ1B0



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Bank Number	VREF Bank	Pin Name/Function	Optionn Function(s)	Configuration Function	F672	DQS for x32
B8	VREF1B8	IO	RDN8		R15	
B8	VREF1B8	IO	RUP8		V16	
B8	VREF1B8	IO			Y15	
B8	VREF1B8	IO		RDYnBSY	W16	
B8	VREF1B8	IO		nCS	R13	
B8	VREF1B8	IO		CS	U14	
B8	VREF1B8	VREF1B8			V17	
B8	VREF1B8	IO	CLK5n		AD14	
B8	VREF1B8	CLK5p			AC14	
B8	VREF1B8	IO	CLK4n		AF14	
B8	VREF1B8	CLK4p			AE14	
B8	VREF1B8	PLL_ENA		PLL_ENA	W15	
B8	VREF1B8	MSEL0		MSEL0	U13	
B8	VREF1B8	MSEL1		MSEL1	T13	
B8	VREF1B8	MSEL2		MSEL2	V14	
B12	VREF1B8	IO	PLL6_OUT3n		AF13	
B12	VREF1B8	IO	PLL6_OUT3p		AE13	
B12	VREF1B8	IO	PLL6_OUT2n		AB14	
B12	VREF1B8	IO	PLL6_OUT2p		AA14	
B11	VREF1B8	IO	PLL6_FBn		AE12	
B11	VREF1B8	IO	PLL6_FBp		AD12	
B11	VREF1B8	IO	PLL6_OUT1n		AB13	
B11	VREF1B8	IO	PLL6_OUT1p		AA13	
B11	VREF1B8	IO	PLL6_OUT0n		AD13	
B11	VREF1B8	IO	PLL6_OUT0p		AC13	
B12		VCC_PLL6_OUTB			R11	
B11		VCC_PLL6_OUTA			V13	
		VCCA_PLL6			T11	
		GND				
		GND_A_PLL6			W12	
		VCCG_PLL6			V12	
		GNDG_PLL6			U12	
B7	VREF0B7	CLK7p			Y12	
B7	VREF0B7	IO	CLK7n		AA12	
B7	VREF0B7	CLK6p			AB12	
B7	VREF0B7	IO	CLK6n		AC12	
B7	VREF0B7	nCE		nCE	P9	
B7	VREF0B7	nCEO		nCEO	T9	
B7	VREF0B7	IO			Y11	
B7	VREF0B7	IO			AA11	
B7	VREF0B7	IO		PGM0	R10	
B7	VREF0B7	nIO_PULLUP		nIO_PULLUP	T10	
B7	VREF0B7	VCCSEL		VCCSEL	R9	
B7	VREF0B7	PORSEL		PORSEL	U10	
B7	VREF0B7	IO		INIT_DONE	U11	
B7	VREF0B7	IO		nRS	U9	
B7	VREF0B7	IO		RUnLU	W11	
B7	VREF0B7	IO		PGM1	U8	
B7	VREF0B7	IO	RDN7		V8	
B7	VREF0B7	IO	RUP7		Y10	
B7	VREF0B7	VREF0B7			V11	



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Bank Number	VREF Bank	Pin Name/Function	Optionn Function(s)	Configuration Function	F672	DQS for x32
B7	VREF0B7	IO	DQ3B7		AF8	DQ0B31
B7	VREF0B7	IO	DQ3B6		AE11	DQ0B30
B7	VREF0B7	IO	DQ3B5		AE10	DQ0B29
B7	VREF0B7	IO	DEV_CLRn		W10	
B7	VREF0B7	IO	DQ3B4		AF10	DQ0B28
B7	VREF0B7	IO	DQ3B3		AE8	DQ0B27
B7	VREF0B7	IO	DQS3B		AE9	
B7	VREF0B7	IO	DQ3B2		AF9	DQ0B26
B7	VREF0B7	IO	DQ3B1		AD9	DQ0B25
B7	VREF0B7	IO	DQ3B0		AD8	DQ0B24
B7	VREF0B7	IO	FCLK5		W9	
B7	VREF0B7	IO	FCLK4		Y9	
B7	VREF1B7	IO	DQ2B7		AC9	DQ0B23
B7	VREF1B7	IO	DQ2B6		Y7	DQ0B22
B7	VREF1B7	IO	DQ2B5		AA7	DQ0B21
B7	VREF1B7	IO	DQ2B4		AC8	DQ0B20
B7	VREF1B7	IO	DQ2B3		AB9	DQ0B19
B7	VREF1B7	IO	DQS2B		AB7	DQS0B
B7	VREF1B7	IO	DQ2B2		Y8	DQ0B18
B7	VREF1B7	IO	DQ1B7		AF5	DQ0B15
B7	VREF1B7	IO	DQ2B1		AA8	DQ0B17
B7	VREF1B7	IO	DQ1B6		AD7	DQ0B14
B7	VREF1B7	IO	DQ2B0		AB8	DQ0B16
B7	VREF1B7	IO	DQ1B5		AF7	DQ0B13
B7	VREF1B7	IO	DQ1B4		AE7	DQ0B12
B7	VREF1B7	IO	DQ1B3		AD6	DQ0B11
B7	VREF1B7	IO	DQS1B		AE6	
B7	VREF1B7	IO	DQ1B2		AF6	DQ0B10
B7	VREF1B7	IO	DQ1B1		AC7	DQ0B9
B7	VREF1B7	IO	DQ1B0		AC6	DQ0B8
B7	VREF1B7	VREF1B7			V10	
B7	VREF1B7	IO			W7	
B7	VREF1B7	IO			V7	
B7	VREF1B7	IO	DQ0B7		AF4	DQ0B7
B7	VREF1B7	IO	DQ0B6		AE5	DQ0B6
B7	VREF1B7	IO	DQ0B5		AC4	DQ0B5
B7	VREF1B7	IO	DQ0B4		AD4	DQ0B4
B7	VREF1B7	IO	DQ0B3		AD5	DQ0B3
B7	VREF1B7	IO	DQS0B		AE4	
B7	VREF1B7	IO	DQ0B2		AE2	DQ0B2
B7	VREF1B7	IO	DQ0B1		AE3	DQ0B1
B7	VREF1B7	IO	DQ0B0		AC5	DQ0B0
B7	VREF1B7	IO			W8	
B15		GXB_RX11n			AC2	
B15		GXB_RX11p			AC1	
B15		GXB_TX11n			AA5	
B15		GXB_TX11p			AA4	
B15		GXB_RX10n			AA2	
B15		GXB_RX10p			AA1	
B15		GXB_TX10n			W5	
B15		GXB_TX10p			W4	



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B15		VCCA_B15			P8	
B15		REFCLKB15n			W2	
B15		REFCLKB15p			W1	
		VCCG_B15			P7	
		GND			P6	
B15		RREFB15			U7	
B15		GXB_RX8n			U2	
B15		GXB_RX8p			U1	
B15		GXB_TX8n			U5	
B15		GXB_TX8p			U4	
B15		GXB_RX9n			R2	
B15		GXB_RX9p			R1	
B15		GXB_TX9n			R5	
B15		GXB_TX9p			R4	
B14		GXB_RX7n			N2	
B14		GXB_RX7p			N1	
B14		GXB_TX7n			N5	
B14		GXB_TX7p			N4	
B14		GXB_RX6n			L2	
B14		GXB_RX6p			L1	
B14		GXB_TX6n			L5	
B14		GXB_TX6p			L4	
B14		VCCA_B14			N7	
B14		REFCLKB14n			J2	
B14		REFCLKB14p			J1	
		VCCG_B14			N8	
		GND			N6	
B14		RREFB14			K7	
B14		GXB_RX4n			G2	
B14		GXB_RX4p			G1	
B14		GXB_TX4n			J5	
B14		GXB_TX4p			J4	
B14		GXB_RX5n			E2	
B14		GXB_RX5p			E1	
B14		GXB_TX5n			G5	
B14		GXB_TX5p			G4	
B4	VREF0B4	IO			G9	
B4	VREF0B4	IO	DQ0T0		B2	DQ0T0
B4	VREF0B4	IO	DQ0T1		C2	DQ0T1
B4	VREF0B4	IO	DQ0T2		C1	DQ0T2
B4	VREF0B4	IO	DQS0T		C3	
B4	VREF0B4	IO	DQ0T3		B3	DQ0T3
B4	VREF0B4	IO	DQ0T4		D4	DQ0T4
B4	VREF0B4	IO	DQ0T5		E4	DQ0T5
B4	VREF0B4	IO	DQ0T6		B4	DQ0T6
B4	VREF0B4	IO	DQ0T7		C4	DQ0T7
B4	VREF0B4	IO			H7	
B4	VREF0B4	IO			H8	
B4	VREF0B4	VREF0B4			K9	
B4	VREF0B4	IO	DQ1T0		E5	DQ0T8
B4	VREF0B4	IO	DQ1T1		C6	DQ0T9



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B4	VREF0B4	IO	DQ1T2		B5	DQ0T10
B4	VREF0B4	IO	DQS1T		C5	
B4	VREF0B4	IO	DQ1T3		D5	DQ0T11
B4	VREF0B4	IO	DQ1T4		A5	DQ0T12
B4	VREF0B4	IO	DQ1T5		A4	DQ0T13
B4	VREF0B4	IO	DQ2T0		B6	DQ0T16
B4	VREF0B4	IO	DQ1T6		E6	DQ0T14
B4	VREF0B4	IO	DQ2T1		E8	DQ0T17
B4	VREF0B4	IO	DQ1T7		D6	DQ0T15
B4	VREF0B4	IO	DQ2T2		F7	DQ0T18
B4	VREF0B4	IO	DQS2T		C7	DQS0T
B4	VREF0B4	IO	DQ2T3		A6	DQ0T19
B4	VREF0B4	IO	DQ2T4		B7	DQ0T20
B4	VREF0B4	IO	DQ2T5		D7	DQ0T21
B4	VREF0B4	IO	DQ2T6		E7	DQ0T22
B4	VREF0B4	IO	DQ2T7		A7	DQ0T23
B4	VREF1B4	IO	FCLK6		G10	
B4	VREF1B4	IO	FCLK7		G7	
B4	VREF1B4	IO	DQ3T0		D8	DQ0T24
B4	VREF1B4	IO	DQ3T1		A8	DQ0T25
B4	VREF1B4	IO	DQ3T2		C9	DQ0T26
B4	VREF1B4	IO	DQS3T		B8	
B4	VREF1B4	IO	DQ3T3		C8	DQ0T27
B4	VREF1B4	IO	DQ3T4		A10	DQ0T28
B4	VREF1B4	IO	DQ3T5		A9	DQ0T29
B4	VREF1B4	IO	DEV_OE		J7	
B4	VREF1B4	IO	DQ3T6		B9	DQ0T30
B4	VREF1B4	IO	DQ3T7		D9	DQ0T31
B4	VREF1B4	VREF1B4			K10	
B4	VREF1B4	IO	RUP4		G11	
B4	VREF1B4	IO	RDN4		G8	
B4	VREF1B4	IO		nWS	H11	
B4	VREF1B4	IO		DATA0	H10	
B4	VREF1B4	IO		DATA1	F8	
B4	VREF1B4	IO		DATA2	K8	
B4	VREF1B4	TMS		TMS	F9	
B4	VREF1B4	TRST		TRST	H9	
B4	VREF1B4	TCK		TCK	J8	
B4	VREF1B4	IO		DATA3	J9	
B4	VREF1B4	IO			E10	
B4	VREF1B4	IO			E11	
B4	VREF1B4	TDI		TDI	F10	
B4	VREF1B4	TDO		TDO	F11	
B4	VREF1B4	IO	CLK12n		D12	
B4	VREF1B4	CLK12p			E12	
B4	VREF1B4	IO	CLK13n		F12	
B4	VREF1B4	CLK13p			G12	
		TEMPDIODEp			J11	
		TEMPDIODEn			J10	
		VCCA_PLL5			H13	
		GND				



## Pin Information For The Stratix™ GX EP1SGX10D Device, ver 1.7

Bank Number	VREF Bank	Pin Name/Function	Optionn Function(s)	Configuration Function	F672	DQS for x32
		GND <sub>A</sub> _PLL5			G13	
		VCCG <sub>A</sub> _PLL5			H12	
		GND <sub>G</sub> _PLL5			J12	
B9		VCC <sub>A</sub> _PLL5_OUTA			J13	
B10		VCC <sub>A</sub> _PLL5_OUTB			K12	
B9	VREF0B3	IO	PLL5_OUT0p		D13	
B9	VREF0B3	IO	PLL5_OUT0n		C13	
B9	VREF0B3	IO	PLL5_OUT1p		C12	
B9	VREF0B3	IO	PLL5_OUT1n		B12	
B9	VREF0B3	IO	PLL5_FBp		F13	
B9	VREF0B3	IO	PLL5_FBn		E13	
B10	VREF0B3	IO	PLL5_OUT2p		F14	
B10	VREF0B3	IO	PLL5_OUT2n		E14	
B10	VREF0B3	IO	PLL5_OUT3p		B13	
B10	VREF0B3	IO	PLL5_OUT3n		A13	
B3	VREF0B3	nSTATUS		nSTATUS	K14	
B3	VREF0B3	nCONFIG		nCONFIG	L14	
B3	VREF0B3	DCLK		DCLK	K13	
B3	VREF0B3	CONF_DONE		CONF_DONE	K15	
B3	VREF0B3	CLK14p			B14	
B3	VREF0B3	IO	CLK14n		A14	
B3	VREF0B3	CLK15p			D14	
B3	VREF0B3	IO	CLK15n		C14	
B3	VREF0B3	VREF0B3			J16	
B3	VREF0B3	IO		DATA4	L15	
B3	VREF0B3	IO		DATA5	M15	
B3	VREF0B3	IO		DATA6	K16	
B3	VREF0B3	IO	RUP3		L16	
B3	VREF0B3	IO	RDN3		M16	
B3	VREF0B3	IO	DQ6T0		E16	DQ1T0
B3	VREF0B3	IO	DQ6T1		B15	DQ1T1
B3	VREF0B3	IO		DATA7	G17	
B3	VREF0B3	IO	DQ6T2		E15	DQ1T2
B3	VREF0B3	IO	DQS6T		D15	
B3	VREF0B3	IO	DQ6T3		C16	DQ1T3
B3	VREF0B3	IO		CLKUSR	F17	
B3		GND				
		GND			H17	
B3	VREF0B3	IO	FCLK0		F18	
B3	VREF0B3	IO	FCLK1		G18	
B3	VREF0B3	IO	DQ6T4		D16	DQ1T4
B3	VREF0B3	IO	DQ6T5		F15	DQ1T5
B3	VREF0B3	IO	DQ6T6		C15	DQ1T6
B3	VREF0B3	IO	DQ6T7		B16	DQ1T7
B3	VREF1B3	IO	DQ7T0		E17	DQ1T8
B3	VREF1B3	IO	DQ7T1		B17	DQ1T9
B3	VREF1B3	IO	DQ7T2		A17	DQ1T10
B3	VREF1B3	IO	DQS7T		C17	DQS1T
B3	VREF1B3	IO	DQ7T3		D17	DQ1T11
B3	VREF1B3	IO	DQ7T4		C18	DQ1T12
B3	VREF1B3	IO	DQ7T5		B18	DQ1T13





## Pin Information For The Stratix™ GX EP1SGX10D Device, ver 1.7

Bank Number	VREF Bank	Pin Name/Function	Optionn Function(s)	Configuration Function	F672	DQS for x32
B3	VREF1B3	IO	DQ8T0		C19	DQ1T16
B3	VREF1B3	IO	DQ7T6		D18	DQ1T14
B3	VREF1B3	IO	DQ8T1		D19	DQ1T17
B3	VREF1B3	IO	DQ7T7		E18	DQ1T15
B3	VREF1B3	IO	DQ8T2		A18	DQ1T18
B3	VREF1B3	IO	DQS8T		B19	
B3	VREF1B3	IO	DQ8T3		B20	DQ1T19
B3	VREF1B3	IO	DQ8T4		A20	DQ1T20
B3	VREF1B3	IO	DQ8T5		A19	DQ1T21
B3	VREF1B3	IO	DQ8T6		C20	DQ1T22
B3	VREF1B3	IO	DQ8T7		D20	DQ1T23
B3	VREF1B3	VREF1B3			J17	
B3	VREF1B3	IO			G16	
B3	VREF1B3	IO			H18	
B3	VREF1B3	IO	DQ9T0		A21	DQ1T24
B3	VREF1B3	IO	DQ9T1		B21	DQ1T25
B3	VREF1B3	IO	DQ9T2		C21	DQ1T26
B3	VREF1B3	IO	DQS9T		B22	
B3	VREF1B3	IO	DQ9T3		C22	DQ1T27
B3	VREF1B3	IO	DQ9T4		A22	DQ1T28
B3	VREF1B3	IO	DQ9T5		B23	DQ1T29
B3	VREF1B3	IO	DQ9T6		A23	DQ1T30
B3	VREF1B3	IO	DQ9T7		B24	DQ1T31
B3	VREF1B3	IO			H16	
		GXB_GND				
		GND				
		VCCIO2			C26	
		VCCIO2			M26	
		VCCIO2			N18	
		VCCIO1			AD26	
		VCCIO1			P18	
		VCCIO1			R26	
		VCCIO8			AF15	
		VCCIO8			AF24	
		VCCIO8			T14	
		VCCIO7			AF3	
		VCCIO7			AF12	
		VCCIO7			T12	
		VCCIO4			A3	
		VCCIO4			A12	
		VCCIO4			L12	
		VCCIO3			A15	
		VCCIO3			A24	
		VCCIO3			L13	
		VCCP_B14			L8	
		VCCP_B14			M8	
		VCCP_B15			R8	
		VCCP_B15			T8	
		VCCR_B14			L7	
		VCCR_B14			M7	
		VCCR_B15			R7	



## Pin Information For The Stratix™ GX EP1SGX10D Device, ver 1.7

Bank Number	VREF Bank	Pin Name/Function	Optionn Function(s)	Configuration Function	F672	DQS for x32
		VCCR_B15			T7	
		VCCT_B14			L6	
		VCCT_B14			M6	
		VCCT_B15			R6	
		VCCT_B15			T6	
		VCCINT			AB6	
		VCCINT			N9	
		VCCINT			Y6	
		VCCINT			F6	
		VCCINT			N11	
		VCCINT			H6	
		VCCINT			N13	
		VCCINT			L11	
		VCCINT			P12	
		VCCINT			L9	
		VCCINT			N16	
		VCCINT			M10	
		VCCINT			P16	
		VCCINT			K6	
		VCCINT			N15	
		VCCINT			M9	
		VCCINT			P14	
		VCCINT			L10	
		VCCINT			P10	
		VCCINT			M14	
		VCCINT			V6	
		GXB_GND			AA3	
		GXB_GND			D2	
		GXB_GND			H4	
		GXB_GND			M3	
		GXB_GND			T2	
		GXB_GND			Y1	
		GXB_GND			AB2	
		GXB_GND			F1	
		GXB_GND			J3	
		GXB_GND			M5	
		GXB_GND			T4	
		GXB_GND			Y3	
		GXB_GND			AB4	
		GXB_GND			F3	
		GXB_GND			K2	
		GXB_GND			P1	
		GXB_GND			U3	
		GXB_GND			Y5	
		GXB_GND			AD1	
		GXB_GND			F5	
		GXB_GND			K4	
		GXB_GND			P3	
		GXB_GND			V2	
		GXB_GND			D1	
		GXB_GND			H1	



## Pin Information For The Stratix™ GX EP1SGX10D Device, ver 1.7

Bank Number	VREF Bank	Pin Name/Function	Optionn Function(s)	Configuration Function	F672	DQS for x32
		GXB_GND			L3	
		GXB_GND			P5	
		GXB_GND			V4	
		GXB_GND			H3	
		GXB_GND			M2	
		GXB_GND			T1	
		GXB_GND			W3	
		GXB_GND			AB1	
		GXB_GND			E3	
		GXB_GND			H5	
		GXB_GND			M4	
		GXB_GND			T3	
		GXB_GND			Y2	
		GXB_GND			AB3	
		GXB_GND			F2	
		GXB_GND			K1	
		GXB_GND			N3	
		GXB_GND			T5	
		GXB_GND			Y4	
		GXB_GND			AB5	
		GXB_GND			F4	
		GXB_GND			K3	
		GXB_GND			P2	
		GXB_GND			V1	
		GXB_GND			AD2	
		GXB_GND			G3	
		GXB_GND			K5	
		GXB_GND			P4	
		GXB_GND			V3	
		GXB_GND			H2	
		GXB_GND			M1	
		GXB_GND			R3	
		GXB_GND			V5	
		GND			A2	
		GND			AF2	
		GND			L26	
		GND			P13	
		GND			AA6	
		GND			B1	
		GND			N10	
		GND			R14	
		GND			A16	
		GND			AF16	
		GND			M12	
		GND			P17	
		GND			AD3	
		GND			D3	
		GND			N14	
		GND			U6	
		GND			A11	
		GND			AF11	



## Pin Information For The Stratix™ GX EP1SGX10D Device, ver 1.7

Bank Number	VREF Bank	Pin Name/Function	Optionn Function(s)	Configuration Function	F672	DQS for x32
		GND			M11	
		GND			P15	
		GND			AC3	
		GND			B26	
		GND			N12	
		GND			T26	
		GND			A25	
		GND			AF25	
		GND			M13	
		GND			R12	
		GND			AE1	
		GND			G6	
		GND			N17	
		GND			W6	
		GND			AE26	
		GND			J6	
		GND			P11	
		NC			AA9	
		NC			AA25	
		NC			AB22	
		NC			AC20	
		NC			AD11	
		NC			B11	
		NC			D21	
		NC			E21	
		NC			F21	
		NC			G22	
		NC			J18	
		NC			Y13	
		NC			AA15	
		NC			AB10	
		NC			AB24	
		NC			AC22	
		NC			AD24	
		NC			C10	
		NC			D23	
		NC			E23	
		NC			F23	
		NC			G24	
		NC			T17	
		NC			Y19	
		NC			AA20	
		NC			AB15	
		NC			AB26	
		NC			AC24	
		NC			AE23	
		NC			C23	
		NC			D25	
		NC			E25	
		NC			G14	
		NC			H15	



## Pin Information For The Stratix™ GX EP1SGX10D Device, ver 1.7

Bank Number	VREF Bank	Pin Name/Function	Optionn Function(s)	Configuration Function	F672	DQS for x32
		NC			V15	
		NC			Y21	
		NC			AA22	
		NC			AB20	
		NC			AC11	
		NC			AC26	
		NC			AE25	
		NC			C25	
		NC			E9	
		NC			F16	
		NC			G19	
		NC			H22	
		NC			W14	
		NC			AA10	
		NC			AA26	
		NC			AB23	
		NC			AC21	
		NC			AD23	
		NC			B25	
		NC			D22	
		NC			E22	
		NC			F22	
		NC			G23	
		NC			K11	
		NC			Y14	
		NC			AA19	
		NC			AB11	
		NC			AB25	
		NC			AC23	
		NC			AD25	
		NC			C11	
		NC			D24	
		NC			E24	
		NC			F24	
		NC			H14	
		NC			V9	
		NC			Y20	
		NC			AA21	
		NC			AB19	
		NC			AC10	
		NC			AC25	
		NC			AE24	
		NC			C24	
		NC			D26	
		NC			E26	
		NC			G15	
		NC			H21	
		NC			W13	
		NC			Y22	
		NC			AA23	
		NC			AB21	



## Pin Information For The Stratix™ GX EP1SGX10D Device, ver 1.7

Bank Number	VREF Bank	Pin Name/Function	Optionn Function(s)	Configuration Function	F672	DQS for x32
		NC			AC19	
		NC			AD10	
		NC			B10	
		NC			D10	
		NC			E19	
		NC			F19	
		NC			G20	
		NC			J14	
		NC			W21	
		NC			AA24	
		NC			D11	
		NC			E20	
		NC			F20	
		NC			G21	
		NC			J15	
		NC			W22	



## Pin Definitions For The Stratix™ GX EP1SGX Device, ver 1.7

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
<b>Supply and Reference Pins</b>		
VREF[1..4]B[1..4,7,8]	Input	Input reference voltage for banks. If a bank is used for a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank. If VREF pins are not used, they should be connected to Gnd.
VCCIO[1..4]B[1..4,7,8]	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O standards. VCCIO also supplies power to the input buffers used for the LVTTTL, LVCMOS, 1.5-V, 1.8-V, 2.5-V, 3.3-V PCI, and 3.3-V PCI-X I/O standards.
VCCINT	Power	These power pins are supplied with a 1.5V source. These are internal logic array voltage supply pins. VCCINT also supplies power to the input buffers used for the LVDS, LVPECL, 3.3-V PCML, HyperTransport™ technology, differential HSTL, GTL, GTL+, HSTL, SSTL, CTT, and 3.3-V AGP I/O standards.
VCC_PLL5_OUTA	Power	External clock output buffer power for PLL5 clock outputs PLL5_OUT[1..0]. The designer must connect this pin to the VCCIO of bank 9.
VCC_PLL5_OUTB	Power	External clock output buffer power for PLL5 clock outputs PLL5_OUT[3..2]. The designer must connect this pin to the VCCIO of bank 10.
VCC_PLL6_OUTA	Power	External clock output buffer power for PLL6 clock outputs PLL6_OUT[1..0]. The designer must connect this pin to the VCCIO of bank 11.
VCC_PLL6_OUTB	Power	External clock output buffer power for PLL6 clock outputs PLL6_OUT[3..2]. The designer must connect this pin to the VCCIO of bank 12.
VCCA_PLL[1,2,5,...,8,11,12]	Power	Analog power for PLLs[1,2,5,...,8,11,12]. The designer must connect this pin to 1.5 V, even if the PLL is not used.
GND_A_PLL[1,2,5,...,8,11,12]	Ground	Analog ground for PLLs[1,2,5,...,8,11,12]. The designer can connect this pin to the GND plane on the board.
VCCG_PLL[1,2,5,...,8,11,12]	Power	Guard ring power for PLLs[1,2,5,...,8,11,12]. The designer must connect this pin to 1.5 V, even if the PLL is not used.
GNDG_PLL[1,2,5,...,8,11,12]	Ground	Guard ring ground for PLLs[1,2,5,...,8,11,12]. The designer can connect this pin to the GND plane on the board.
GXB_GND	Ground	Transceiver Power Ground. These ground pins need to be connected to a ground island plane isolated from noisy digital ground.
GND	Ground	These ground pins need to be connected to digital ground. The digital ground is used for VCCINT and VCCIO return current.
NC	No Connect	These pins should be left unconnected.
<b>Dedicated &amp; Configuration/JTAG Pins</b>		
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration status pin; it is not available as a user I/O pin.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin; it is not available as a user I/O pin.
nCONFIG	Input	Dedicated configuration control input. A low transition resets the target device; a low-to-high transition begins configuration. All I/O pins tri-state when nCONFIG is driven low.
DCLK	Input	Clock input used to clock configuration data from an external source into the Stratix device. This is a dedicated pin used for configuration.
nIO_PULLUP	Input	IF nIO_PULLUP is driven high during configuration, the weak pull-ups on all user I/O pins are disabled. If driven low, the weak pull-ups are enabled during configuration. nIO_PULLUP can be pulled up to either 1.5, 1.8, 2.5, or 3.3 V.
PORSEL	Input	Dedicated input pin used to select POR delay times of 2 ms or 100 ms during powerup. When PORSEL is connected to ground, the POR time is 100 ms. When PORSEL is connected to 3.3 V, the POR time is 2 ms.
VCCSEL	Input	VCCSEL is used to select which input buffer is used on all configuration pins. VCCSEL will control whether the 3.3-/2.5-V input buffer or the 1.8-/1.5-V input buffer is used. A "0" means 3.3/2.5 V and a "1" means 1.8-/1.5 V. At powerup, VCCSEL accepts 3.3
nCE	Input	Active-low chip enables. Dedicated chip enable input used to detect which device is active in a chain of devices. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCEO	Output	Output that drives low when device configuration is complete. During multi-device configuration, this pin feeds a subsequent device's nCE pin.
TMS	Input	This is a dedicated JTAG input pin.
TDI	Input	This is a dedicated JTAG input pin.
TCK	Input	This is a dedicated JTAG input pin.
TDO	Output	This is a dedicated JTAG input pin.
TRST	Input	This is a dedicated JTAG input pin. Active low input, used to asynchronously reset the JTAG boundary scan circuit.
MSEL[2..0]	Input	Dedicated mode select control pins that set the configuration mode for the device.



## Pin Definitions For The Stratix™ GX EP1SGX Device, ver 1.7

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
TEMPDIODEp	Input	Pin used in conjunction with the temperature sensing diode (bias-high input) inside the Stratix device. If the temperature sensing diode is not used then connect this pin to GND.
TEMPDIODEn	Input	Pin used in conjunction with the temperature sensing diode (bias-low input) inside the Stratix device. If the temperature sensing diode is not used then connect this pin to GND.
<b>Clock and PLL Pins</b>		
PLL_ENA	Input	Dedicated input pin that drives the optional pllana port of all or a set of PLLs. If a PLL uses the pllana port, drive the PLL_ENA pin low to reset all PLLs including the counters to their default state. If VCCSEL = 0, then you must drive the PLL_ENA with a 3.3/2.5 V signal to enable the PLLs. If VCCSEL = 1, connect PLL_ENA to 1.8/1.5 V to enable the PLLs.
FCLK[7..0]	Bidirectional	Dedicated fast regional clock pins. FCLK pins can also be used as input, output, or bidirectional pins.
CLK[15..12]p	Input	Dedicated global clock inputs 12 to 15.
CLK[15..12]n	I/O, Input	Negative terminal input for differential global clock input. May also be used as regular I/O
CLK[7..0]p	Input	Dedicated global clock inputs 0 to 7.
CLK[7, 6, 5, 4, 3, 1]n	I/O, Input	Negative terminal input for differential global clock input. Or may be used as a regular I/O pin.
CLK[2, 0]n	Input	Dedicated negative terminal input for differential global clock input.
PLL6_OUT[3..0]p	I/O, Output	External clock outputs [3..0] from enhanced PLL 6. These pins can be differential (four output pin pairs) or single ended (eight clock outputs from PLL6). May also be used as regular I/O
PLL6_OUT[3..0]n	I/O, Output	Negative terminal for external clock outputs [3..0] from PLL6. If the clock outputs are single ended, then each pair of pins (i.e., PLL6_OUT0p and PLL6_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase. May also be used as regular I/O
PLL5_OUT[3..0]p	I/O, Output	External clock outputs [3..0] from enhanced PLL 5. These pins can be differential (four output pin pairs) or single ended (eight clock outputs from PLL5). May also be used as regular I/O
PLL5_OUT[3..0]n	I/O, Output	Negative terminal for external clock outputs [3..0] from PLL 5. If the clock outputs are single ended, then each pair of pins (i.e., PLL5_OUT0p and PLL5_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase. May also be used as regular I/O
<b>Optional/Dual-Purpose Pins</b>		
DIFFIO_RX[44..0]p	Input	High speed source synchronous differential I/O receiver channels 0 to 44. Pins with an p suffix carry the positive signal for the differential channel. If not used, these pins are dedicated input pins.
DIFFIO_RX[44..0]n	Input	This pin is the complementary signal of the differential inputs. If not used for the differential pair, these pins are dedicated input pins. Pins with an n suffix carry the negative signal for the differential channel.
DIFFIO_TX[44..0]p	I/O, Output	Dual-purpose source synchronous high speed differential I/O transmitter channels 0 to 44. Pins with an p suffix carry the positive signal for the differential channel. If not used, these pins are regular I/O pins.
DIFFIO_TX[44..0]n	I/O, Output	This pin is the complementary signal of the differential inputs and outputs. If not used for the differential pair, these pins are regular I/O pins. Pins with an n suffix carry the negative signal for the differential channel.
PLL5_FBp	I/O, Input	External feedback input pin for PLL5. This pin can be used as a user I/O pin if external feedback mode is not used.
PLL5_FBn	I/O, Input	Negative terminal input for external feedback input PLL5_FBp
PLL6_FBp	I/O, Input	External feedback input pin for PLL6
PLL6_FBn	I/O, Input	Negative terminal input for external feedback input PLL6_FBp
INIT_DONE	I/O, Output	the pin indicates when the device has entered user mode. This pin can be used as a user I/O pin after configuration.
DATA[7..0]	I/O, Input	Dual-purpose configuration input data pins. These pins can be used for configuration or as regular I/O pins. These pins can also be used as user I/O pins after configuration.
nRS	I/O, Input	Read strobe input pin. This pin can be used as a user I/O pin after configuration.
DEV_CLRn	I/O, Input	Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as defined in the users design.
DEV_OE	I/O, Input	Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. This pin can be used as a user I/O pin after configuration.
RDYnBSY	I/O, Output	Ready not busy output. A high output indicates that the target device is ready to accept another data byte. A low output indicates that the target device is not ready to receive another data byte. This pin can be used as a user I/O pin after configuration





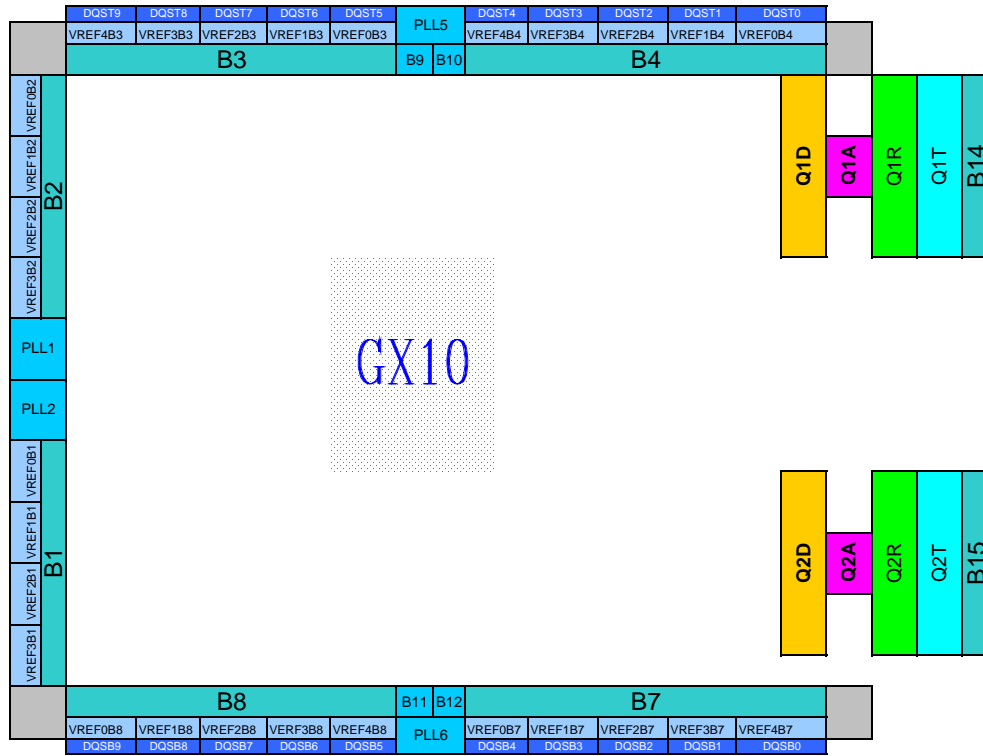
## Pin Definitions For The Stratix™ GX EP1SGX Device, ver 1.7

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
nCS,CS	I/O, Input	These are chip-select inputs that enable the Stratix device in the passive parallel asynchronous configuration mode. Drive nCS low and CS high to target a device for configuration. If a design requires an active high enable, use the CS pin and drive the nCS pin low.
nWS	I/O, Input	Active-low write strobe input to latch a byte of data on the DATA pins. This pin can be used as a user I/O pin after configuration.
PGM[2..0]	I/O, Output	These output pins control one of eight pages in the EPC16 configuration device when using remote update or local update configuration modes. When not using remote update or local update configuration modes, these pins are user I/O pins.
RUP[8..7],RUP[4..1]	I/O, Input	Reference pins for banks 8,7,4,3,2,1 The external precision resistors R <sub>UP</sub> must be connected to the designated RUP pin on that I/O bank. If not required, these pins are regular I/O pins.
RDN[8..7],RDN[4..1]	I/O, Input	Reference pins for banks 8,7,4,3,2,1. The external precision resistors R <sub>DN</sub> must be connected to the designated RDN pin on that I/O bank. If not required, these pins are regular I/O pins.
RUnLU	I/O, Input	Pin Definitions Input control pin to select remote update or local update modes. If MSEL2 = 1, this is a input control pin to select remote update (RUnLU =1) or local update (RUnLU =0) modes. If MSEL2 = 0, the RUnLU pin is a user I/O pin.
<b>GX ( I/O banks 13 to 17 ) Pins</b>		
VCCP_B[17..13]	VCC	GX bank [17..13] digital power. This power is connected to 1.5V.
VCCR_B[17..13]	VCC	GX bank [17..13] receiver power. This power is connected to 1.5V.
VCCT_B[17..13]	VCC	GX bank [17..13] transmitter power. This power is connected to 1.5V.
VCCG_B[17..13]	VCC	GX bank[17..13] guard ring power. This power is connected to 1.5V.
VCCA_B[17..13]	VCC	GX bank [17..13] analog power. This power is connected to 3.3V.
GXB_RX[19..0]n	I, Input	High speed differential I/O receiver channels negative. Connect any of these unused pins to ground through a 10K ohm resistor.
GXB_RX[19..0]p	I, Input	High speed differential I/O receiver channels positive. Connect any of these unused pins to 1.5V through a 10K ohm resistor.
GXB_TX[19..0]n	O,Output	High speed differential I/O transmitter channels negative. Connect any of these unused pins to ground through a 10K ohm resistor.
GXB_TX[19..0]p	O,Output	High speed differential I/O transmitter channels positive. Connect any of these unused pins to 1.5V through a 10K ohm resistor.
REFCLKB[17..13]n	I, Input	High speed differential I/O reference clock negative. Connect any of these unused pins to ground through a 10K ohm resistor.
REFCLKB[17..13]p	I, Input	High speed differential I/O reference clock positive. Connect any of these unused pins to 1.5V through a 10K ohm resistor.
RREFB[17..13]	I, Input	Reference resistor for Gx side banks. Should be connected to a 2K of a tolerance of 1% to ground. In the PCB layout the trace from this pin to the resistor needs to be routed so that it avoids any aggressor signals.
RREFB[15,14]A	I, Input	Reference resistor for Gx side banks. Should be connected to a 2K of a tolerance of 1% to ground. In the PCB layout the trace from this pin to the resistor needs to be routed so that it avoids any aggressor signals.

**Notes:**

- 1.This is a top view of the silicon die.
- 2.This is a pictorial representation only to get an idea of placement on the device. Refer to the pin-list and the Quartus II for exact locations.

**PLL Numbering, PowerBank & Vref Arrangement**



Device Name	GX Bank # Utilized
EP1SGX10C	15
EP1SGX10D	14 & 15

## Power

Power Description	Flip Chip		Notes
	Global Power on Die	Pkg route	
<b>Left, Top, and Bottom Power and Ground are the same as Stratix Devices</b>			
EPLL clock output power	VCC_CLKOUT[0:7]	isolated	
EPLL clock output power			
EPLL clock output ground	VSSN	VSSN plane	VSSN
EPLL clock output ground	VCCN[4,7]	VCCN[4,7]plane	
EPLL clock output ground	VSSN	VSSN plane	
PLL analog power	VCCA[1:2, 5:8, 11:12]	isolated	VCCA[3:4,9:10]
PLL analog ground	VSSA[1:2, 5:8, 11:12]	isolated	VSSA[3:4,9:10]
PLL digital power	VCC[1:2, 5:8, 11:12]	VCC plane	It is shorted to VCC in the package of the flip chip.
PLL digital ground	VSS[1:2, 5:8, 11:12]	VSS plane	It is shorted to VSS in the package of the flip chip.
PLL guard ring power	VCCG[1:2, 5:8, 11:12]	isolated	
PLL guard ring ground	VSSG[1:2, 5:8, 11:12]	isolated	
Noisy power	VCCN[1:4,7:8]	VCCN[1:4,7:8] plane	
Noisy ground	VSSN	VSS plane	
Quiet power	VCC	VCC plane	
Quiet ground	VSS	VSS plane	
<b>HSSI Global Power: Power and Ground are grouped in QUAD. Quad Order is 0,1,4,2,3</b>			
<b>Marketing</b>			
HSSI digital power (1.5 v )	VCCP0		Each Quad has 5 bumps connected to 2 isolated digital power balls
	VCCP1		
	VCCP4		
	VCCP2		
	VCCP3		
HSSI RX power (1.5 v )	VCCR[0:3]		Each Quad has 4 bumps connected to 1 isolated RX power ball
	VCCR[4:7]		
	VCCR[16:19]		
	VCCR[8:11]		
	VCCR[12:15]		
HSSI TX power (1.5 v )	VCCT[0:3]		Each Quad has 4 bumps connected to 1 isolated TX power ball
	VCCT[4:7]		
	VCCT[16:19]		
	VCCT[8:11]		
	VCCT[12:15]		
HSSI CMU power (1.5 v )	VCCM0		VCCM# bump shares power with VCCT# of the same QUAD There are no pin associated with this pin name since they share the same bump power with VCCT# of the same Quad
	VCCM1		
	VCCM4		
	VCCM2		
	VCCM3		
HSSI Analog power (3.3 v )	VCCAQ0		Each Quad has its own analog power. One bump--> one ball Provides power to Tx PLL and some biasing circuit
	VCCAQ1		
	VCCAQ4		
	VCCAQ2		
	VCCAQ3		
HSSI VCCG (1.5 v )	VCCGQ0		Each Quad has its own VCCG power. One bump--> one ball Guard ring for TX PLL should be used to isolate noise to TX pll
	VCCGQ1		
	VCCGQ4		
	VCCGQ2		
	VCCGQ3		
HSSI substrate ground	VSSASUB0		Each Quad has its own substrate ground. One bump--> one ball
	VSSASUB1		
	VSSASUB4		
	VSSASUB2		
	VSSASUB3		
HSSI digital ground	DGND		All digital grounds are connected to the HSSI ground plane at package level
	DGND		
	DGND		
	DGND		
	DGND		
HSSI TX/RX ground	HGND		All TX/RX grounds are connected to the HSSI ground plane at package level
	HGND		
	HGND		
	HGND		
	HGND		
HSSI CMU ground	CGND		All CMU grounds are connected to the HSSI ground plane at package level

	CGND		
	CGND		
	CGND		
	CGND		
<b>Global Power on Die</b> is the signal name that the schematics and layout use for this power or ground			
<b>Pkg Route:</b> 1) plane = indicates the power plane the bump/pad routes to in the pkg;			
2) isolated = indicates the bump/pad is routed to the pkg ball without connect to any other pkg route or plane.			
<b>Plane:</b> A plane has multiple bump/pads connected to it which in turn connect to multiple balls. It does not necessarily imply a complete sheet of conductor; it may look be more like Swiss cheese.			
<b>Net:</b> Multiple bumps/balls can share the same net bus			

Non-Migratable IO Pins						
		Non-Migratable IO Pins				
		1020FBGA ( EP1SGX40 <--> EP1SGX25 )	672FBGA ( EP1SGX25 <-->EP1SGX10)			
		AA23				
		AB23				
		AC23				
		AD23				
		AG25				
		AG26				
		AH27				
		AH28				
		AH29				
		AH30				
		AJ29				
		AJ30				
		D29				
		D30				
		E29				
		E30				
		F27				
		F28				
		F29				
		F30				
		J23				
		K23				
		L23				
		M23				

Device Part Numbers		Number of Fast PLL	Device Pin Count	# of Receiver Chs	# of Transmitter Chs	Speed (Mbps)
EP1SGX10C	2	672	22	22	1000	
EP1SGX10D	2	672	22	22	1000	
EP1SGX25C	2	672	39	39	1000	
EP1SGX25D	2	672 / 1020	39	39	1000	
EP1SGX25F	2	1020	39	39	1000	
EP1SGX40D	4	1020	45	45	1000	
EP1SGX40G	4	1020	45	45	1000	
Receiver channels operate at 1,000 Mbps with DPA. Without DPA, the receiver channels operate at 840 Mbps						
Device Part Numbers		I/O Count <sup>(1)</sup>				
Name	672-Pin FineLine BGA	1,020 Pin FineLine BGA				
EP1SGX10C	330					
EP1SGX10D	330					
EP1SGX25C	426					
EP1SGX25D	426	542				
EP1SGX25F		542				
EP1SGX40D		548				
EP1SGX40G		548				
Note 1 : The total number of I/O pins for each package described above include dedicated clock pins, and dedicated fast I/O pins. However it does not include High-Speed or the Clock Reference pins for High Speed I/O.						

What	Comment	Date
Added voltage value to power pins	rev 1.2	10/15/2002
Added information to the VCCM , they share the same bump with VCCT.	rev 1.3	12/17/2002
Added Non-Migrateble pins	rev 1.3	12/17/2002
Added I/O pin count	rev 1.3	12/17/200
Added info regarding RREF pin	rev 1.3	1/10/2003
Sent to Product Marketing	rev 1.3	2/19/2003
Connected NC pins to RREF pins( NOTE 1)	rev 1.4	5/30/2003
Connected NC pins to VCCx_Bxx ( NOTE 1 )	rev 1.4	5/30/2003
Connected unused NC pins on the HSSI side to GND. These pins are listed as NC/GND in this document and are listed as GND* in Quartus II software ( NOTE 1 and 2 )	rev 1.4	5/30/2003
Added pin status change information from rev 1.3 to rev 1.4. Pin changes are for EP1SGX10C, EP1SGX25C,EP1SGX25D,EP1SGX40 D only.	rev 1.4	5/30/2003
Added section for 1SGX25C missing from 1.4. Changed DATA0 to be an IO after configuration.	rev 1.42	7/30/2003
Note 1: Modifications in Rev 1.4 are recommendations for noise reduction. Do NOT make modifications to the board already laid out based on pin table Rev 1.3 . It is recommended that the pin table Rev 1.4 be implemented for new designs or re-designed boards only.		
NOTE 2 : GND/NC is shown as GND* in Quartus II software		
Add HSSI_GND to the pin list	rev 1.43	9/10/2003
Wrong Bank was referenced in the GX25C device	rev 1.44	9/11/2003
Update non-migration table	rev 1.45	9/17/2003
change all references of GX_TX, GX_RX to GXB_TX, GXB_RX		
Change all references of HSSI_GND to GXB_GND		
Change pin description data[7..1] to include data0		
Changed false references of RUP/RDN to different banks		
Updated pin description so only CLK0n and CLK2n were dedicated clock inputs. While the rest were also I/Os		
Updated pin description of VCCINT to explicitly say it needs a 1.5V supply		
Updated the pin description for PLENA		
Update pin description to explain what to do with unused pins for the transceivers and REFCLKB.	rev 1.46	9/19/2003
Definition for RUnLU needed to be updated to correctly indicate poarity of signal for remote and local update. Also the pin definitions for GND and NC were added to the pin definition.	rev 1.47	10/21/2003
Updated pin descriptions for items 74 though 78 of the pin descriptions. These describe the VCC voltages and the pin description was updated with more specific information as to what voltage to connect them to.		
Item 42 in the pin desription was updated to specify that the CLK[15..12]p pins are dedicated input clock pins		
Item 43 in the pin desription was updated to specify that the CLK[15..12]n pins are either clock inputs or regular I/O	rev 1.48	12/11/2003
Item 47 through 50 which describe the PLL_OUT pins are updated to specify that they can be used as either I/O or Output		
Items 80 through 83 was updated to describe the termination of the unused pins for GX_RX and GX_TX.		

Items 85 and 86 was updated to describe the termination of the unused pins for REFCLK.		
Updated description for unused VREF pins so the it reads the same description as Quartus II	rev 1.49	3/17/2004
Updated description for RREFB. Layout guidelines were added.	rev 1.50	6/2/2004
Updated RREFB pins to address new Quartus change (please refer to the "RREFB pin change in 1.6" worksheet)		
Deleted DQS for x16 column in EP1SGX10C & EP1SGX10D pin-list	rev 1.60	4/27/2005
Created pin definition for RREFB[15,14]A		
Added CRC_ERROR pins in pin list	rev 1.70	2/22/2006



RREFB pin change in 1.6	Device	Status in Rev 1.5	Pin name	Status in Rev 1.6
	EP1SGX10CF672	RREFB15	U7	RREFB15A
		RREFB15	K7	RREFB15
	EP1SGX25CF672	RREFB15	U7	RREFB15
		RREFB15	K7	RREFB15A
	EP1SGX25DF1020	RREFB14	L7	RREFB14
		RREFB14	J7	RREFB14A
		RREFB15	AC7	RREFB15A
		RREFB15	T8	RREFB15
	EP1SGX40DF1020	RREFB14	J7	RREFB13
		RREFB15	AC7	RREFB16
		RREFB15	T7	GND/NC
		RREFB15	T8	RREFB15
		RREFB14	L7	RREFB14