Pin Information For The Stratix™ EP1S20 Device, ver 3.6 (Note 2)

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F484	B672	F672	F780	DQS for x16	DQS for x32	DIFFIO Speed (1)
B2	VREF0B2	IO	DIFFIO_RX32p			C1	C1	C27			HIGH
B2	VREF0B2	IO	DIFFIO_RX32n		F18	D2	D2	C28			HIGH
B2	VREF0B2	IO	DIFFIO_TX32p		E19	E3	E3	G23			HIGH
B2	VREF0B2	IO	DIFFIO_TX32n		E20	E4	E4	G24			HIGH
B2	VREF0B2	IO	DIFFIO_RX31p			E1	E1	D27			HIGH
B2	VREF0B2	IO	DIFFIO_RX31n			E2	E2	D28			HIGH
B2	VREF0B2	IO	DIFFIO_TX31p			F3	F3	H24			HIGH
B2	VREF0B2	IO	DIFFIO_TX31n		G18	F4	F4	H23			HIGH
B2	VREF0B2	IO	DIFFIO_RX30p			F1	F1	E27			HIGH
B2	VREF0B2	IO	DIFFIO_RX30n			F2	F2	E28			HIGH
B2	VREF0B2	IO	DIFFIO_TX30p			G5	G5	H22			HIGH
B2	VREF0B2	IO	DIFFIO_TX30n		H17	G6	G6	H21			HIGH
B2	VREF0B2	IO	DIFFIO_RX29p			G1	G1	F25			HIGH
B2	VREF0B2	IO	DIFFIO_RX29n			G2	G2	F26			HIGH
B2	VREF0B2	IO	DIFFIO_TX29p			G3	G3	J24			HIGH
B2	VREF0B2	IO	DIFFIO_TX29n		J17	G4	G4	J23			HIGH
B2	VREF0B2	VREF0B2			H18	H8	H8	E24			
B2	VREF0B2	IO	DIFFIO_RX28p			H1	H1	F27			HIGH
B2	VREF0B2	IO	DIFFIO_RX28n			H2	H2	F28			HIGH
B2	VREF0B2	IO	DIFFIO_TX28p			H3	H3	K23			HIGH
B2	VREF0B2	IO	DIFFIO_TX28n		J19	H4	H4	K24			HIGH
B2	VREF0B2	IO	DIFFIO_RX27p					G26			HIGH
B2	VREF0B2	IO	DIFFIO_RX27n					G25			HIGH
B2	VREF0B2	IO	DIFFIO_TX27p		F19	H6	H6	J21			HIGH
B2	VREF0B2	IO	DIFFIO_TX27n		F20	H5	H5	J22			HIGH
B2	VREF0B2	IO	DIFFIO_RX26p		D22	J4	J4	G27			HIGH
B2	VREF0B2	IO	DIFFIO_RX26n		D21	J3	J3	G28			HIGH
B2	VREF0B2	IO	DIFFIO_TX26p					K21			HIGH
B2	VREF0B2	IO	DIFFIO_TX26n					K22			HIGH
B2	VREF0B2	IO	DIFFIO_RX25p/RUP2		E21	K4	K4	H26			HIGH
B2	VREF0B2	IO	DIFFIO_RX25n/RDN2		E22	K3	K3	H25			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F484	B672	F672	F780	DQS for x16	DQS for x32	DIFFIO Speed (1)
B2	VREF0B2	IO	DIFFIO_TX25p					L22			HIGH
B2	VREF0B2	IO	DIFFIO_TX25n					L21			HIGH
B2	VREF0B2	IO	DIFFIO_RX24p					H27			HIGH
B2	VREF0B2	IO	DIFFIO_RX24n					H28			HIGH
B2	VREF0B2	IO	DIFFIO_TX24p					L23			HIGH
B2	VREF0B2	IO	DIFFIO_TX24n					L24			HIGH
B2	VREF1B2	IO	DIFFIO_RX23p			K2	K2	J25			HIGH
B2	VREF1B2	IO	DIFFIO_RX23n			K1	K1	J26			HIGH
B2	VREF1B2	IO	DIFFIO_TX23p		G19	K9	K9	L20			HIGH
B2	VREF1B2	IO	DIFFIO_TX23n		G20	J8	J8	L19			HIGH
B2	VREF1B2	IO	DIFFIO_RX22p			K6	K6	J27			HIGH
B2	VREF1B2	IO	DIFFIO_RX22n			K5	K5	J28			HIGH
B2	VREF1B2	IO	DIFFIO_TX22p			K8	K8	M22			HIGH
B2	VREF1B2	IO	DIFFIO_TX22n		L17	K7	K7	M21			HIGH
B2	VREF1B2	IO	DIFFIO_RX21p			L3	L3	K26			HIGH
B2	VREF1B2	IO	DIFFIO_RX21n			L2	L2	K25			HIGH
B2	VREF1B2	IO	DIFFIO_TX21p			L5	L5	M24			HIGH
B2	VREF1B2	IO	DIFFIO_TX21n		K17	L4	L4	M23			HIGH
B2	VREF1B2	IO	DIFFIO_RX20p					K27			HIGH
B2	VREF1B2	IO	DIFFIO_RX20n					K28			HIGH
B2	VREF1B2	IO	DIFFIO_TX20p		H19	L7	L7	M20			HIGH
B2	VREF1B2	IO	DIFFIO_TX20n		H20	L6	L6	M19			HIGH
B2	VREF1B2	IO	DIFFIO_RX19p		F21	M6	M6	L25			HIGH
B2	VREF1B2	IO	DIFFIO_RX19n		F22	M7	M7	L26			HIGH
B2	VREF1B2	IO	DIFFIO_TX19p					N26			HIGH
B2	VREF1B2	IO	DIFFIO_TX19n					N25			HIGH
B2	VREF1B2	VREF1B2			J18	L8	L8	K20			
B2	VREF1B2	IO	DIFFIO_RX18p		G22	M4	M4	L27			HIGH
B2	VREF1B2	IO	DIFFIO_RX18n		G21	M5	M5	L28			HIGH
B2	VREF1B2	IO	DIFFIO_TX18p					N24			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F484	B672	F672	F780	DQS for x16	DQS for x32	DIFFIO Speed (1)
B2	VREF1B2	IO	DIFFIO_TX18n					N23			HIGH
B2	VREF1B2	IO	DIFFIO_RX17p		H21	N6	N6	M25			HIGH
B2	VREF1B2	IO	DIFFIO_RX17n		H22	N7	N7	M26			HIGH
B2	VREF1B2	IO	DIFFIO_TX17p		J20	M8	M8	N22			HIGH
B2	VREF1B2	IO	DIFFIO_TX17n		J21	M9	M9	N21			HIGH
B2	VREF1B2	IO	DIFFIO_RX16p					M27			HIGH
B2	VREF1B2	IO	DIFFIO_RX16n					N28			HIGH
B2	VREF1B2	IO	DIFFIO_TX16p		K20	P8	P8	N20			HIGH
B2	VREF1B2	IO	DIFFIO_TX16n		K21	N8	N8	N19			HIGH
B2	VREF1B2	CLK0n			L22	N2	N2	N27			
B2	VREF1B2	CLK0p			L21	N3	N3	P27			
B2	VREF1B2	IO	CLK1n					P26			
B2	VREF1B2	CLK1p			L20	M1	M1	P25			
		VCCA_PLL1			K19	M3	M3	P23			
		GND									
		GNDA_PLL1			L19	N5	N5	P24			
		VCCG_PLL1			K18	M2	M2	P21			
		GNDG_PLL1			L18	N4	N4	P22			
		VCCA_PLL2			M18	P5	P5	R23			
		GND									
		GNDA_PLL2			M19	P3	P3	R24			
		VCCG_PLL2			N18	P4	P4	R21			
		GNDG_PLL2			N19	P2	P2	R22			
B1	VREF0B1	CLK2p			M21	R1	R1	R27			
B1	VREF0B1	CLK2n			M22	R2	R2	T27			
B1	VREF0B1	CLK3p			M20	R3	R3	R25			
B1	VREF0B1	IO	CLK3n					R26			
B1	VREF0B1	IO	DIFFIO_RX15p					T28			HIGH
B1	VREF0B1	IO	DIFFIO_RX15n					U27			HIGH
B1	VREF0B1	IO	DIFFIO_TX15p		N21	P6	P6	T21			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F484	B672	F672	F780	DQS for x16	DQS for x32	DIFFIO Speed (1)
B1	VREF0B1	IO	DIFFIO_TX15n		N20	P7	P7	T22			HIGH
B1	VREF0B1	IO	DIFFIO_RX14p		R22	R6	R6	U26			HIGH
B1	VREF0B1	IO	DIFFIO_RX14n		R21	R7	R7	U25			HIGH
B1	VREF0B1	IO	DIFFIO_TX14p		P21	R8	R8	T19			HIGH
B1	VREF0B1	IO	DIFFIO_TX14n		P20	R9	R9	T20			HIGH
B1	VREF0B1	IO	DIFFIO_RX13p		T22	R4	R4	V27			HIGH
B1	VREF0B1	IO	DIFFIO_RX13n		T21	R5	R5	V28			HIGH
B1	VREF0B1	IO	DIFFIO_TX13p					T23			HIGH
B1	VREF0B1	IO	DIFFIO_TX13n					T24			HIGH
B1	VREF0B1	IO	DIFFIO_RX12p		U21	T3	T3	V26			HIGH
B1	VREF0B1	IO	DIFFIO_RX12n		U22	T2	T2	V25			HIGH
B1	VREF0B1	IO	DIFFIO_TX12p					T26			HIGH
B1	VREF0B1	IO	DIFFIO_TX12n					T25			HIGH
B1	VREF0B1	VREF0B1			P18	T8	T8	R19			
B1	VREF0B1	IO	DIFFIO_RX11p					W28			HIGH
B1	VREF0B1	IO	DIFFIO_RX11n					W27			HIGH
B1	VREF0B1	IO	DIFFIO_TX11p		R20	T7	T7	U19			HIGH
B1	VREF0B1	IO	DIFFIO_TX11n		R19	T6	T6	U20			HIGH
B1	VREF0B1	IO	DIFFIO_RX10p		V22	T5	T5	W26			HIGH
B1	VREF0B1	IO	DIFFIO_RX10n		V21	T4	T4	W25			HIGH
B1	VREF0B1	IO	DIFFIO_TX10p		T20	U6	U6	U24			HIGH
B1	VREF0B1	IO	DIFFIO_TX10n		T19	U5	U5	U23			HIGH
B1	VREF0B1	IO	DIFFIO_RX9p			U2	U2	Y28			HIGH
B1	VREF0B1	IO	DIFFIO_RX9n			U1	U1	Y27			HIGH
B1	VREF0B1	IO	DIFFIO_TX9p			U8	U8	U21			HIGH
B1	VREF0B1	IO	DIFFIO_TX9n		N17	U7	U7	U22			HIGH
B1	VREF0B1	IO	DIFFIO_RX8p			U4	U4	Y26			HIGH
B1	VREF0B1	IO	DIFFIO_RX8n			U3	U3	Y25			HIGH
B1	VREF0B1	IO	DIFFIO_TX8p			U9	U9	V19			HIGH
B1	VREF0B1	IO	DIFFIO_TX8n		M17	V8	V8	V20			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F484	B672	F672	F780	DQS for x16	DQS for x32	DIFFIO Speed (1)
B1	VREF1B1	IO	DIFFIO_RX7p					AA28			HIGH
B1	VREF1B1	IO	DIFFIO_RX7n					AA27			HIGH
B1	VREF1B1	IO	DIFFIO_TX7p					V24			HIGH
B1	VREF1B1	IO	DIFFIO_TX7n					V23			HIGH
B1	VREF1B1	IO	DIFFIO_RX6p/RUP1		W21	V6	V6	AA25			HIGH
B1	VREF1B1	IO	DIFFIO_RX6n/RDN1		W22	V5	V5	AA26			HIGH
B1	VREF1B1	IO	DIFFIO_TX6p					V22			HIGH
B1	VREF1B1	IO	DIFFIO_TX6n					V21			HIGH
B1	VREF1B1	IO	DIFFIO_RX5p					AB28			HIGH
B1	VREF1B1	IO	DIFFIO_RX5n					AB27			HIGH
B1	VREF1B1	IO	DIFFIO_TX5p		U20	Y3	Y3	W23			HIGH
B1	VREF1B1	IO	DIFFIO_TX5n		U19	Y4	Y4	W24			HIGH
B1	VREF1B1	IO	DIFFIO_RX4p			W3	W3	AB26			HIGH
B1	VREF1B1	IO	DIFFIO_RX4n			W4	W4	AB25			HIGH
B1	VREF1B1	IO	DIFFIO_TX4p			Y6	Y6	W21			HIGH
B1	VREF1B1	IO	DIFFIO_TX4n		P17	Y5	Y5	W22			HIGH
B1	VREF1B1	VREF1B1			R17	V7	V7	W20			
B1	VREF1B1	IO	DIFFIO_RX3p			Y2	Y2	AC28			HIGH
B1	VREF1B1	IO	DIFFIO_RX3n			Y1	Y1	AC27			HIGH
B1	VREF1B1	IO	DIFFIO_TX3p			AA6	AA6	Y21			HIGH
B1	VREF1B1	IO	DIFFIO_TX3n		P19	AA5	AA5	Y22			HIGH
B1	VREF1B1	IO	DIFFIO_RX2p			AA2	AA2	AD28			HIGH
B1	VREF1B1	IO	DIFFIO_RX2n			AA1	AA1	AD27			HIGH
B1	VREF1B1	IO	DIFFIO_TX2p			AA4	AA4	Y24			HIGH
B1	VREF1B1	IO	DIFFIO_TX2n		T18	AA3	AA3	Y23			HIGH
B1	VREF1B1	IO	DIFFIO_RX1p			AB2	AB2	AE28			HIGH
B1	VREF1B1	IO	DIFFIO_RX1n			AB1	AB1	AE27			HIGH
B1	VREF1B1	IO	DIFFIO_TX1p			AB4	AB4	AA23			HIGH
B1	VREF1B1	IO	DIFFIO_TX1n		U18	AB3	AB3	AA24			HIGH
B1	VREF1B1	IO	DIFFIO_RX0p			AC2	AC2	AF28			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F484	B672	F672	F780	DQS for x16	DQS for x32	DIFFIO Speed (1)
B1	VREF1B1	IO	DIFFIO_RX0n			AD1	AD1	AF27			HIGH
B1	VREF1B1	IO	DIFFIO_TX0p		V19	AC4	AC4	AA21			HIGH
B1	VREF1B1	IO	DIFFIO_TX0n		V20	AC3	AC3	AA22			HIGH
B8	VREF0B8	IO						AC23			
B8	VREF0B8	IO	DQ9B7		W20	AD5	AD5	AG26	DQ3B15	DQ1B31	
B8	VREF0B8	IO			N16	AB6	AB6	AB22			
B8	VREF0B8	IO	DQ9B6		W19	AD2	AD2	AH26	DQ3B14	DQ1B30	
B8	VREF0B8	IO	DQ9B5		AA21	AE2	AE2	AG25	DQ3B13	DQ1B29	
B8	VREF0B8	IO	DQ9B4		AA20	AD3	AD3	AH25	DQ3B12	DQ1B28	
B8	VREF0B8	IO						AE25			
B8	VREF0B8	IO	DQ9B3		Y21	AE4	AE4	AF25	DQ3B11	DQ1B27	
B8	VREF0B8	IO	DQS9B		Y20	AD4	AD4	AF24			
B8	VREF0B8	IO	DQ9B2		Y19	AE3	AE3	AG24	DQ3B10	DQ1B26	
B8	VREF0B8	IO	DQ9B1		AA19	AB5	AB5	AE24	DQ3B9	DQ1B25	
B8	VREF0B8	IO	DQ9B0		AB19	AF3	AF3	AH24	DQ3B8	DQ1B24	
B8	VREF0B8	VREF0B8			R18	AE5	AE5	AD22			
B8	VREF0B8	IO						AD24			
B8	VREF0B8	IO						AB21			
B8	VREF0B8	IO	DQ8B7		W18	AC7	AC7	AG23	DQ3B7	DQ1B23	
B8	VREF0B8	IO	DQ8B6		AA18	AD6	AD6	AD23	DQ3B6	DQ1B22	
B8	VREF0B8	IO	DQ8B5		AA17	AE7	AE7	AF23	DQ3B5	DQ1B21	
B8	VREF0B8	IO	DQ8B4		AB18	AB7	AB7	AH23	DQ3B4	DQ1B20	
B8	VREF0B8	IO	DQ8B3		V18	AD7	AD7	AE22	DQ3B3	DQ1B19	
B8	VREF0B8	IO	DQS8B		Y18	AE6	AE6	AE23	DQS3B		
B8	VREF0B8	IO	DQ8B2		W17	AA7	AA7	AF22	DQ3B2	DQ1B18	
B8	VREF0B8	IO	DQ8B1		Y17	AF7	AF7	AH22	DQ3B1	DQ1B17	
B8	VREF0B8	IO	DQ8B0		AB17	AF6	AF6	AG22	DQ3B0	DQ1B16	
B8	VREF0B8	IO						AB20			
B8	VREF1B8	IO	DQ7B7		U17	AC8	AC8	AD21	DQ2B15	DQ1B15	
B8	VREF1B8	IO	DQ7B6		U16	AB8	AB8	AE21	DQ2B14	DQ1B14	

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F484	B672	F672	F780	DQS for x16	DQS for x32	DIFFIO Speed (1)
B8	VREF1B8	IO	DQ7B5		V17	AD8	AD8	AG21	DQ2B13	DQ1B13	
B8	VREF1B8	IO	DQ7B4		V16	AE8	AE8	AF21	DQ2B12	DQ1B12	
B8	VREF1B8	IO	DQ7B3		Y16	AF8	AF8	AE20	DQ2B11	DQ1B11	
B8	VREF1B8	IO	DQS7B		AA16	Y9	Y9	AG20		DQS1B	
B8	VREF1B8	IO	DQ7B2		T16	Y8	Y8	AF20	DQ2B10	DQ1B10	
B8	VREF1B8	IO	DQ6B7		Y15	AC9	AC9	AE19	DQ2B7	DQ1B7	
B8	VREF1B8	IO	DQ7B1		W16	W9	W9	AH21	DQ2B9	DQ1B9	
B8	VREF1B8	IO	DQ6B6		AA15	AF9	AF9	AD19	DQ2B6	DQ1B6	
B8	VREF1B8	IO	DQ7B0		AB16	AA8	AA8	AH20	DQ2B8	DQ1B8	
B8	VREF1B8	IO	DQ6B5		AB15	AD10	AD10	AF19	DQ2B5	DQ1B5	
B8	VREF1B8	VREF1B8			R16	AE9	AE9	AD20			
B8	VREF1B8	IO	DQ6B4		V15	AE10	AE10	AG19	DQ2B4	DQ1B4	
B8	VREF1B8	IO	DQ6B3		U15	AC10	AC10	AH19	DQ2B3	DQ1B3	
B8	VREF1B8	IO	DQS6B		W15	Y10	Y10	AF18	DQS2B		
B8	VREF1B8	IO		PGM2	R15	AA9	AA9	AB19			
B8	VREF1B8	IO	FCLK3		P16	AD9	AD9	AC21			
B8	VREF1B8	IO	FCLK2		T15	AB9	AB9	AC19			
B8	VREF1B8	IO	DQ6B2		U14	AA10	AA10	AD18	DQ2B2	DQ1B2	
B8	VREF1B8	IO		CRC_ERROR	N14	W10	W10	AA20			
B8	VREF1B8	IO	DQ6B1		W14	AB10	AB10	AE18	DQ2B1	DQ1B1	
B8	VREF1B8	IO	DQ6B0		V14	AF10	AF10	AG18	DQ2B0	DQ1B0	
B8	VREF1B8	IO	RDN8		P15	AB11	AB11	Y19			
B8	VREF1B8	IO	RUP8		N15	AE11	AE11	W19			
B8	VREF1B8	IO	DQ5B7					AF17			
B8	VREF1B8	IO	DQ5B6					AG17			
B8	VREF1B8	IO	DQ5B5					AE17			
B8	VREF1B8	IO	DQ5B4					AD17			
B8	VREF1B8	IO		RDYnBSY	P14	AC11	AC11	AA19			
B8	VREF1B8	IO	DQ5B3					AG16			
B8	VREF2B8	IO	DQS5B					AH16			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F484	B672	F672	F780	DQS for x16	DQS for x32	DIFFIO Speed (1)
B8	VREF2B8	IO	DQ5B2					AD16			
B8	VREF2B8	IO		nCS	T14	Y11	Y11	Y18			
B8	VREF2B8	IO	DQ5B1					AF16			
B8	VREF2B8	IO	DQ5B0					AE16			
B8	VREF2B8	IO						Y20			
B8	VREF2B8	IO						AC22			
B8	VREF2B8	IO						AC20			
B8	VREF2B8	IO			N13	AD11	AD11	AB18			
B8	VREF2B8	IO		CS	P13	AA11	AA11	AA18			
B8	VREF2B8	IO						V18			
B8	VREF2B8	IO						W18			
B8	VREF2B8	VREF2B8			R14	W11	W11	AH18			
B8	VREF2B8	IO	CLK5n		W13	AD12	AD12	Y17			
B8	VREF2B8	CLK5p			V13	AC12	AC12	AA17			
B8	VREF2B8	IO	CLK4n		Y14	AF12	AF12	AB17			
B8	VREF2B8	CLK4p			AA14	AE12	AE12	AC17			
B8	VREF2B8	PLL_ENA		PLL_ENA	R13	W12	W12	AC18			
B8	VREF2B8	MSEL0		MSEL0	T13	Y12	Y12	AC16			
B8	VREF2B8	MSEL1		MSEL1	P12	Y13	Y13	W17			
B8	VREF2B8	MSEL2		MSEL2	R12	W13	W13	AB15			
B12	VREF2B8	IO	PLL6_OUT3n					Y16			
B12	VREF2B8	IO	PLL6_OUT3p					W16			
B12	VREF2B8	IO	PLL6_OUT2n					AG15			
B12	VREF2B8	IO	PLL6_OUT2p					AF15			
B11	VREF2B8	IO	PLL6_FBn		Y12	AB12	AB12	AA15			
B11	VREF2B8	IO	PLL6_FBp		W12	AA12	AA12	AA14			
B11	VREF2B8	IO	PLL6_OUT1n		AB12	AB14	AB14	W15			
B11	VREF2B8	IO	PLL6_OUT1p		AA12	AA14	AA14	W14			
B11	VREF2B8	IO	PLL6_OUT0n		Y13	AB13	AB13	AE15			
B11	VREF2B8	IO	PLL6_OUT0p		AA13	AA13	AA13	AD15			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F484	B672	F672	F780	DQS for x16	DQS for x32	DIFFIO Speed (1)
B12		VCC_PLL6_OUTB						AB16			
B11		VCC_PLL6_OUTA						AC14			
B11		VCC_PLL6_OUTA			U13	AE13	AE13				
		VCCA_PLL6			T12	AD14	AD14	AG14			
		GND									
		GNDA_PLL6			U12	AC14	AC14	AF14			
		VCCG_PLL6			U11	AD13	AD13	AA13			
		GNDG_PLL6			T11	AE14	AE14	AB14			
B7	VREF0B7	CLK7p			AA11	AE15	AE15	W13			
B7	VREF0B7	IO	CLK7n					Y13			
B7	VREF0B7	CLK6p			AB11	AF15	AF15	AD14			
B7	VREF0B7	IO	CLK6n					AE14			
B7	VREF0B7	nCE		nCE	R11	Y14	Y14	AB13			
B7	VREF0B7	nCEO		nCEO	P11	W14	W14	AC13			
B7	VREF0B7	IO						V11			
B7	VREF0B7	IO						Y11			
B7	VREF0B7	IO		PGM0	N10	W15	W15	W12			
B7	VREF0B7	nIO_PULLUP		nIO_PULLUP	N9	AA15	AA15	Y12			
B7	VREF0B7	VCCSEL		VCCSEL	R10	Y15	Y15	AA12			
B7	VREF0B7	PORSEL		PORSEL	U10	W16	W16	AC12			
B7	VREF0B7	IO		INIT_DONE	P10	AC15	AC15	W11			
B7	VREF0B7	IO	DQ4B7		V12			AD13			
B7	VREF0B7	IO	DQ4B6		V11			AE13			
B7	VREF0B7	IO		nRS	T10	Y16	Y16	AC11			
B7	VREF0B7	IO	DQ4B5		W11			AF13			
B7	VREF0B7	IO	DQ4B4		Y11			AD12			
B7	VREF0B7	VREF0B7			R9	AB15	AB15	AD11			
B7	VREF0B7	IO	DQ4B3		V10			AG13			
B7	VREF0B7	IO		RUnLU	P9	AD15	AD15	W10			
B7	VREF0B7	IO	DQS4B		W10			AH13			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F484	B672	F672	F780	DQS for x16	DQS for x32	DIFFIO Speed (1)
B7	VREF0B7	IO	DQ4B2		AA9			AE12			
B7	VREF0B7	IO	DQ4B1		Y10			AF12			
B7	VREF0B7	IO	DQ4B0		AA10			AG12			
B7	VREF0B7	IO		PGM1	M8	AC16	AC16	AA11			
B7	VREF0B7	IO	RDN7		T9	AB16	AB16	AC10			
B7	VREF0B7	IO	RUP7		N8	AD16	AD16	AB11			
B7	VREF0B7	IO	DQ3B7		AA8	W17	W17	AG11	DQ1B15	DQ0B31	
B7	VREF0B7	IO	DQ3B6		Y9	AE16	AE16	AH11	DQ1B14	DQ0B30	
B7	VREF0B7	IO	DQ3B5		Y8	Y17	Y17	AE11	DQ1B13	DQ0B29	
B7	VREF1B7	IO	DEV_CLRn		P8	AF17	AF17	AC9			
B7	VREF1B7	IO	DQ3B4		U9	AA17	AA17	AF11	DQ1B12	DQ0B28	
B7	VREF1B7	IO	DQ3B3		V9	Y18	Y18	AE10	DQ1B11	DQ0B27	
B7	VREF1B7	IO	DQS3B		W8	AE17	AE17	AG10	DQS1B		
B7	VREF1B7	IO						Y10			
B7	VREF1B7	IO	DQ3B2		W9	W18	W18	AH10	DQ1B10	DQ0B26	
B7	VREF1B7	IO	DQ3B1		V8	AB17	AB17	AF10	DQ1B9	DQ0B25	
B7	VREF1B7	IO	DQ3B0		U8	AA18	AA18	AD10	DQ1B8	DQ0B24	
B7	VREF1B7	IO			R8	AF20	AF20	AA10			
B7	VREF1B7	IO						AB9			
B7	VREF1B7	IO	FCLK5		T8	AC17	AC17	AC8			
B7	VREF1B7	IO	FCLK4		M7	AD17	AD17	AB10			
B7	VREF1B7	VREF1B7			R7	AB18	AB18	AD9			
B7	VREF1B7	IO	DQ2B7		W7	AF18	AF18	AG9	DQ1B7	DQ0B23	
B7	VREF1B7	IO	DQ2B6		U6	AE18	AE18	AF9	DQ1B6	DQ0B22	
B7	VREF1B7	IO	DQ2B5		AB8	AF19	AF19	AE9	DQ1B5	DQ0B21	
B7	VREF1B7	IO	DQ2B4		V6	Y20	Y20	AH8	DQ1B4	DQ0B20	
B7	VREF1B7	IO	DQ2B3		AB7	AA19	AA19	AH9	DQ1B3	DQ0B19	
B7	VREF1B7	IO	DQS2B		AA7	AB19	AB19	AE8		DQS0B	
B7	VREF1B7	IO	DQ2B2		U7	AD19	AD19	AD8	DQ1B2	DQ0B18	
B7	VREF1B7	IO						AA9			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F484	B672	F672	F780	DQS for x16	DQS for x32	DIFFIO Speed (1)
B7	VREF1B7	IO	DQ2B1		V7	AC19	AC19	AF8	DQ1B1	DQ0B17	
B7	VREF1B7	IO						AB8			
B7	VREF1B7	IO	DQ2B0		Y7	AE19	AE19	AG8	DQ1B0	DQ0B16	
B7	VREF1B7	IO						AC7			
B7	VREF2B7	IO	DQ1B7		Y6	AE20	AE20	AF6	DQ0B15	DQ0B15	
B7	VREF2B7	IO	DQ1B6		V5	AA20	AA20	AG7	DQ0B14	DQ0B14	
B7	VREF2B7	IO	DQ1B5		AA6	AB20	AB20	AH7	DQ0B13	DQ0B13	
B7	VREF2B7	IO	DQ1B4		W6	AF21	AF21	AF7	DQ0B12	DQ0B12	
B7	VREF2B7	IO	DQ1B3		AB6	AC20	AC20	AD6	DQ0B11	DQ0B11	
B7	VREF2B7	IO	DQS1B		AB5	AA21	AA21	AE7	DQS0B		
B7	VREF2B7	IO	DQ1B2		W5	AE21	AE21	AH6	DQ0B10	DQ0B10	
B7	VREF2B7	IO						AD5			
B7	VREF2B7	IO	DQ1B1		Y5	AD20	AD20	AG6	DQ0B9	DQ0B9	
B7	VREF2B7	IO	DQ0B7		AA4	AE25	AE25	AF5	DQ0B7	DQ0B7	
B7	VREF2B7	IO	DQ1B0		AA5	AC21	AC21	AE6	DQ0B8	DQ0B8	
B7	VREF2B7	IO	DQ0B6		AB4	AF22	AF22	AH5	DQ0B6	DQ0B6	
B7	VREF2B7	VREF2B7			R5	AD21	AD21	AD7			
B7	VREF2B7	IO						Y9			
B7	VREF2B7	IO	DQ0B5		Y2	AF24	AF24	AF4	DQ0B5	DQ0B5	
B7	VREF2B7	IO	DQ0B4		Y4	AE22	AE22	AG4	DQ0B4	DQ0B4	
B7	VREF2B7	IO			T7	Y19	Y19	AE4			
B7	VREF2B7	IO	DQ0B3		AA3	AB22	AB22	AG5	DQ0B3	DQ0B3	
B7	VREF2B7	IO	DQS0B		AA2	AE23	AE23	AH3			
B7	VREF2B7	IO			P7	AD22	AD22	AB12			
B7	VREF2B7	IO	DQ0B2		W3	AC23	AC23	AG3	DQ0B2	DQ0B2	
B7	VREF2B7	IO	DQ0B1		W4	AC22	AC22	AE5	DQ0B1	DQ0B1	
B7	VREF2B7	IO			N7	AB21	AB21	AC5			
B7	VREF2B7	IO	DQ0B0		Y3	AE24	AE24	AH4	DQ0B0	DQ0B0	
B7	VREF2B7	IO						AB7			
B6	VREF0B6	IO	DIFFIO_TX65n		V4	AD25	AD25	AA7			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F484	B672	F672	F780	DQS for x16	DQS for x32	DIFFIO Speed (1)
B6	VREF0B6	IO	DIFFIO_TX65p		V3	AC24	AC24	AA8			HIGH
B6	VREF0B6	IO	DIFFIO_RX65n			AD26	AD26	AF2			HIGH
B6	VREF0B6	IO	DIFFIO_RX65p			AC25	AC25	AF1			HIGH
B6	VREF0B6	IO	DIFFIO_TX64n		U5	AB24	AB24	AA5			HIGH
B6	VREF0B6	IO	DIFFIO_TX64p			AB23	AB23	AA6			HIGH
B6	VREF0B6	IO	DIFFIO_RX64n			AB26	AB26	AE2			HIGH
B6	VREF0B6	IO	DIFFIO_RX64p			AB25	AB25	AE1			HIGH
B6	VREF0B6	IO	DIFFIO_TX63n		T5	AA24	AA24	Y6			HIGH
B6	VREF0B6	IO	DIFFIO_TX63p			AA23	AA23	Y5			HIGH
B6	VREF0B6	IO	DIFFIO_RX63n			AA26	AA26	AD2			HIGH
B6	VREF0B6	IO	DIFFIO_RX63p			AA25	AA25	AD1			HIGH
B6	VREF0B6	IO	DIFFIO_TX62n		P4	AA22	AA22	Y7			HIGH
B6	VREF0B6	IO	DIFFIO_TX62p			Y22	Y22	Y8			HIGH
B6	VREF0B6	IO	DIFFIO_RX62n			Y26	Y26	AC2			HIGH
B6	VREF0B6	IO	DIFFIO_RX62p			Y25	Y25	AC1			HIGH
B6	VREF0B6	VREF0B6			R6	Y21	Y21	AE3			
B6	VREF0B6	IO	DIFFIO_TX61n		U4	Y24	Y24	W7			HIGH
B6	VREF0B6	IO	DIFFIO_TX61p		U3	Y23	Y23	W8			HIGH
B6	VREF0B6	IO	DIFFIO_RX61n			W23	W23	AB4			HIGH
B6	VREF0B6	IO	DIFFIO_RX61p			W24	W24	AB3			HIGH
B6	VREF0B6	IO	DIFFIO_TX60n		P6	W21	W21	W5			HIGH
B6	VREF0B6	IO	DIFFIO_TX60p			W22	W22	W6			HIGH
B6	VREF0B6	IO	DIFFIO_RX60n					AB2			HIGH
B6	VREF0B6	IO	DIFFIO_RX60p					AB1			HIGH
B6	VREF0B6	IO	DIFFIO_TX59n					V8			HIGH
B6	VREF0B6	IO	DIFFIO_TX59p					V7			HIGH
B6	VREF0B6	IO	DIFFIO_RX59n/RDN6		W1	U24	U24	AA3			HIGH
B6	VREF0B6	IO	DIFFIO_RX59p/RUP6		W2	U23	U23	AA4			HIGH
B6	VREF0B6	IO	DIFFIO_TX58n					V6			HIGH
B6	VREF0B6	IO	DIFFIO_TX58p					V5			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F484	B672	F672	F780	DQS for x16	DQS for x32	DIFFIO Speed (1)
B6	VREF0B6	IO	DIFFIO_RX58n					AA2			HIGH
B6	VREF0B6	IO	DIFFIO_RX58p					AA1			HIGH
B6	VREF1B6	IO	DIFFIO_TX57n		T4	V19	V19	V9			HIGH
B6	VREF1B6	IO	DIFFIO_TX57p		T3	U20	U20	V10			HIGH
B6	VREF1B6	IO	DIFFIO_RX57n			U26	U26	Y4			HIGH
B6	VREF1B6	IO	DIFFIO_RX57p			U25	U25	Y3			HIGH
B6	VREF1B6	IO	DIFFIO_TX56n		N6	U19	U19	U7			HIGH
B6	VREF1B6	IO	DIFFIO_TX56p			U18	U18	U8			HIGH
B6	VREF1B6	IO	DIFFIO_RX56n		V2	U22	U22	Y2			HIGH
B6	VREF1B6	IO	DIFFIO_RX56p		V1	U21	U21	Y1			HIGH
B6	VREF1B6	IO	DIFFIO_TX55n		M6	T21	T21	U6			HIGH
B6	VREF1B6	IO	DIFFIO_TX55p			T20	T20	U5			HIGH
B6	VREF1B6	IO	DIFFIO_RX55n			T25	T25	W4			HIGH
B6	VREF1B6	IO	DIFFIO_RX55p			T24	T24	W3			HIGH
B6	VREF1B6	IO	DIFFIO_TX54n		R3	T19	T19	U9			HIGH
B6	VREF1B6	IO	DIFFIO_TX54p		R4	R19	R19	U10			HIGH
B6	VREF1B6	IO	DIFFIO_RX54n					W2			HIGH
B6	VREF1B6	IO	DIFFIO_RX54p					W1			HIGH
B6	VREF1B6	VREF1B6			P5	V20	V20	W9			
B6	VREF1B6	IO	DIFFIO_TX53n					T6			HIGH
B6	VREF1B6	IO	DIFFIO_TX53p					T5			HIGH
B6	VREF1B6	IO	DIFFIO_RX53n		U1	T23	T23	V4			HIGH
B6	VREF1B6	IO	DIFFIO_RX53p		U2	T22	T22	V3			HIGH
B6	VREF1B6	IO	DIFFIO_TX52n					T10			HIGH
B6	VREF1B6	IO	DIFFIO_TX52p					T9			HIGH
B6	VREF1B6	IO	DIFFIO_RX52n		T2	R22	R22	V1			HIGH
B6	VREF1B6	IO	DIFFIO_RX52p		T1	R23	R23	V2			HIGH
B6	VREF1B6	IO	DIFFIO_TX51n		P3	P20	P20	T7			HIGH
B6	VREF1B6	IO	DIFFIO_TX51p		P2	P21	P21	T8			HIGH
B6	VREF1B6	IO	DIFFIO_RX51n		R2	R20	R20	U4			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F484	B672	F672	F780	DQS for x16	DQS for x32	DIFFIO Speed (1)
B6	VREF1B6	IO	DIFFIO_RX51p		R1	R21	R21	U3			HIGH
B6	VREF1B6	IO	DIFFIO_TX50n		N3	P19	P19	T4			HIGH
B6	VREF1B6	IO	DIFFIO_TX50p		N2	N19	N19	T3			HIGH
B6	VREF1B6	IO	DIFFIO_RX50n					U2			HIGH
B6	VREF1B6	IO	DIFFIO_RX50p					T1			HIGH
B6	VREF1B6	IO	CLK8n					R3			
B6	VREF1B6	CLK8p			M3	P24	P24	R4			
B6	VREF1B6	CLK9n			M1	P25	P25	T2			
B6	VREF1B6	CLK9p			M2	R26	R26	R2			
		GNDG_PLL3			N4	R25	R25	R7			
		VCCG_PLL3			N5	P23	P23	R8			
		GNDA_PLL3			M4	R24	R24	R5			
		GND									
		VCCA_PLL3			M5	P22	P22	R6			
		GNDG_PLL4			L5	N22	N22	P7			
		VCCG_PLL4			K5	N24	N24	P8			
		GNDA_PLL4			L4	N23	N23	P5			
		GND									
		VCCA_PLL4			K4	N25	N25	P6			
B5	VREF0B5	CLK10p			L3	M26	M26	P4			
B5	VREF0B5	IO	CLK10n					P3			
B5	VREF0B5	CLK11p			L2	M24	M24	P2			
B5	VREF0B5	CLK11n			L1	M25	M25	N2			
B5	VREF0B5	IO	DIFFIO_TX49n		K2	N20	N20	N10			HIGH
B5	VREF0B5	IO	DIFFIO_TX49p		K3	N21	N21	N9			HIGH
B5	VREF0B5	IO	DIFFIO_RX49n					M2			HIGH
B5	VREF0B5	IO	DIFFIO_RX49p					N1			HIGH
B5	VREF0B5	IO	DIFFIO_TX48n		J2	M18	M18	N5			HIGH
B5	VREF0B5	IO	DIFFIO_TX48p		J3	M19	M19	N6			HIGH
B5	VREF0B5	IO	DIFFIO_RX48n		H1	M20	M20	M3			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F484	B672	F672	F780	DQS for x16	DQS for x32	DIFFIO Speed (1)
B5	VREF0B5	IO	DIFFIO_RX48p		H2	M21	M21	M4			HIGH
B5	VREF0B5	IO	DIFFIO_TX47n					N7			HIGH
B5	VREF0B5	IO	DIFFIO_TX47p					N8			HIGH
B5	VREF0B5	IO	DIFFIO_RX47n		G2	M22	M22	L1			HIGH
B5	VREF0B5	IO	DIFFIO_RX47p		G1	M23	M23	L2			HIGH
B5	VREF0B5	VREF0B5			J5	L19	L19	P10			
B5	VREF0B5	IO	DIFFIO_TX46n					N4			HIGH
B5	VREF0B5	IO	DIFFIO_TX46p					N3			HIGH
B5	VREF0B5	IO	DIFFIO_RX46n		F1	L22	L22	L3			HIGH
B5	VREF0B5	IO	DIFFIO_RX46p		F2	L23	L23	L4			HIGH
B5	VREF0B5	IO	DIFFIO_TX45n		H3	L21	L21	M10			HIGH
B5	VREF0B5	IO	DIFFIO_TX45p		H4	L20	L20	M9			HIGH
B5	VREF0B5	IO	DIFFIO_RX45n					K1			HIGH
B5	VREF0B5	IO	DIFFIO_RX45p					K2			HIGH
B5	VREF0B5	IO	DIFFIO_TX44n		K6	K20	K20	M6			HIGH
B5	VREF0B5	IO	DIFFIO_TX44p			K19	K19	M5			HIGH
B5	VREF0B5	IO	DIFFIO_RX44n			L25	L25	K4			HIGH
B5	VREF0B5	IO	DIFFIO_RX44p			L24	L24	K3			HIGH
B5	VREF0B5	IO	DIFFIO_TX43n		L6	K22	K22	M8			HIGH
B5	VREF0B5	IO	DIFFIO_TX43p			K21	K21	M7			HIGH
B5	VREF0B5	IO	DIFFIO_RX43n			K24	K24	J1			HIGH
B5	VREF0B5	IO	DIFFIO_RX43p			K23	K23	J2			HIGH
B5	VREF0B5	IO	DIFFIO_TX42n		G3	J20	J20	L10			HIGH
B5	VREF0B5	IO	DIFFIO_TX42p		G4	J19	J19	L9			HIGH
B5	VREF0B5	IO	DIFFIO_RX42n			K26	K26	J3			HIGH
B5	VREF0B5	IO	DIFFIO_RX42p			K25	K25	J4			HIGH
B5	VREF1B5	IO	DIFFIO_TX41n					L5			HIGH
B5	VREF1B5	IO	DIFFIO_TX41p					L6			HIGH
B5	VREF1B5	IO	DIFFIO_RX41n					H1			HIGH
B5	VREF1B5	IO	DIFFIO_RX41p					H2			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F484	B672	F672	F780	DQS for x16	DQS for x32	DIFFIO Speed (1)
B5	VREF1B5	IO	DIFFIO_TX40n					L8			HIGH
B5	VREF1B5	IO	DIFFIO_TX40p					L7			HIGH
B5	VREF1B5	IO	DIFFIO_RX40n/RDN5		E1	J22	J22	H3			HIGH
B5	VREF1B5	IO	DIFFIO_RX40p/RUP5		E2	J21	J21	H4			HIGH
B5	VREF1B5	IO	DIFFIO_TX39n					K7			HIGH
B5	VREF1B5	IO	DIFFIO_TX39p					K8			HIGH
B5	VREF1B5	IO	DIFFIO_RX39n		D2	J24	J24	G1			HIGH
B5	VREF1B5	IO	DIFFIO_RX39p		D1	J23	J23	G2			HIGH
B5	VREF1B5	IO	DIFFIO_TX38n		J6	H24	H24	J7			HIGH
B5	VREF1B5	IO	DIFFIO_TX38p			H23	H23	J8			HIGH
B5	VREF1B5	IO	DIFFIO_RX38n					G4			HIGH
B5	VREF1B5	IO	DIFFIO_RX38p					G3			HIGH
B5	VREF1B5	VREF1B5			H5	J18	J18	K9			
B5	VREF1B5	IO	DIFFIO_TX37n		J4	G21	G21	K5			HIGH
B5	VREF1B5	IO	DIFFIO_TX37p			G22	G22	K6			HIGH
B5	VREF1B5	IO	DIFFIO_RX37n			H25	H25	F1			HIGH
B5	VREF1B5	IO	DIFFIO_RX37p			H26	H26	F2			HIGH
B5	VREF1B5	IO	DIFFIO_TX36n		G5	G23	G23	J6			HIGH
B5	VREF1B5	IO	DIFFIO_TX36p			G24	G24	J5			HIGH
B5	VREF1B5	IO	DIFFIO_RX36n			G25	G25	F3			HIGH
B5	VREF1B5	IO	DIFFIO_RX36p			G26	G26	F4			HIGH
B5	VREF1B5	IO	DIFFIO_TX35n		F5	F23	F23	H8			HIGH
B5	VREF1B5	IO	DIFFIO_TX35p			F24	F24	H7			HIGH
B5	VREF1B5	IO	DIFFIO_RX35n			F25	F25	E1			HIGH
B5	VREF1B5	IO	DIFFIO_RX35p			F26	F26	E2			HIGH
B5	VREF1B5	IO	DIFFIO_TX34n		F3	E23	E23	H6			HIGH
B5	VREF1B5	IO	DIFFIO_TX34p		F4	E24	E24	H5			HIGH
B5	VREF1B5	IO	DIFFIO_RX34n			E25	E25	D1			HIGH
B5	VREF1B5	IO	DIFFIO_RX34p			E26	E26	D2			HIGH
B5	VREF1B5	IO	DIFFIO_TX33n		E3	D24	D24	G5			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F484	B672	F672	F780	DQS for x16	DQS for x32	DIFFIO Speed (1)
B5	VREF1B5	IO	DIFFIO_TX33p		E4	C25	C25	G6			HIGH
B5	VREF1B5	IO	DIFFIO_RX33n			D25	D25	C1			HIGH
B5	VREF1B5	IO	DIFFIO_RX33p			C26	C26	C2			HIGH
B4	VREF0B4	IO						G7			
B4	VREF0B4	IO	DQ0T0		B3	B24	B24	A4		DQ0T0	
B4	VREF0B4	IO			K7	C23	C23	G12			
B4	VREF0B4	IO	DQ0T1		B2	D23	D23	A3		DQ0T1	
B4	VREF0B4	IO	DQ0T2		D3	D22	D22	B3		DQ0T2	
B4	VREF0B4	IO	DQS0T		C2	C24	C24	D5			
B4	VREF0B4	IO			J7	C19	C19	G8			
B4	VREF0B4	IO	DQ0T3		B4	E22	E22	B5		DQ0T3	
B4	VREF0B4	IO	DQ0T4		C3	B22	B22	B4		DQ0T4	
B4	VREF0B4	IO	DQ0T5		C4	A24	A24	C4		DQ0T5	
B4	VREF0B4	IO						F8			
B4	VREF0B4	IO	DQ0T6		D4	A22	A22	A5		DQ0T6	
B4	VREF0B4	VREF0B4			H6	F22	F22	E7			
B4	VREF0B4	IO	DQ0T7		A4	C22	C22	C5		DQ0T7	
B4	VREF0B4	IO						J9			
B4	VREF0B4	IO			G7	B21	B21	H9			
B4	VREF0B4	IO	DQ1T0		C5	C20	C20	E6		DQ0T8	
B4	VREF0B4	IO						G9			
B4	VREF0B4	IO	DQ1T1		D5	D21	D21	A6		DQ0T9	
B4	VREF0B4	IO	DQ1T2		B5	D20	D20	B7		DQ0T10	
B4	VREF0B4	IO	DQS1T		A5	A21	A21	B6			
B4	VREF0B4	IO						F9			
B4	VREF0B4	IO	DQ1T3		C6	C21	C21	D6		DQ0T11	
B4	VREF0B4	IO	DQ1T4		E5	B20	B20	A7		DQ0T12	
B4	VREF0B4	IO	DQ1T5		D6	E21	E21	D7		DQ0T13	
B4	VREF1B4	IO	DQ1T6		A6	A20	A20	C6		DQ0T14	
B4	VREF1B4	IO	DQ2T0		B7	D19	D19	D8	DQ1T0	DQ0T16	

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F484	B672	F672	F780	DQS for x16	DQS for x32	DIFFIO Speed (1)
B4	VREF1B4	IO	DQ1T7		B6	F21	F21	C7		DQ0T15	
B4	VREF1B4	IO	DQ2T1		E6	E20	E20	C8	DQ1T1	DQ0T17	
B4	VREF1B4	IO						H10			
B4	VREF1B4	IO	DQ2T2		F7	E19	E19	E8	DQ1T2	DQ0T18	
B4	VREF1B4	IO	DQS2T		A7	A19	A19	C9		DQS0T	
B4	VREF1B4	IO	DQ2T3		A8	C18	C18	D9	DQ1T3	DQ0T19	
B4	VREF1B4	IO	DQ2T4		D7	B18	B18	B9	DQ1T4	DQ0T20	
B4	VREF1B4	IO	DQ2T5		C7	D18	D18	B8	DQ1T5	DQ0T21	
B4	VREF1B4	IO	DQ2T6		F6	F20	F20	A8	DQ1T6	DQ0T22	
B4	VREF1B4	IO	DQ2T7		E7	G20	G20	A9	DQ1T7	DQ0T23	
B4	VREF1B4	VREF1B4			H7	F18	F18	E9			
B4	VREF1B4	IO	FCLK6		G8	G19	G19	G10			
B4	VREF1B4	IO	FCLK7		H8	E18	E18	F10			
B4	VREF1B4	IO	DQ3T0		E8	F19	F19	E10	DQ1T8	DQ0T24	
B4	VREF1B4	IO	DQ3T1		C8	C17	C17	A10	DQ1T9	DQ0T25	
B4	VREF1B4	IO	DQ3T2		F8	G18	G18	C10	DQ1T10	DQ0T26	
B4	VREF1B4	IO	DQS3T		D8	B17	B17	D10	DQS1T		
B4	VREF1B4	IO	DQ3T3		B8	E17	E17	B10	DQ1T11	DQ0T27	
B4	VREF1B4	IO						J10			
B4	VREF1B4	IO	DQ3T4		C9	F17	F17	A11	DQ1T12	DQ0T28	
B4	VREF1B4	IO	DQ3T5		D9	D17	D17	C11	DQ1T13	DQ0T29	
B4	VREF1B4	IO	DQ3T6		E9	A17	A17	D11	DQ1T14	DQ0T30	
B4	VREF1B4	IO	DQ3T7		F9	H18	H18	B11	DQ1T15	DQ0T31	
B4	VREF2B4	IO	DEV_OE		L7	G17	G17	J11			
B4	VREF2B4	IO			G9	B16	B16	F11			
B4	VREF2B4	IO						K10			
B4	VREF2B4	IO	RUP4		J8	D16	D16	H11			
B4	VREF2B4	IO	RDN4		K8	C16	C16	G11			
B4	VREF2B4	IO	DQ4T0		B9			B12			
B4	VREF2B4	IO		nWS	F10	E16	E16	K11			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F484	B672	F672	F780	DQS for x16	DQS for x32	DIFFIO Speed (1)
B4	VREF2B4	IO	DQ4T1		C10			C12			
B4	VREF2B4	IO	DQ4T2		B10			D12			
B4	VREF2B4	IO	DQS4T		D10			A13			
B4	VREF2B4	IO		DATA0	L8	F16	F16	H12			
B4	VREF2B4	IO	DQ4T3		E10			B13			
B4	VREF2B4	VREF2B4			H9	G16	G16	E11			
B4	VREF2B4	IO	DQ4T4		C11			E12			
B4	VREF2B4	IO	DQ4T5		D11			C13			
B4	VREF2B4	IO		DATA1	J9	C15	C15	F12			
B4	VREF2B4	IO	DQ4T6		E11			D13			
B4	VREF2B4	IO	DQ4T7		E12			E13			
B4	VREF2B4	IO		DATA2	H10	H16	H16	J12			
B4	VREF2B4	TMS		TMS	G10	E15	E15	F13			
B4	VREF2B4	TRST		TRST	J10	D15	D15	L12			
B4	VREF2B4	TCK		TCK	K9	G15	G15	K12			
B4	VREF2B4	IO		DATA3	K10	F15	F15	M12			
B4	VREF2B4	IO						L11			
B4	VREF2B4	IO						M11			
B4	VREF2B4	TDI		TDI	J11	H15	H15	G13			
B4	VREF2B4	TDO		TDO	H11	G14	G14	H13			
B4	VREF2B4	IO	CLK12n					J13			
B4	VREF2B4	CLK12p			A11	B15	B15	K13			
B4	VREF2B4	IO	CLK13n					L13			
B4	VREF2B4	CLK13p			B11	A15	A15	M13			
		TEMPDIODEp			G12	H14	H14	B14			
		TEMPDIODEn			H12	G13	G13	C14			
		VCCA_PLL5			G13	D14	D14	F14			
		GND									
		GNDA_PLL5			F12	B14	B14	G14			
		VCCG_PLL5			F11	C14	C14	D14			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F484	B672	F672	F780	DQS for x16	DQS for x32	DIFFIO Speed (1)
		GNDG_PLL5			G11	B13	B13	E14			
B9		VCC_PLL5_OUTA			F13	D13	D13	F15			
B10		VCC_PLL5_OUTB						G16			
B9	VREF0B3	IO	PLL5_OUT0p		C13	F13	F13	E15			
B9	VREF0B3	IO	PLL5_OUT0n		B13	E13	E13	D15			
B9	VREF0B3	IO	PLL5_OUT1p		B12	F14	F14	K14			
B9	VREF0B3	IO	PLL5_OUT1n		A12	E14	E14	K15			
B9	VREF0B3	IO	PLL5_FBp		D12	F12	F12	H14			
B9	VREF0B3	IO	PLL5_FBn		C12	E12	E12	H15			
B10	VREF0B3	IO	PLL5_OUT2p					C15			
B10	VREF0B3	IO	PLL5_OUT2n					B15			
B10	VREF0B3	IO	PLL5_OUT3p					K16			
B10	VREF0B3	IO	PLL5_OUT3n					J16			
B3	VREF0B3	nSTATUS		nSTATUS	J12	H13	H13	M16			
B3	VREF0B3	nCONFIG		nCONFIG	H13	H12	H12	L16			
B3	VREF0B3	DCLK		DCLK	J13	G12	G12	F16			
B3	VREF0B3	CONF_DONE		CONF_DONE	K13	H11	H11	G17			
B3	VREF0B3	CLK14p			B14	B12	B12	K17			
B3	VREF0B3	IO	CLK14n		C14	A12	A12	J17			
B3	VREF0B3	CLK15p			E13	D12	D12	M17			
B3	VREF0B3	IO	CLK15n		D13	C12	C12	L17			
B3	VREF0B3	VREF0B3			H14	F11	F11	E18			
B3	VREF0B3	IO						L18			
B3	VREF0B3	IO						M18			
B3	VREF0B3	IO		DATA4	K14	E11	E11	H17			
B3	VREF0B3	IO			J14	B11	B11	F17			
B3	VREF0B3	IO						F18			
B3	VREF0B3	IO	DQ5T0					D16			
B3	VREF0B3	IO	DQ5T1					C16			
B3	VREF0B3	IO	DQ5T2					E16			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F484	B672	F672	F780	DQS for x16	DQS for x32	DIFFIO Speed (1)
B3	VREF0B3	IO		DATA5	G14	G11	G11	K18			
B3	VREF0B3	IO	DQS5T					A16			
B3	VREF0B3	IO	DQ5T3					B16			
B3	VREF0B3	IO	DQ5T4					E17			
B3	VREF1B3	IO		DATA6	K15	H10	H10	H18			
B3	VREF1B3	IO	DQ5T5					D17			
B3	VREF1B3	IO	DQ5T6					B17			
B3	VREF1B3	IO	DQ5T7					C17			
B3	VREF1B3	IO	RUP3		M15	C11	C11	J18			
B3	VREF1B3	IO	RDN3		L15	D11	D11	K19			
B3	VREF1B3	IO	DQ6T0		A15	A10	A10	A18	DQ2T0	DQ1T0	
B3	VREF1B3	IO	DQ6T1		C15	E10	E10	C18	DQ2T1	DQ1T1	
B3	VREF1B3	IO	DQ6T2		D14	F10	F10	D18	DQ2T2	DQ1T2	
B3	VREF1B3	IO		DATA7	J15	G10	G10	G18			
B3	VREF1B3	IO	DQS6T		F14	G9	G9	B18	DQS2T		
B3	VREF1B3	IO	DQ6T3		E14	F9	F9	A19	DQ2T3	DQ1T3	
		GND			G15	F8	F8	G20			
B3	VREF1B3	IO	FCLK0		K16	E9	E9	F19			
B3	VREF1B3	IO	FCLK1		J16	B9	B9	G19			
B3	VREF1B3	IO		CLKUSR	L16	D10	D10	J19			
B3	VREF1B3	IO	DQ6T4		D15	C10	C10	B19	DQ2T4	DQ1T4	
B3	VREF1B3	IO	DQ6T5		E15	B10	B10	C19	DQ2T5	DQ1T5	
B3	VREF1B3	IO	DQ6T6		F15	A9	A9	E19	DQ2T6	DQ1T6	
B3	VREF1B3	VREF1B3			H15	D9	D9	E20			
B3	VREF1B3	IO	DQ6T7		B15	C9	C9	D19	DQ2T7	DQ1T7	
B3	VREF1B3	IO	DQ7T0		A16	A8	A8	B20	DQ2T8	DQ1T8	
B3	VREF1B3	IO						H19			
B3	VREF1B3	IO	DQ7T1		E16	A7	A7	A20	DQ2T9	DQ1T9	
B3	VREF1B3	IO						J20			
B3	VREF1B3	IO	DQ7T2		G16	B8	B8	C20	DQ2T10	DQ1T10	

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F484	B672	F672	F780	DQS for x16	DQS for x32	DIFFIO Speed (1)
B3	VREF1B3	IO	DQS7T		B16	E8	E8	D20		DQS1T	
B3	VREF1B3	IO	DQ7T3		C16	F7	F7	A21	DQ2T11	DQ1T11	
B3	VREF1B3	IO	DQ7T4		D16	B7	B7	B21	DQ2T12	DQ1T12	
B3	VREF1B3	IO	DQ7T5		F16	C8	C8	C21	DQ2T13	DQ1T13	
B3	VREF1B3	IO	DQ7T6		E17	D8	D8	D21	DQ2T14	DQ1T14	
B3	VREF1B3	IO	DQ7T7		F17	E7	E7	E21	DQ2T15	DQ1T15	
B3	VREF2B3	IO	DQ8T0		A17	B6	B6	B22	DQ3T0	DQ1T16	
B3	VREF2B3	IO	DQ8T1		B17	A6	A6	A22	DQ3T1	DQ1T17	
B3	VREF2B3	IO	DQ8T2		C17	F6	F6	C22	DQ3T2	DQ1T18	
B3	VREF2B3	IO	DQS8T		C18	F5	F5	D23	DQS3T		
B3	VREF2B3	IO	DQ8T3		D17	D6	D6	D22	DQ3T3	DQ1T19	
B3	VREF2B3	IO	DQ8T4		E18	E6	E6	A23	DQ3T4	DQ1T20	
B3	VREF2B3	IO	DQ8T5		A18	A5	A5	C23	DQ3T5	DQ1T21	
B3	VREF2B3	IO	DQ8T6		B18	E5	E5	E23	DQ3T6	DQ1T22	
B3	VREF2B3	IO						H20			
B3	VREF2B3	IO	DQ8T7		D18	C7	C7	B23	DQ3T7	DQ1T23	
B3	VREF2B3	IO						F20			
B3	VREF2B3	IO						F21			
B3	VREF2B3	VREF2B3			H16	D7	D7	E22			
B3	VREF2B3	IO	DQ9T0		A19	C3	C3	A24	DQ3T8	DQ1T24	
B3	VREF2B3	IO	DQ9T1		B19	A3	A3	C25	DQ3T9	DQ1T25	
B3	VREF2B3	IO	DQ9T2		C19	D5	D5	A25	DQ3T10	DQ1T26	
B3	VREF2B3	IO	DQS9T		C21	B4	B4	C24			
B3	VREF2B3	IO	DQ9T3		D19	C2	C2	D24	DQ3T11	DQ1T27	
B3	VREF2B3	IO						G21			
B3	VREF2B3	IO	DQ9T4		B20	B3	B3	B24	DQ3T12	DQ1T28	
B3	VREF2B3	IO	DQ9T5		B21	D4	D4	B25	DQ3T13	DQ1T29	
B3	VREF2B3	IO	DQ9T6		C20	C4	C4	A26	DQ3T14	DQ1T30	
B3	VREF2B3	IO			M16	C5	C5	G22			
B3	VREF2B3	IO	DQ9T7		D20	D3	D3	B26	DQ3T15	DQ1T31	

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F484	B672	F672	F780	DQS for x16	DQS for x32	DIFFIO Speed (1)
B3	VREF2B3	IO						F22			
		VCCIO2			C22	D1	D1	B28			
		VCCIO2			K22	L1	L1	M28			
		VCCIO2				L9	L9	P20			
		VCCIO1			N22	T1	T1	R20			
		VCCIO1			Y22	AC1	AC1	U28			
		VCCIO1				T9	T9	AG28			
		VCCIO8			AB20	AF4	AF4	Y15			
		VCCIO8			AB13	AF11	AF11	AH17			
		VCCIO8				V11	V11	AH27			
		VCCIO8				V12	V12				
		VCCIO7			AB10	V15	V15	Y14			
		VCCIO7			AB3	V16	V16	AH2			
		VCCIO7				AF16	AF16	AH12			
		VCCIO7				AF23	AF23				
		VCCIO6			Y1	T18	T18	R9			
		VCCIO6			N1	AC26	AC26	U1			
		VCCIO6				T26	T26	AG1			
		VCCIO5			K1	L26	L26	B1			
		VCCIO5			C1	L18	L18	M1			
		VCCIO5				D26	D26	P9			
		VCCIO4			A3	A23	A23	A2			
		VCCIO4			A10	A16	A16	A12			
		VCCIO4				J15	J15	J14			
		VCCIO4				J16	J16				
		VCCIO3			A13	A4	A4	A17			
		VCCIO3			A20	A11	A11	A27			
		VCCIO3				J11	J11	J15			
		VCCIO3				J12	J12				
		VCCINT			A1	K11	K11	M14			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F484	B672	F672	F780	DQS for x16	DQS for x32	DIFFIO Speed (1)
		VCCINT			A22	K13	K13	N11			
		VCCINT			AB1	K15	K15	N13			
		VCCINT			AB22	K17	K17	N15			
		VCCINT			K12	L10	L10	N17			
		VCCINT			L11	L12	L12	P12			
		VCCINT			L13	L14	L14	P14			
		VCCINT			L9	L16	L16	P16			
		VCCINT			M10	M11	M11	R13			
		VCCINT			M12	M13	M13	R15			
		VCCINT			M14	M15	M15	R17			
		VCCINT			N11	M17	M17	T12			
		VCCINT				N10	N10	T14			
		VCCINT				N12	N12	T16			
		VCCINT				N14	N14	T18			
		VCCINT				N16	N16	U11			
		VCCINT				P11	P11	U13			
		VCCINT				P13	P13	U15			
		VCCINT				P15	P15	U17			
		VCCINT				P17	P17	V12			
		VCCINT				R10	R10	V16			
		VCCINT				R12	R12				
		VCCINT				R14	R14				
		VCCINT				R16	R16				
		VCCINT				T11	T11				
		VCCINT				T13	T13				
		VCCINT				T15	T15				
		VCCINT				T17	T17				
		VCCINT				U10	U10				
		VCCINT				U12	U12				
		VCCINT				U14	U14				

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F484	B672	F672	F780	DQS for x16	DQS for x32	DIFFIO Speed (1)
		VCCINT				U16	U16				
		GND			A14	A13	A13	A14			
		GND			A2	A14	A14	A15			
		GND			A21	A2	A2	AA16			
		GND			A9	A25	A25	AC15			
		GND			AA1	AC13	AC13	AF26			
		GND			AA22	AE1	AE1	AF3			
		GND			AB14	AE26	AE26	AG2			
		GND			AB2	AF13	AF13	AG27			
		GND			AB21	AF14	AF14	AH14			
		GND			AB9	AF2	AF2	AH15			
		GND			B1	AF25	AF25	B2			
		GND			B22	B1	B1	B27			
		GND			G17	B2	B2	C26			
		GND			G6	B26	B26	C3			
		GND			J1	C13	C13	G15			
		GND			J22	G8	G8	H16			
		GND			K11	H17	H17	L14			
		GND			L10	H9	H9	L15			
		GND			L12	J10	J10	M15			
		GND			L14	J13	J13	N12			
		GND			M11	J14	J14	N14			
		GND			M13	J17	J17	N16			
		GND			M9	J9	J9	N18			
		GND			N12	K10	K10	P1			
		GND			P1	K12	K12	P11			
		GND			P22	K14	K14	P13			
		GND			T17	K16	K16	P15			
		GND			T6	K18	K18	P17			
		GND				L11	L11	P18			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F484	B672	F672	F780	DQS for x16	DQS for x32	DIFFIO Speed (1)
		GND				L13	L13	P28			
		GND				L15	L15	R1			
		GND				L17	L17	R11			
		GND				M10	M10	R12			
		GND				M12	M12	R14			
		GND				M14	M14	R16			
		GND				M16	M16	R18			
		GND				N1	N1	R28			
		GND				N11	N11	T11			
		GND				N13	N13	T13			
		GND				N15	N15	T15			
		GND				N17	N17	T17			
		GND				N18	N18	U12			
		GND				N26	N26	U14			
		GND				N9	N9	U16			
		GND				P1	P1	U18			
		GND				P10	P10	V13			
		GND				P12	P12	V14			
		GND				P14	P14	V15			
		GND				P16	P16	V17			
		GND				P18	P18				
		GND				P26	P26				
		GND				P9	P9				
		GND				R11	R11				
		GND				R13	R13				
		GND				R15	R15				
		GND				R17	R17				
		GND				T10	T10				
		GND				T12	T12				
		GND				T14	T14				

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F484	B672	F672	F780	DQS for x16	DQS for x32	DIFFIO Speed (1)
		GND				T16	T16				
		GND				U11	U11				
		GND				U13	U13				
		GND				U15	U15				
		GND				U17	U17				
		GND				V10	V10				
		GND				V13	V13				
		GND				V14	V14				
		GND				V17	V17				
		GND				V18	V18				
		GND				V9	V9				
		NC				A18	A18	AB23			
		NC				AA16	AA16	AB24			
		NC				AC18	AC18	AB5			
		NC				AC5	AC5	AB6			
		NC				AC6	AC6	AC24			
		NC				AD18	AD18	AC25			
		NC				AD23	AD23	AC26			
		NC				AD24	AD24	AC3			
		NC				AF5	AF5	AC4			
		NC				B19	B19	AC6			
		NC				B23	B23	AD25			
		NC				B25	B25	AD26			
		NC				B5	B5	AD3			
		NC				C6	C6	AD4			
		NC				G7	G7	AE26			
		NC				H19	H19	D25			
		NC				H20	H20	D26			
		NC				H21	H21	D3			
		NC				H22	H22	D4			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F484	B672	F672	F780	DQS for x16	DQS for x32	DIFFIO Speed (1)
		NC				H7	H7	E25			
		NC				J1	J1	E26			
		NC				J2	J2	E3			
		NC				J25	J25	E4			
		NC				J26	J26	E5			
		NC				J5	J5	F23			
		NC				J6	J6	F24			
		NC				J7	J7	F5			
		NC				R18	R18	F6			
		NC				V1	V1	F7			
		NC				V2	V2	P19			
		NC				V21	V21	R10			
		NC				V22	V22				
		NC				V23	V23				
		NC				V24	V24				
		NC				V25	V25				
		NC				V26	V26				
		NC				V3	V3				
		NC				V4	V4				
		NC				W1	W1				
		NC				W19	W19				
		NC				W2	W2				
		NC				W20	W20				
		NC				W25	W25				
		NC				W26	W26				
		NC				W5	W5				
		NC				W6	W6				
		NC				W7	W7				
		NC				W8	W8				
		NC				Y7	Y7				

Pin Information For The Stratix™ EP1S20 Device, ver 3.6 (Note 2)

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F484	B672	F672	F780	DQS for x16	DQS for x32	DIFFIO Speed (1)
Note to Pin-List:											
1) The wire bond and flip-chip packages will have different data rates for the high speed differential I/O channels. The following table shows the data rates as supported for each package.											
2) Optional Functions (LVDS, DDR, Differential I/O, etc) are not available for some pins in certain packages. E.g. for EP1S20, DIFFIO_TX30 pair is available for package B672, F672 and F780 but not for F484.											

Package	Package Type	High Speed Differential I/O Channel Performance (DIFFIO Speed)		Units
		High	Low	
F484	flip chip	840	N/A	Mbps
B672	wire bond	462	N/A	Mbps
F672	wire bond	462	N/A	Mbps
F780	flip chip	840	N/A	Mbps

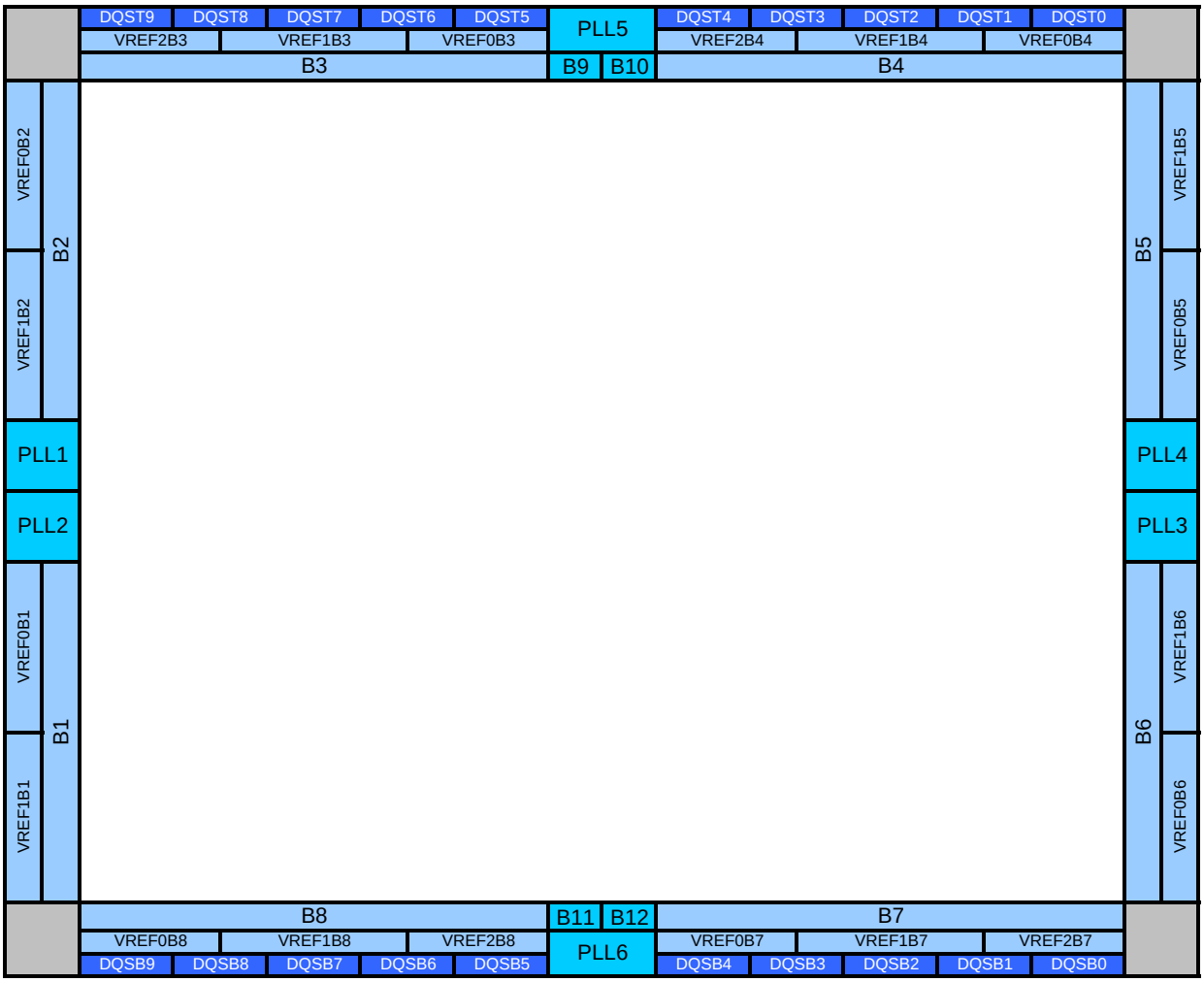
Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
		Supply and Reference Pins
VREF[1..4]B[1..8]	Input	Input reference voltage for bank 1. If a bank is used for a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank. If VREF pins are not used, designers should connect them to either VCC or Gnd.
VCCIO[1..8]	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O standards. VCCIO also supplies power to the input buffers used for the LVTTL, LVCMOS, 1.5-V, 1.8-V, 2.5-V, 3.3-V PCI, and 3.3-V PCI-X I/O standards.
VCCINT	Power	These are internal logic array voltage supply pins. VCCINT also supplies power to the input buffers used for the LVDS, LVPECL, 3.3-V PCML, HyperTransport™ technology, differential HSTL, GTL, GTL+, HSTL, SSTL, CTT, and 3.3-V AGP I/O standards.
VCC_PLL5_OUTA	Power	External clock output buffer power for PLL5 clock outputs PLL5_OUT[1..0]. The designer must connect this pin to the VCCIO of bank 9.
VCC_PLL5_OUTB	Power	External clock output buffer power for PLL5 clock outputs PLL5_OUT[3..2]. The designer must connect this pin to the VCCIO of bank 10.
VCC_PLL6_OUTA	Power	External clock output buffer power for PLL6 clock outputs PLL6_OUT[1..0]. The designer must connect this pin to the VCCIO of bank 11.
VCC_PLL6_OUTB	Power	External clock output buffer power for PLL6 clock outputs PLL6_OUT[3..2]. The designer must connect this pin to the VCCIO of bank 12.
VCCA_PLL[1..12]	Power	Analog power for PLLs[1..12]. The designer must connect this pin to 1.5 V, even if the PLL is not used.
GNDA_PLL[1..12]	Ground	Analog ground for PLLs[1..12]. The designer can connect this pin to the GND plane on the board.
VCCG_PLL[1..12]	Power	Guard ring power for PLLs[1..12]. The designer must connect this pin to 1.5 V, even if the PLL is not used.
GNDG_PLL[1..12]	Ground	Guard ring ground for PLLs[1..12]. The designer can connect this pin to the GND plane on the board.
NC	No Connect	Do not drive signals into these pins.
		Dedicated & Configuration/JTAG Pins
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration status pin; it is not available as a user I/O pin.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin; it is not available as a user I/O pin.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
nCONFIG	Input	Dedicated configuration control input. A low transition resets the target device; a low-to-high transition begins configuration. All I/O pins tri-state when nCONFIG is driven low.
DCLK	Input	Clock input used to clock configuration data from an external source into the Stratix device. This is a dedicated pin used for configuration.
nIO_PULLUP	Input	IF nIO_PULLUP is driven high during configuration, the weak pull-ups on all user I/O pins are disabled. If driven low, the weak pull-ups are enabled during configuration. nIO_PULLUP can be pulled up to either 1.5, 1.8, 2.5, or 3.3 V.
PORSEL	Input	Dedicated input pin used to select POR delay times of 2 ms or 100 ms during powerup. When PORSEL is connected to ground, the POR time is 100 ms. When PORSEL is connected to 3.3 V, the POR time is 2 ms.
VCCSEL	Input	VCCSEL is used to select which input buffer is used on all configuration pins. VCCSEL will control whether the 3.3-/2.5-V input buffer or the 1.8-/1.5-V input buffer is used. A "0" means 3.3/2.5 V and a "1" means 1.8-/1.5 V. At powerup, VCCSEL accepts 3.3V and 2.5V TTL Levels. VCCSEL affects the following pins: TDI, TMS, TCK, TRST, MSEL0, MSEL1, MSEL2, nCONFIG, nCE, DCLK, CONF_DONE, nSTATUS, and PLL_ENA.
nCE	Input	Active-low chip enables. Dedicated chip enable input used to detect which device is active in a chain of devices. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCEO	Output	Output that drives low when device configuration is complete. During multi-device configuration, this pin feeds a subsequent device's nCE pin.
TMS	Input	This is a dedicated JTAG input pin.
TDI	Input	This is a dedicated JTAG input pin.
TCK	Input	This is a dedicated JTAG input pin.
TDO	Output	This is a dedicated JTAG input pin.
TRST	Input	This is a dedicated JTAG input pin. Active low input, used to asynchronously reset the JTAG boundary scan circuit.
MSEL[2..0]	Input	Dedicated mode select control pins that set the configuration mode for the device.
TEMPDIODEp	Input	Pin used in conjunction with the temperature sensing diode (bias-high input) inside the Stratix device. If the temperature sensing diode is not used then connect this pin to GND.
TEMPDIODEn	Input	Pin used in conjunction with the temperature sensing diode (bias-low input) inside the Stratix device. If the temperature sensing diode is not used then connect this pin to GND.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
	Clock and PLL Pins	
PLL_ENA	Input	Dedicated input pin that drives the optional pllena port of all or a set of PLLs. If a PLL uses the pllena port, drive the PLL_ENA pin low to reset all PLLs including the counters to their default state. If VCCSEL = 0, then you must drive the PLL_ENA with a 3.3/2.5 V signal to enable the PLLs. If VCCSEL = 1, connect PLL_ENA to 1.8/1.5 V to enable the PLLs.
FCLK[7..0]	Bidirectional	Optional fast regional clock pins. FCLK pins can also be used as type input, output, or as bidirectional pins.
CLK[15..0]p	Input	Dedicated global clock inputs 0 to 15.
CLK[15..0]n	I/O, Input	Optional negative terminal input for differential global clock input.
PLL6_OUT[3..0]p	I/O, Output	Optional external clock outputs [3..0] from enhanced PLL 6. These pins can be differential (four output pin pairs) or single ended (eight clock outputs from PLL6).
PLL6_OUT[3..0]n	I/O, Output	Optional negative terminal for external clock outputs [3..0] from PLL6. If the clock outputs are single ended, then each pair of pins (i.e., PLL6_OUT0p and PLL6_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase.
PLL5_OUT[3..0]p	I/O, Output	Optional external clock outputs [3..0] from enhanced PLL 5. These pins can be differential (four output pin pairs) or single ended (eight clock outputs from PLL5).
PLL5_OUT[3..0]n	I/O, Output	Optional negative terminal for external clock outputs [3..0] from PLL 5. If the clock outputs are single ended, then each pair of pins (i.e., PLL5_OUT0p and PLL5_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase.
	Optional/Dual-Purpose Pins	
DATA0	I/O, Input	Dual-purpose configuration data input pin. Can be used as an I/O pin after configuration is complete.
DIFFIO_TX[0..65]p/n	I/O, TX channel	Dual-purpose differential transmitter channels. These channels can be used for transmitting LVDS or HyperTransport compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_RX[0..65]p/n	I/O, RX channel	Dual-purpose differential receiver channels. These channels can be used for receiving LVDS or HyperTransport compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
PLL5_FBp	I/O, Input	External feedback input pin for PLL5. This pin can be used as a user I/O pin if external feedback mode is not used.

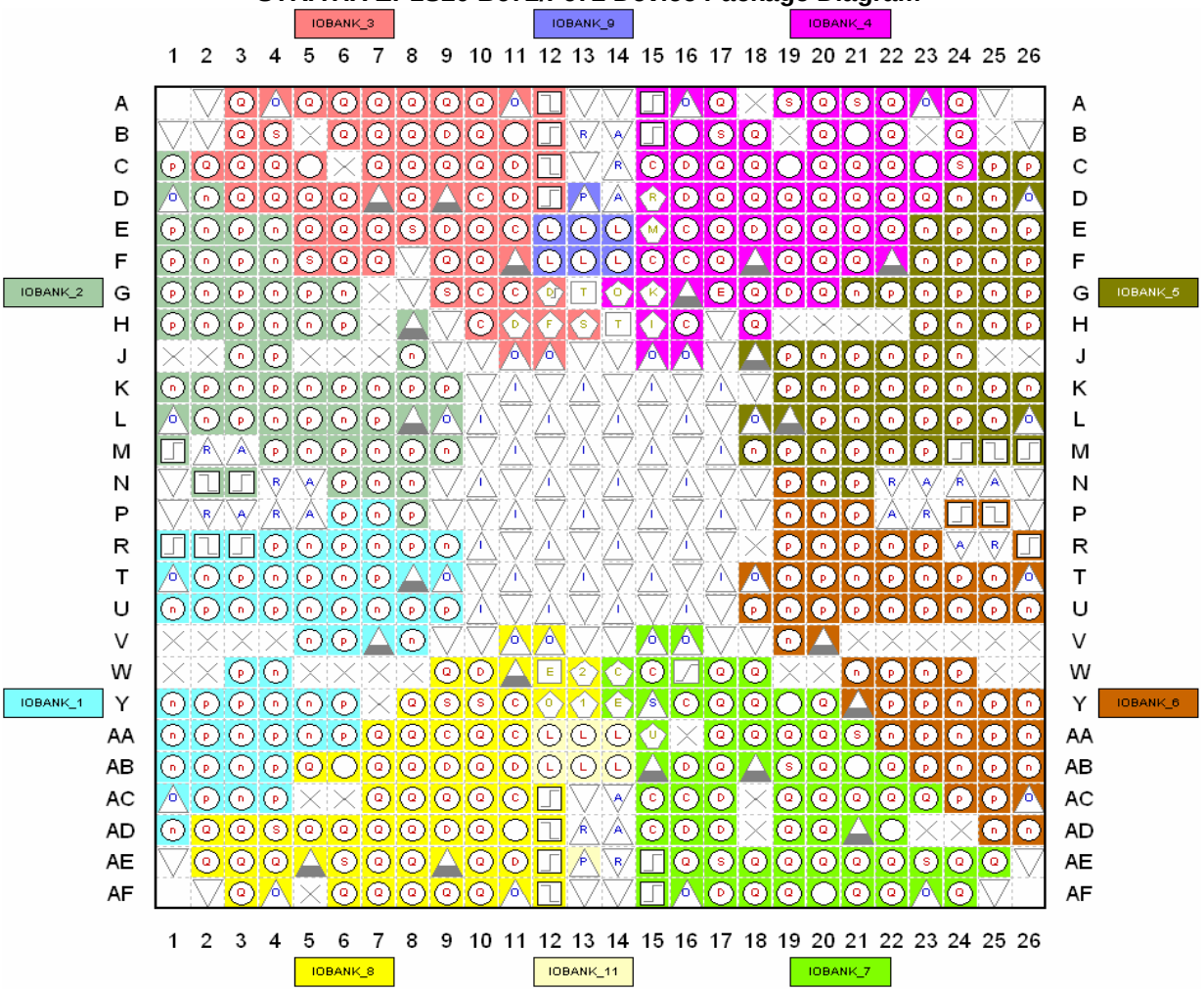
Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
PLL5_FBn	I/O, Input	Negative terminal input for external feedback input PLL5_FBp
PLL6_FBp	I/O, Input	External feedback input pin for PLL6
PLL6_FBn	I/O, Input	Negative terminal input for external feedback input PLL6_FBp
INIT_DONE	I/O, Output	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.
DATA[7..1]	I/O, Input	Dual-purpose configuration input data pins. These pins can be used for configuration or as regular I/O pins. These pins can also be used as user I/O pins after configuration.
nRS	I/O, Input	Read strobe input pin. This pin can be used as a user I/O pin after configuration.
DEV_CLRn	I/O, Input	Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as defined in the users design.
DEV_OE	I/O, Input	Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. This pin can be used as a user I/O pin after configuration.
RDYnBSY	I/O, Output	Ready not busy output. A high output indicates that the target device is ready to accept another data byte. A low output indicates that the target device is not ready to receive another data byte. This pin can be used as a user I/O pin after configuration
nCS,CS	I/O, Input	These are chip-select inputs that enable the Stratix device in the passive parallel asynchronous configuration mode. Drive nCS low and CS high to target a device for configuration. If a design requires an active high enable, use the CS pin and drive the nCS pin low. If a design requires an active low enable, use the nCS pin and drive the CS pin high. Configuration will be paused when either signal is inactive. Hold the nCS and CS pins active during configuration and initialization. The design can use these pins as user I/O pins after configuration.
nWS	I/O, Input	Active-low write strobe input to latch a byte of data on the DATA pins. This pin can be used as a user I/O pin after configuration.
PGM[2..0]	I/O, Output	These output pins control one of eight pages in the EPC16 configuration device when using remote update or local update configuration modes. When not using remote update or local update configuration modes, these pins are user I/O pins.
RUP[8..1]	I/O, Input	Reference pins for banks 8 to 1. The external precision resistors R_{UP} must be connected to the designated RUP pin on that I/O bank. If not required, these pins are regular I/O pins.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
RDN[8..1]	I/O, Input	Reference pins for banks 8 to 1. The external precision resistors R_{DN} must be connected to the designated RDN pin on that I/O bank. If not required, these pins are regular I/O pins.
RUnLU	I/O, Input	Input control pin to select remote update or local update modes. If MSEL2 = 1, this is a input control pin to select remote update (RUnLU =1) or local update (RUnLU =0) modes. If MSEL2=0, the RUnLU pin is a user I/O pin.
CRC_ERROR	I/O, Output	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled.

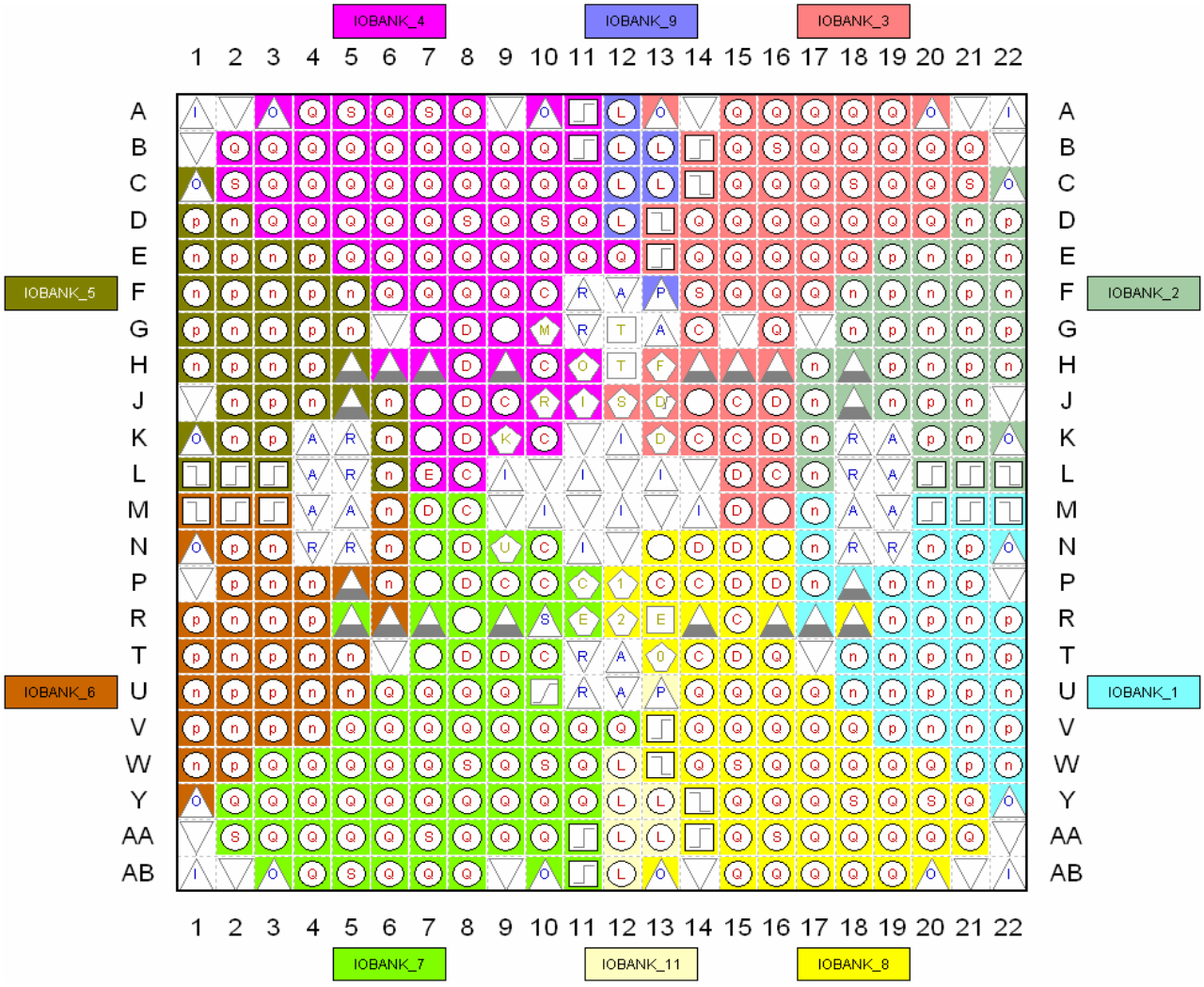


Notes:
1.This is a top view of the silicon die. The die is mounted up-side down in flip-chip packages and right-side up in wire-bond packages.
2.This is a pictoral representation only to get an idea of placement on the device. Refer to the pin-list and the Quartus II for exact locations.

STRATIX EP1S20 B672/F672 Device Package Diagram

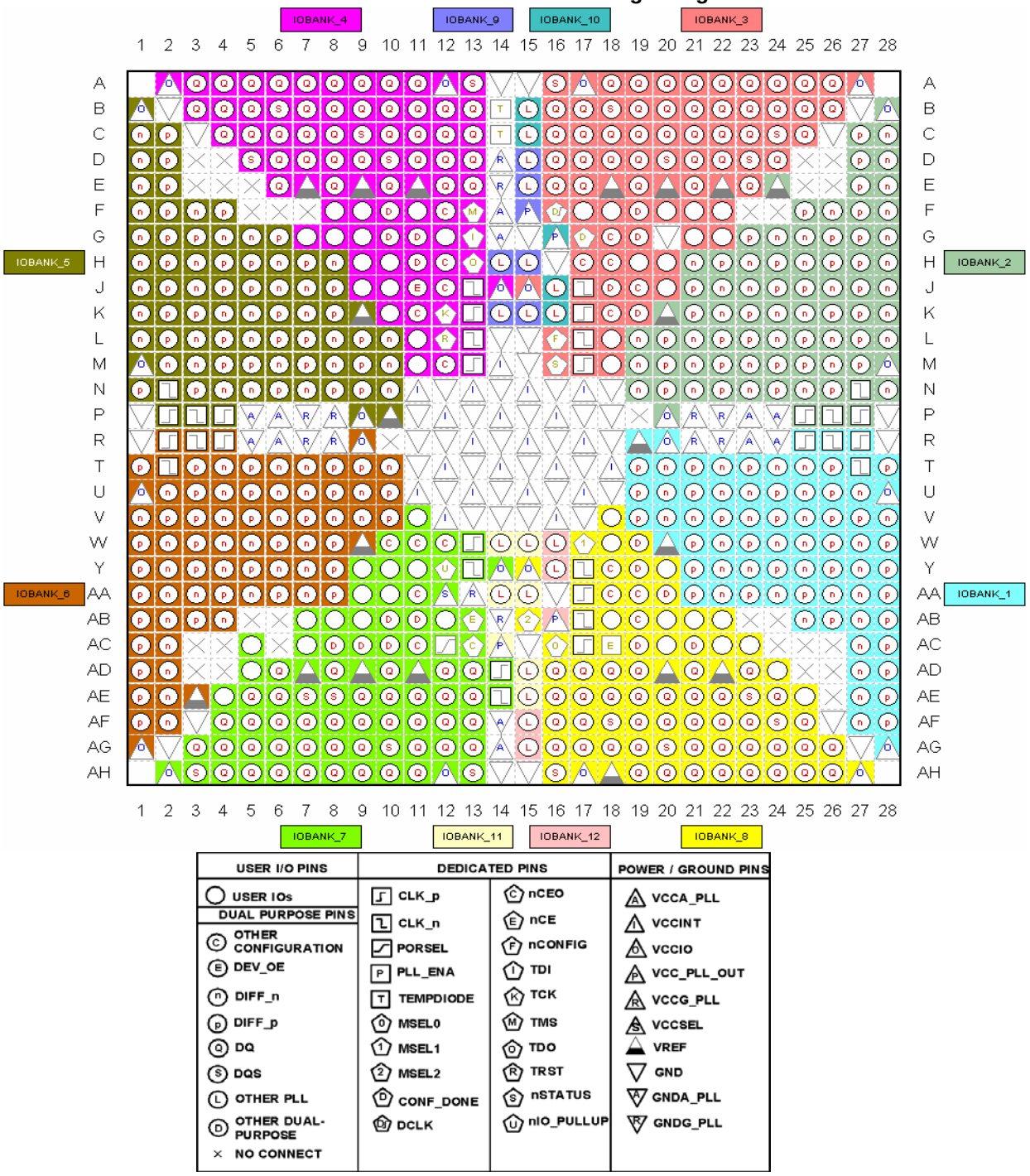


STRATIX EP1S20 F484 Device Package Diagram



USER I/O PINS	DEDICATED PINS		POWER / GROUND PINS
USER IOs	CLK_p	nCEO	VCCA_PLL
DUAL PURPOSE PINS	CLK_n	nCE	VCCINT
OTHER CONFIGURATION	PORSEL	nCONFIG	VCCIO
DEV_OE	PLL_ENA	TDI	VCC_PLL_OUT
DIFF_n	TEMPDIODE	TCK	VCCG_PLL
DIFF_p	MSEL0	TMS	VCCSEL
DQ	MSEL1	TDO	VREF
DQS	MSEL2	TRST	GND
OTHER PLL	CONF_DONE	nSTATUS	GNDA_PLL
OTHER DUAL-PURPOSE	DCLK	nIO_PULLUP	GNDG_PLL
NO CONNECT			

STRATIX EP1S20 F780 Device Package Diagram



Clock Resources for High Speed Differential I/O (DIFFIO) Receiver and Transmitter channels. *Notes (5),(7)*										
Device	**Pin Count**	**Source FAST PLL**	**Rx Channels** ***Note (1)***		**Tx channels** ***Note (2)***		**Total Rx Channels per PLL** ***Note (3)***		**Total Tx Channels per PLL** ***Note (4)***	
			High ***(6)***	**Low** ***(6)***	**High** ***(6)***	**Low** ***(6)***	**Direct** ***(8)***	**Cross Bank** ***(9)***	**Direct** ***(8)***	**Cross Bank** ***(9)***
EP1S20	484	PLL1	[17-19,25-26]	-	[16-17,20,23,27,32]	-	5	5	6	6
		PLL2	[6,10,12-14]	-	[0,5,10-11,14-15]	-	5	5	6	6
		PLL3	[51-53,55,59]	-	[50-51,54-55,60,65]	-	5	5	6	6
		PLL4	[39,40,46-48]	-	[33,38,42,45,48-49]	-	5	5	6	6
	672	PLL1	[17-19,21-23,25-26,28-32]	-	[16-17,20-23,27-32]	-	13	12	12	12
		PLL2	[0-4,6,8-10,12-14]	-	[0-5,8-11,14-15]	-	12	13	12	12
		PLL3	[51-53,55-57,59,61-65]	-	[50-51,54-57,60-65]	-	12	13	12	12
		PLL4	[33-37,39-40,42-44,46-48]	-	[33-38,42-45,48-49]	-	13	12	12	12
	780	PLL1	[16-32]	-	[16-32]	-	17	16	17	16
		PLL2	[0-15]	-	[0-15]	-	16	17	16	17
		PLL3	[50-65]	-	[50-65]	-	16	17	16	17
		PLL4	[33-49]	-	[33-49]	-	17	16	17	16

Notes:

1. These Rx channels can be clocked by the PLL listed in the "FAST PLL Source location" column.
2. These Tx channels can be clocked by the PLL listed in the "FAST PLL Source location" column.
3. This column shows the total number of Rx channels that can be driven by the PLL listed in the "FAST PLL Source location" column.
4. This column shows the total number of Tx channels that can be driven without by the PLL listed in the "FAST PLL Source location" column.
5. Each range of channel numbers are shown in [ ] brackets.
6. Data channels designated as "high" speed support a maximum data rate of 840 Mbps for -5 and -6 speed grade devices and 624 Mbps for -7 speed grade devices. Data channels designated as "low" speed support a maximum data rate of 462 Mbps for all speed grades.
7. The high speed differential I/O (DIFFIO) channels span across two banks on both sides of the device. Each Fast PLL can normally only feed channels in one bank. However, the center PLLs can also clock the channels associated with the adjacent center PLL on the same side of the device through a mux that is shown in figures 5-16 and 5-17 in volume 2 of the Stratix Device Handbook. These channels are called "cross-bank" channels. When cross-bank channels are used only one center PLL on each side can be used.
8. This column shows the total number of channels in one I/O bank that can be driven by the PLL listed in the "FAST PLL Source location" column.
9. This column shows the total number of cross-bank channels on the same side of the device that can be driven by the PLL the "FAST PLL Source location" column.

Revision History For The Stratix™ EP1S20 Device, ver 3.6

Version Number	Date	Changes Made
3.4	2/4/2005	Revised package diagrams.
3.5	10/20/2005	Update all package diagrams for EP1S20.
		Added footnote for pins that do not support Optional Functions (LVDS, DDR, etc)
3.6	3/2/2006	Added CRC_ERROR pin in Pin List and Pin Definition