FPGAs at 40 nm and >10 Gbps:
Jitter-, Signal Integrity-, Power-, and Process-
Optimized Transceivers

White Paper
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This paper describes key technologies that enable Stratix IV GT FPGAs to deliver the performance and capabilities necessary to support 40G/100G applications with integrated 11.3 Gbps transceivers. These include the LC-based oscillator and decision-feedback equalization (DFE) at 40 nm for ultra-low jitter FPGA transceivers. Furthermore, the transceiver architecture, including clocking and clock data recovery (CDR) technologies, are highlighted, as well as performance validation results.

Introduction

Technology advancement for the semiconductor industry largely follows Moore’s Law in that the number of transistors in an integrated circuit doubles roughly every two years, as well as demanding a higher data rate for communication links between devices or systems. Moore’s Law is facilitated by feature size or process node shrinkage, because smaller features enable more functionalities, higher operation speed, logic density, integration, and lower power consumption per logic function. A higher data rate often is achieved through advanced design methodologies and process technologies, and enables wireline and wireless communication, computer, storage, military, and broadcast electronic systems to send and receive large amounts of data to meet the ever-increasing data transfer or bandwidth demand.

The 65 nm process technology is found in the bulk of leading-edge products such as microprocessors and FPGAs. Leading-edge companies use the 45 nm or 40 nm process for their current products and the next process node for future products. The smaller feature size implies a smaller channel length for a transistor and shorter interconnects for a logic gate, resulting in faster switch time and shorter interconnect transport delay. The results of this process node shrinkage are favorable for logical operation, high density, and high-speed data transmission, as they are optimized for power-consumption efficiency.

Today, the data rates for most high-speed transceivers range from 5 to 6 Gbps for communication and I/O standards. Examples include CEI/Optical Internetworking Forum (OIF) 6G and 2X XAUI (6.25 Gbps) for network communication, PCI Express (PCIe) Gen1 (2.5 Gbps) and Gen2 (5 Gbps) for computer I/O buses, and Serial Advanced Technology Attachment (SATA) III/SAS II (6 Gbps) for storage area networks. The leading-edge and next-generation standards with data rates of 8 to 11 Gbps includes IEEE 10G Ethernet, IEEE 40G/100G Ethernet (802.3ba, 4X/10X 10.3125 Gbps), and CEI/OIF 11G for network communication, PCIe Gen3 (8.0 Gbps) for computer I/O buses, and Fibre Channel 8X (8.5 Gbps) for storage area networks.

Altera® Stratix® IV GT FPGAs are based on 40 nm technology. The core logic fabric has up to 530K logic elements (LEs), enabling large system-on-chip (SOC) FPGA designs and applications. The high-speed transceiver has a quad topology with an up-to-24-channel capacity supporting lane data rates up to 11.3 Gbps. In summary, Altera’s Stratix IV GT FPGAs deliver the highest density, the highest data rate, the highest
performance, and the lowest power. By leveraging the 40 nm benefits, including proven transceivers, memory interface, general-purpose I/Os, logical fabric, clocking networks, and soft and hard intellectual property (IP), Stratix IV GT FPGAs provide an unprecedented level of system capacity and bandwidth with superior signal integrity.

This white paper describes key technologies that enable Stratix IV GT FPGAs to deliver the performance and capabilities to support 40G/100G applications with integrated 11.3 Gbps transceivers.

- “Trends and Requirements for High-Speed Links” on page 3 covers the technology, market, and application trends, as well as requirements for high-speed transceivers. These include the new 10–11G high-speed I/O interface standards, such as IEEE 40G/100G (802.3ba, XLAUI (40G)/CAUI (100G) interface), SERDES Frame Interface Level 5 Phase 2 (SFI-5.2, CEI/OIF 11G interface), Scalable SERDES Framer interface (SFI-S, CEI/OIF 11G interface), Interlaken (CEI/OIF 6G and 11G interfaces), and 10G electrical-to-optical module interfaces (such as XFI and SFI interfaces).

- “40 nm Process Node and Transceiver” on page 8 covers the Stratix IV GT FPGAs’ capabilities and performance, and how these meet or exceed the technology and standards requirements.

- “Architectures” on page 10 covers the Stratix IV GT FPGAs’ important and unique capabilities, technology superiority, and performance metrics—including the high-speed link and transceiver process node—and architectures.

- “Mixed Signal Clock Recovery” on page 13 discusses the clock recovery circuit (CRC), and

- “End-to-End Equalization” on page 17 covers both transmitter and receiver equalizations.

- “Advanced Clock and Timing Generation” on page 33 covers the various types of oscillators, including both ring and LC based, along with their performance capabilities

- “Power and Jitter” on page 34 discusses built-in self-test jitter (BIST), noise, signal integrity, bit error rate (BER), power management and power integrity, precision timing-generation circuits, and supportability of high-speed standards.

- “Conclusion” on page 43 summarizes and concludes the paper.
Trends and Requirements for High-Speed Links

This section covers the general technology trends and requirements for high-speed I/O links, as well as focusing on the corresponding markets and applications.

Technology Trends and Challenges

As shown in Figure 1, the International Technology Roadmap (ITRS) states that both the single-lane data rate and the pin counts for I/Os in SOC-type integrated devices have increased since 2000, due to the ever-increasing demand for more bandwidth and higher data rates. According to the ITRS 2008 revision, most high-speed I/O interface data rates double every two to three years, with most at 5 to 6 Gbps in 2008. The predictions accurately reflect the reality of the high-speed I/O devices currently available on the market and historical data. These multiple-Gbps, high-speed I/O interfaces are used for

- Chip-to-chip, board-to-board, and system-to-system links
- Data communication and telecommunication networks: Gigabit Ethernet (GbE)
- OIF: SFI, Interlaken
- Computing I/Os: PCIe, Hypertransport
- Storage area networking (SAN): SATA, Fibre Channel
- Wireless networking (CPRI)
- Embedded processing: Serial RapidIO® (SRIO)

The next-generation I/O devices for most high-speed standards are expected to maintain data-rate growth similar to that of previous generations. Specifically, PCIe 3.0 (8.0 Gbps), Fibre Channel 8X (8.5 Gbps), IEEE Ethernet 40G/100G, and ITU OTN 40G/100G will emerge in the 2009-2010 time frame.
Most multiple-Gbps link transceivers use a serializer/deserializer (SERDES) to format/deformat and transfer/receive data bits. At the transmitter side, many parallel and low-speed (commonly a few hundred Mbps) coded data lines are multiplexed to a single lane at a much higher data rate (several Gbps). At the receiver side, data is received and processed in a reversal of the transmitted data. The received single-lane data first is recovered and then de-multiplexed to many parallel data lines, re-assembling the original data bits sent to the transmitter. Because of the higher single-lane data rate, the high-speed SERDES enables fewer I/O pins, channels, and associated channel materials compared to the low-speed synchronous parallel I/Os. Furthermore, the lane-to-lane skew is no longer a major issue for SERDES since each lane is self-timed and asynchronous to each other. The self-timing is achieved by using a CRC that not only recovers a clock, but also tracks low-frequency jitter.

As the data rate keeps increasing, the unit interval (UI) for the data bit decreases, due to their reciprocal relationship. The UI is the total timing budget available for the link, consisting of a minimum three components, which correspond to the transmitter, receiver, and channel subsystems. Most multiple-Gbps standards require a system BER be at $10^{-12}$ or lower (such as $10^{-15}$ or $10^{-17}$). If the UI decreases and the BER is unchanged, the jitter generated by the subsystems must be reduced accordingly. Meanwhile, for cost considerations, the PCB and backplane materials likely to be unchanged when the data rate increases. The same material means the same lossy physical characteristics, so the intersymbol interference (ISI) gets worse when a higher data rate signal propagates through the same channel material. The ISI manifests as a more closed eye diagram, corresponding to the increases in time jitter, amplitude
noise, and BER. Since the UI is fixed for a given data rate to maintain the same BER metric, either the ISI (caused by the channel) must be equalized or compensated, or the jitter (from the transmitter and receiver) must be reduced. Figure 2 shows what happens to the eye diagram when a high-speed signal propagates through a lossy channel.

**Figure 2. Signal and Eye-Diagram Properties Before and After a Lossy Channel at Multiple Gbps**

![Signal and Eye-Diagram Properties](image)

There are many different types of equalization. From the topology point of view, equalization may be implemented either at the transmitter, or the receiver, or both. From a signal and system point of view, equalization can be digital (such as finite impulse response (FIR) or infinite impulse response (IIR)) or analog (such as continuous time linear equalization (CTLE)), and linear or adaptive (such as decision-feedback equalization (DFE)). Each type of equalization has certain capabilities, advantages, and limitations. Using a better and intrinsically low noise/jitter component (such as a better oscillator), both transmitter and receiver jitter can be reduced. The Stratix IV GT equalization technology and its associated capabilities and advantages, as well as CRC and jitter tracking, are covered in more detail in the following sections.
I/O Protocol Standards Supported

Stratix IV GT FPGAs support data rates from 2.488 Gbps to 11.3 Gbps. Stratix IV GT FPGAs have dedicated hardware and IP to support a wide range of high-speed I/O standards, covering applications in the areas of wireline, wireless, computer storage, broadcast, military, test and measurement, and medical. Table 1 summarizes all the high-speed standards supported by Stratix IV GT FPGAs, of which a few new, emerging, and leading standards merit detailed discussions.

Table 1. High-Speed Protocol Standards Supported by Stratix IV GT FPGAs

<table>
<thead>
<tr>
<th>Protocol</th>
<th>Interface</th>
<th>Lanes per Side</th>
<th>Data Rate per Lane</th>
</tr>
</thead>
<tbody>
<tr>
<td>10G independent channels</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10 Gb Ethernet, 10 Gb Fibre Channel</td>
<td>XFI, SFI</td>
<td>1–12</td>
<td>9.9–11.3 Gbps</td>
</tr>
<tr>
<td>10G Basic (proprietary)</td>
<td>CEI-11G</td>
<td>1–12</td>
<td>9.9–11.3 Gbps</td>
</tr>
<tr>
<td>40G bonded channels</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Interlaken</td>
<td>CEI-6G</td>
<td>10</td>
<td>6.25 Gbps</td>
</tr>
<tr>
<td>Interlaken</td>
<td>CEI-11G</td>
<td>6</td>
<td>10.3125 Gbps</td>
</tr>
<tr>
<td>40G IEEE 802.3ba</td>
<td>XLAUI</td>
<td>4</td>
<td>10.3125 Gbps</td>
</tr>
<tr>
<td>SFI-4.2</td>
<td>SXI-5</td>
<td>5</td>
<td>2.488–3.125 Gbps</td>
</tr>
<tr>
<td>SFI-5.1</td>
<td>SXI-5</td>
<td>17</td>
<td>2.488–3.125 Gbps</td>
</tr>
<tr>
<td>SFI-5.2</td>
<td>CEI-11G</td>
<td>5</td>
<td>9.9–11.3 Gbps</td>
</tr>
<tr>
<td>SFI-S</td>
<td>CEI-11G</td>
<td>5</td>
<td>9.9–11.3 Gbps</td>
</tr>
<tr>
<td>SPAUI, DDR-XAUI</td>
<td>CEI-6G</td>
<td>4–6</td>
<td>6.4 Gbps</td>
</tr>
<tr>
<td>100G bonded channels</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Interlaken</td>
<td>CEI-6G</td>
<td>20</td>
<td>6.25 Gbps</td>
</tr>
<tr>
<td>Interlaken</td>
<td>CEI-11G</td>
<td>12</td>
<td>10.3125 Gbps</td>
</tr>
<tr>
<td>100G IEEE 802.3ba</td>
<td>CAUI</td>
<td>10</td>
<td>10.3125 Gbps</td>
</tr>
<tr>
<td>SFI-S</td>
<td>CEI-11G</td>
<td>11</td>
<td>9.9–11.3 Gbps</td>
</tr>
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40G/100G Ethernet

40G/100G Ethernet (IEEE 802.3ba) is intended to increase the Ethernet (802.3) data rate to 40 Gbps/100 Gbps (2). The 40G/100G standards are the Ethernet response to the increasing I/O bandwidth requirements driven by high-performance computing (such as server, computing-cluster, SAN, and network-attached storage (NAS)) and core-networking (such as switching, routing, data rate aggregating, internet exchanging). The two data rates are designed to serve appropriate applications of computing and networking. The 40G/100G standard objectives are achieved by defining new physical coding sublayers (PCSs), physical media attachments (PMAs), and physical medium dependents (PMDs), while maintaining the general architecture and medium access control (MAC) frame formatting of the basic 802.3 Ethernet. For PMA, the new chip-to-chip and chip-to-module interfaces of XLAUI (supporting 40G) and CAUI (supporting 100G) are under development. XLAUI is a 4X 10.3125 Gbps interface and CAUI is a 10X 10.3125 Gbps multiple-lane electrical interface, both with a nominal BER of 10⁻¹² and a formative BER of 10⁻¹⁵.
SFI
SFI-5.2 is a physical-layer interface between SERDES and framer devices developed by OIF \(^{(3)}\). SFI-5.2 has four data lanes with each running at 9.952 to 11.1 Gbps, plus a deskew lane. The objectives of SFI-5.2 is to provide a 40 Gbps aggregate data rate to support OC-768, STM-256, OTN OUT-3 of ITU, and other 40 Gbps applications. CEI/OIF-11G \(^{(3)}\) is used for the SFI-5.2 electrical specification. The BER sets for CEI/OIF are 10^{-15} for short reach (SR) and 10^{-12} for long reach (LR).

SFI-S is also a physical-layer interface between SERDES and framer devices, developed by OIF, which supports an aggregate data rate of 40 to 100 Gbps and beyond. SFI-S has 4 to 16 data lanes, with each running at 9.952 to 11.1 Gbps, plus 1 to 4 deskew lanes, all supporting a maximum aggregate data rate of up to 160 Gbps. The initial objective of SFI-S is to provide a 100 Gbps data rate to support 100G Ethernet (IEEE 802.3ba) and 100G optical networks (OTN OTU-4 under ITU). The CEI/OIF-11G interface is used for the SFI-S electrical specification.

Interlaken
Interlaken is a SERDES-based, chip-to-chip interface standard for packet-processor connections, which supports SERDES lane data rates up to 6.25 Gbps and 10.3125 Gbps \(^{(4)}\). The aggregate connection data rates supported by Interlaken range from 10 Gbps (5X 3.125 Gbps), 25 Gbps (5X 6.25 Gbps), 50 Gbps (10X 6.25 Gbps or 6X 10.3125 Gbps), to 100 Gbps (20X 6.25 Gbps or 12X 10.3125 Gbps). SERDES for Interlaken must comply with CEI/OIF-6G SR specifications if the per-lane data rate is 6.25 Gbps, and with the CEI/OIF-11G SR specification.

Optical Modules
Optical modules are used in communication and computer systems to convert electrical signals received to optical signals and then to drive them to optical fiber channels (viewed from the host receiver side). Similarly, they convert the optical signals to electrical signals and drive them to electrical copper channels (viewed from the host transmitter side).

XFI is an early 10G electrical interface between electrical transceivers and optical modules, supporting hot-pluggable XFP modules \(^{(5)}\). XFP modules are used for 10G Ethernet and 10G Fibre Channel. The XFP optical module is designed with a built-in retimer, for applications such as clock and data recovery (CDR), and a dispersion compensator, for applications such as electronic dispersion compensation (EDC). Therefore, the jitter requirements for the electrical transceiver at the other end of the interface are relatively relaxed.

SFP+ is a recently developed optical module standard that extends the SFP data rate to 10G, and SFI is the electrical interface standard between the electrical transceiver and the host SFP+ optical module \(^{(6)}\). An SFP module has a smaller form-factor size and power consumption compared to an XFP module. Furthermore, an SFP+ module (linear or limiting) does not have a re-timer or EDC insider the optical module. Because of this, the jitter requirement at the electrical transceiver side is relatively tight.
QSFP is the latest and most compact 4X 10G optical module, with a total module data rate of up to 40 Gbps. The CFP (100G (10X 10G) form-factor pluggable) optical module form-factor/mechanical specification was disclosed in OFC (March 2009) and its electrical specifications are covered by XLAUI/CAUI. Stratix IV GT FPGAs can be connected directly to 40G/100G optical modules such as QSFP and CFP to provide easy, efficient, and cost-effective interfaces with optical modules.

Having a 10+G and multiple-channel transceiver is a necessary requirement to support the 10+G single- and multiple-lane high-speed standards and associated interfaces. Together with the programmable logical elements, memory, and hard and soft IPs, Stratix IV GT FPGAs provide complete, comprehensive, high-performance, and cost-effective solutions in supporting these leading-edge standards.

40 nm Process Node and Transceiver

This section will give a high-level overview on process technology roadmap, challenges and solutions associated with deep-sub-micron (DSM) effects, and transceiver circuits for FPGAs at 40 nm.

For further information on DSM effects and transceiver circuits, refer to Altera at 40 nm: Jitter, Signal Integrity, Power, and Process Optimized.

Process Technology Roadmap

CMOS technology continues to evolve at the pace predicted by Moore’s Law, as demonstrated by the Taiwan Semiconductor Manufacturing Company (TSMC)’s technology roadmap in Figure 3.
CMOS scaling is driven mainly by digital applications such as memories and microprocessors, even though memories force high density and low power constraints, and microprocessors demand high performance and speed. This digital process is necessary because most ICs are, in fact, SOCs, which integrate the digital cores, memories, microprocessors or digital signal processors, I/Os and analog interface circuits such as A/D and D/A converters, phase-locked loops (PLLs), and transceivers. For most of these SOCs, digital circuits dominate the die area, hence the choice of technology. In addition, the general digital processes are offered earlier and cost less than the special RF and analog processes.

**Analog Challenges and Solutions as Process Nodes Shrink**

Analog design faces many new challenges—including headroom, gain, leakage, DSM effects and associated modeling, variations, and mismatches—as silicon continues to scale down. At 40 nm, these challenges can be overcome by using high supply voltage for analog blocks, non-nominal length (NML) and asymmetric devices, or analog devices for FPGAs.

**High Supply Voltage for Analog Blocks**

Analog design can be subdivided into two general categories, precision analog and high-speed analog. In general, for analog design, the ITRS proposes using different voltages and oxides than those used in digital logic. Higher voltages and thicker oxides are best suited for the precision analog category, while lower voltages and thin oxides are best for high-speed analog. Altera has used this dual-technology approach in analog design since the 130 nm technology node. Now, at 40 nm, it is essential to move more precision analog circuits to a higher voltage supply to solve the headroom issue.

**NML and Asymmetric Devices**

Analog circuits use non-nominal length (NML) transistors, which have more balanced Vt, Gm/Gds, linearity, and other relevant metrics. Transistors that have two to five times the minimum channel length commonly are used in mixed-signal design, a trend that was recognized in the 2005 edition of ITRS. As semiconductor companies move to mixed-signal formats, transistors are optimized for analog as well. Analog designs in deep sub-micron technology tend to be low voltage, so a combination of high Vt and low Vt transistors throughout a complex analog block is beneficial to the overall performance.

**Analog Devices for FPGAs**

To meet the increasing challenges of mixed-signal/analog design inside FPGA, Altera has designed analog transistors using the TSMC standard logic process. These analog transistors with specially tuned Vt levels, Gm/Gds, and mismatch characteristics successfully meet the analog design requirements. They are designed to ensure adequate Vt headroom for the analog operation at the power-supply voltage determined by logic operations in FPGA. The analog Vt headroom is designed to be a ratio of the power-supply voltage, which is needed to operate stacks of transistors typical of an analog design, such as the CMOS cascode current supply, and to maintain SNR integrity with low power.
During the engineering of these transistors, special attention was paid to ensure high gain and good mismatch behavior. Special channel implants are typically employed in an advanced logic process to control the short channel effects (SCE). These SCE control implants normally are optimized for the logic operation, not for analog. The analog transistors use optimized implants and analog parameters for the high-speed SERDES operation.

Architectures

This section reviews the mainstream multiple-Gbps link architectures, including the conventional data-driven architecture, the common-clock architecture, and Altera’s hybrid architecture. The advantages and limitations of each architecture also are discussed.

Data-Driven Architecture

The SERDES transceiver has emerged as the dominant transceiver for data rates above 1 Gbps. Earlier serial link architectures embedded the bit clock in the transmitting bitstream and relied on a receiver to recover the bit clock solely based on the incoming bitstream. Within the frame of the data-driven architecture (Figure 4), the CRC must recover both the frequency and phase of the clock from the received data. A PLL-type CRC meet these requirements because it can be used as a second- or higher-order system capable of simultaneously recovering both frequency and phase for the bit clock.

Figure 4. Conventional Data-Driven Serial Link Architecture
Data-driven architecture has many advantages, but the two most important are:

- **Simplicity**: there is no need to send a clock to the receiver along with the data
- **Good jitter tracking and tolerance capability**: the PLL CRC can be used as a second- or third-order system, corresponding to a 40 dB/decade or a 60 dB/decade jitter tracking/tolerance.

The implications of the first advantage are multiple folders, including easy testability, and a wide range of channel length reach, from chip-to-chip (≈1 m), to board-to-board (≈10 m), and system-to-system (≈ or >1 km). A wide-range channel reach corresponds to a wide range of transceiver applications. The second advantage implies a relatively larger low-frequency jitter budget for the transmitter, which enables a cost-effective transmitter design and the use of low-cost reference clocks. The drawbacks for the data-driven architectures with an analog PLL CRC include a relatively larger silicon area and a longer lock-in time. However, some limitations may be removed by using the hybrid digitally assisted PLL CRC, which is covered in “Altera’s Hybrid Architecture” on page 12.

### Common-Clock Architecture

The SERDES transceiver was first developed and used in network communications (such as GbE), and soon adopted by computer I/O communication interfaces (such as PCIe). Due to the short-distance reach requirement for computer I/Os (≈10 m), it is possible to send a low-frequency reference clock to both the transmitter and receiver, and then convert it to an in-rate clock for transmitting and receiving data through a multiplication PLL. With an in-rate clock at the receiver, the clock recovery only must recover the phase, making the use of a simple CRC possible, such as phase interpolator (PI) that is essentially a “bang-bang” phase detector. The PI determines whether the phase between the data and the clock is earlier or later and aligns them over a certain time period. Thus, the PI CRC is roughly equivalent to a first-order FIR.

The major advantages of the common-clock architecture\(^{(10)}\)\(^{(11)}\), illustrated in Figure 5, include:

- Maintenance of the phase correlation for the reference clocks used in the transmitter and receiver, enabling the use of a low-cost, relatively cheaper reference clock
- Shorter lock time since it is digital based

The drawbacks of the common-clock architecture include:

- Complex architecture requires both clock and data inputs for CRC
- Extra and complex test requirements
- Less (20 dB/decade) jitter tracking and tolerance capability for its receiver CRC
- Limited to short-reach computer I/O applications
Altera’s Hybrid Architecture

The Stratix IV GT architecture advances the conventional data-driven architecture by allowing two operational modes, as well as the ability to control the CRC digitally. The two operational modes are lock-to-data and lock-to-clock, and can be used automatically or manually. A common usage mode is to use the reference clock as the input and lock to the desired frequency, then switch the input to the data signal to lock to the phase. In the end, both frequency- and phase-aligned bit clocks are recovered. In addition to maintaining most of the advantages of the data-driven architecture, this hybrid architecture offers better lock time, power consumption optimization, and tolerance of jitter and transition density. A schematic drawing for this architecture is shown in Figure 6.

When compared to other link architectures, the hybrid architecture of Stratix IV GT FPGAs has advanced capabilities in filtering and reducing jitter from transmitter and reference clock, therefore enabling the best possible BER performance for the link system. In the hybrid architecture, the reference clock is used only in the initial training phase for CRC, and is not used in the actual data recovery phase. Therefore, reference clock jitter does not contribute to the system BER at all, leaving system designers a significant jitter margin for their system design. In contrast, the common-clock architecture uses the reference clock directly for both clock and data recovery, so...
the reference jitter contributes to the system BER and consumes system jitter budget. As for the conventional data-driven architecture, the CRC may never recover the bit clock or take a long time to lock on the incoming data when the receiver data input has excessive jitter, while hybrid architecture is largely immune from such problems since its frequency-locked bit clock is already in place when recovering the data.

In addition, because the hybrid architecture does not use a reference clock for data recovery, there is no need for the reference compliance test, which simplifies the system design and reduces the associated cost, while the reference-clock compliance test is required for the common-clock architecture.

Finally, due to its digitally assisted design, the hybrid architecture sets the bandwidths of clock generation PLL at the transmitter and the clock-recovery PLL at the receiver independently, so the receiver PLL CRC bandwidth is much wider than that of the transmitter PLL (as shown in Figure 7). Consequently, the transmitter’s high-frequency jitter is attenuated by its PLL, while the transmitter’s low-frequency jitter is attenuated by the receiver CRC, leaving a minimum jitter contribution in the system BER. In contrast, the common-clock architecture does not have the freedom to set the receiver PLL bandwidth wider than that of its transmitter PLL (13)(14), so jitter from transmitter contributes to the system BER.

Figure 7. Stratix IV GT PLL Bandwidth Setting Comparison for Hybrid and Common-Clock Architectures

<table>
<thead>
<tr>
<th>TXPLL BW</th>
<th>RXPLL BW</th>
<th>RXPLL will not be able to track jitter and noise from TXPLL in this region</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hybrid CDR</td>
<td>Extremely wide BW allows RXPLL track jitter and noise from TXPLL</td>
<td></td>
</tr>
</tbody>
</table>

**Mixed Signal Clock Recovery**

Clock recovery (14) is extremely important for a serial receiver. This section starts with a detailed review of the Stratix IV GT clock recovery subsystem architecture and working mechanisms, then covers capabilities, performance, and a comparison with other relevant clock recovery technologies.
Hybrid (Digitally Assisted) Clock Recovery

Stratix IV GT FPGAs use a hybrid clock-recovery architecture, shown in Figure 8, which is a mixture between an analog PLL-based CRC and a phase-interpolator-based CRC. In this architecture, the CRC receives both data and reference clocks. The CRC itself includes two fully integrated loops, which are PFD (lock-to-clock) and PD (lock-to-data) loops. They share a common charge pump (CP), loop filter (LF), and voltage-control oscillator (VCO). The PFD loop is equivalent to a normal PLL structure, and is used to train the PLL to a desired frequency by using the correct feedback counter value. The PD loop is used to align the PLL output clock frequency with incoming data.

Figure 8. Stratix IV GT Clock Recovery

The CRC always starts up using the PFD loop (or PFD mode). Once the CDR reaches the desired output frequency, the CRC automatically switches from the PFD loop to the PD loop so that it can track incoming data and generate the recovered clock quickly since frequency is recovered and locked at this time. Within the CRC, there is a parts-per-million (PPM) detection circuit that constantly checks the difference between recover clock and reference clock. If the CRC clock “drifts” too far from the desired frequency (as in case of excessive spread spectrum), the PPM detection circuit switches the CRC from the PD loop to the PFD loop so that the CDR output frequency is maintained. The Stratix IV GT CRC is also a design for power optimization. In order to reduce the power consumption, the CRC is implemented by using half-rate design in which the VCO frequency is half of the data transfer rate and both data and clock edges are used to sample incoming data.

Capability Comparisons

Each of the link architectures and associated CRCs has its own advantages and drawbacks, including jitter tolerance, design flexibility and area, transition density, run-length tolerance, and lock-time performance. It is important for system designers to understand the capabilities and limitations for the integrated devices so that appropriate design adjustments and tradeoffs are made to meet their system requirements.
Jitter Tolerance

Jitter tolerance measures how much jitter in the incoming data the receiver can tolerate without losing data. Jitter tolerance is closely related to jitter transfer function (JTF), which is governed by CRC properties, and is called for as a compliance test by many high-speed communication I/O standards. It is important for system designers to choose a receiver that meets or exceeds the standard requirement. For the hybrid PLL CRC discussed in “Architectures”, for example, the JTF is a second-order high-pass minimum with a 3 dB bandwidth at up to several 10 MHz. The hybrid PLL CRC tolerates a significant amount of jitter at low frequencies.

In contrast, for a PI-based CRC, the bandwidth depends on the number of integration steps (phases), the up and down counter settings, and a controller update rate. It is desirable to be able to generate as many steps as possible to achieve the necessary phase resolution, but this reduces the CDR bandwidth. Also discussed in “Architectures”, the PI-based CRC has a first-order high-pass JTF, with its 3 dB bandwidth typically at less than 10 MHz. Due to the limited jitter tolerance, a low-jitter and high-performance transmitter must design the link system that uses a PI CRC. Figure 9 compares the jitter tolerances of a PI CRC and a hybrid CRC.

Figure 9. Jitter Tolerance Comparison

Flexibility and Versatility

Most serial I/O link systems must support multiple lanes, which affects the clock and data signal input structure for the receiver. A PI CRC-based receiver normally uses a single PLL to support a multiple-channel operation, but this limits the system to only one standard and one data rate, unless more PLLs or a new clock distribution network is added. In contrast, in a hybrid CRC-based receiver, each channel has its own CRC.
and they are very independent of each other. Since each hybrid CRC in the multiple lane receiver is independent, each supports a different data rate in a different lane. This architecture provides system designers with the flexibility to support different standards and/or data rates simultaneously. Figure 10 compares the multi-channel signal and clock topologies of the PI and hybrid architectures.

**Figure 10. Multiple-Lane Signal Structure Comparison**

![Diagram of multiple-channel signal structures](image)

**Transition Density and Maximum Run Length**

All CRCs rely on some data transition to recover and maintain bit clock from the incoming data. A PI CRC maintains its recovered clock even if it does not receive any data transition for many UIs. This is because its clock is derived from the input clock phase, which is independent of the data signal. In general, analog CRCs have a lower tolerance with a maximum run length (MRL), which requires designers to either encode the data stream (with 8b/10b encoding, MRL = 5) or scrambled data (with PRBS 2⁻¹, MRL = 7) so it has a reasonable MRL and transition density to work without drifting away from the desired frequency. On average, the transition density is inversely proportional to the MRL. The hybrid CRC MRL capability is in the range of 500 to 1000 UIs, between analog PLL and PI CRCs and much longer than most of the MRLs defined by I/O standards.

**Lock Time**

Longer lock times cause latency and lower efficiency for the link system. A hybrid CRC, due to its two-mode operation capability, is able to lock quickly to the desired frequency and phase, so its lock time is shorter than the conventional analog PLL-based CRC.
End-to-End Equalization

This section covers the need and motivation for equalization, different equalization methods and their tradeoffs, and how the backplane influences the type of equalization chosen. The described architecture satisfies a continuous data rate from 2.5 to 11.3 Gbps, but proper equalization requires fine-tuning for each specific backplane. Supporting a host of customer backplanes requires thousands of settings, so adaptive equalization is necessary to tune for each unique backplane. Altera has a long history of best-in-class equalization solutions.

Motivation

As introduced in “Technology Trends and Challenges” on page 3, increases in the data rate lead to higher attenuation, reflections, and coupling. Chips are now so fast that when communicating through a backplane, they hit the bandwidth limitations of the wires. Figure 11 shows a diagram of a typical backplane, where the Tx device transmits a signal to Rx device. The goal is to deliver an electrical signal from Tx to Rx at as high a data rate as possible. As the transmitted signal leaves the Tx driver, it must go through the Tx I/O card traces, then an I/O card connector, the backplane traces, another connector for the Rx I/O card, and finally another set of I/O card traces at the Rx side. The bandwidth limitations of this system are a result of the I/O cards, connectors, and the backplane itself, which is over 40” of FR-4 material. The skin effect, dielectric loss in the wires as well as reflections caused by the vias, significantly distorts the signal from Tx to Rx. The bandwidth of the backplane wires typically ranges between several hundred MHz up to 2 GHz.

Figure 12 shows the frequency response of legacy XAUI, a subset of I/O standards for a 10G GbE backplane built for 3.125 Gbps signaling. Approximately 15 dB of attenuation occurs at three-quarters of the baud rate, or roughly 2.3 GHz. However, if the same legacy backplane is used for a 6.5 Gbps operation, over 30 dB of attenuation occurs.
Assuming the legacy XAUI backplane is used to communicate between Tx and Rx, Figure 13 illustrates various effects the Tx signal experiences. Initially, there is a good quality differential signal observed at point A, the near end in the link. As the signal propagates through the I/O cards, connectors, and backplanes, it is distorted by attenuation, reflections, radiation, and coupling. At point B, the far end in the link, a degraded version of the signal is launched from point A. In extreme cases, the signal at point B may so attenuated that the two differential signals do not even cross. This is true in long backplanes, where the incident signal degrades further, and for higher data rates in the same backplane, which experience higher degradation. These highly distorted signals still must be processed somehow.

Figure 13. Transmitted Signal Affected by a Transmission Medium

Incident => Attenuation + reflection + radiation + coupling
Support of legacy backplanes at increased data rates (beyond what they were originally intended for) is a cost-effective way to upgrade present systems. All that is required for a system upgrade is an I/O card replacement with new-generation high-data-rate transceivers capable of signal conditioning in legacy systems. Exotic backplane materials, which support increased data rates, are more expensive than conventional FR-4 material. Furthermore, replacement of the backplane may necessitate a costly overall system replacement, which is why system designers try to push as much bandwidth as possible with new silicon transceivers operating with legacy backplanes.

Figure 14 shows a 6.5 Gbps signal sent over the example XAUI backplane. The transmitted signal is so attenuated that no recognizable eye can be seen at the far end. The most practical solution to this dilemma is signal conditioning to open the eye before receiver samples the data, and on-chip equalization is the most practical way to compensate for the backplane attenuation.

**Equalization in a Nutshell**

The transmission medium is a linear system, which creates an inverse transfer function. When this inverse transfer function is added to the transfer function of the link, the goal is to have a resultant transfer function that is relatively “flat” up to the required frequency. Figure 15 shows this simplified concept in a frequency domain.
Figure 16 shows eye diagrams at three key points in the link. The first (left) is a launched signal from Tx. As this signal goes through the backplane, the resulting signal is attenuated (center). After the attenuated signal is sent through the equalizer, the original eye is restored (right).

Since the linear system is assumed, it is important to note that signal conditioning can be applied before or after the interconnect. In this example, the equalizer is placed at the far end, at the receiver. Similarly, the signal at Tx is pre-distorted so that after it goes through the interconnect, the resulting signal is clean for recovery at Rx. This type of signal conditioning is called “emphasis,” of which there are two types: pre-emphasis and de-emphasis. However, a complicating factor is that the link may not have a simple attenuation curve. There may be multiple poles in the transfer function, as well as reflections, crosstalk, and resonances at some frequencies. Therefore, it is important to choose the right equalization method from the wide variety of available signal-conditioning techniques.

Types of Signal Conditioning

There are many types of signal conditioning, or compensation/equalization, each of which has benefits and disadvantages. This section reviews some of the more popular implementations.

Transmit Pre-Emphasis/De-Emphasis

Transmit pre-emphasis/de-emphasis is implemented at the Tx driver by pre-conditioning the signal before it is launched into the channel so that the signal high-frequency contents are amplified (pre-emphasis) or the signal low-frequency contents are reduced. The benefit of this method is relative simplicity and low power. All of the sampled data is available at transmitting devices. Delayed versions of transmitted data are created easily to be one UI apart by placing a bank of registers that holds both prior and upcoming serial data bits. Similarly, fractional sampled data (1/2 UI) is available in Tx by taking information from the intermediate latch stages that commonly are used to create registers. Since both prior and upcoming (future) data bits are available, this signal conditioning technique addresses both pre- and post-cursor ISI.

Figure 17 demonstrates a block diagram for a possible pre-emphasis implementation. In general, transmit pre-emphasis is simple to implement since the design has “control” of the delays and clocking, in contrast to the receive side. The causal taps (post-taps) remove the post-cursor ISI, while the anti-causal taps (pre-taps) address the pre-cursor ISI.
The single pulse response in Figure 18 shows the time domain pre-emphasis response. It has pre-tap, followed by a main pulse and two post taps.

Figure 19 shows the pre-emphasis at the channel input and open-eye at the channel output, for the XLAUI/CAUI channel-defined 40G/100G D1.0 specification operating at 10.3125 Gbps.
The main disadvantages of signal conditioning on the Tx side is that it does not address crosstalk and is hard to make adaptive in real time. Tx pre-emphasis may even increase the amount of crosstalk in the system. Because the signal is pre-conditioned on the Tx side to have an excessive amount of high-frequency content, after it is lost to the lossy channel, the resulting signal has balanced high and low frequency. The consequence is that in multiple serial links systems, the increased high frequency content tends to escape into adjacent links, which causes crosstalk.

Real-time adaptation is a critical parameter to consider, specifically for link operations above 3 Gbps. The actual system signals are different even for identical launched signals at Tx, because at the Rx side, adjacent links receive different eye diagrams. For a system that relies on Tx for signal conditioning, a back channel must be created between each Rx and corresponding Tx to change the pre- and post taps of the driver to tailor it to the individual link.

**CTLE**

The continuous time linear equalizer (CTLE) is implemented on the receive side, so based on the equalization theory, the linear equalizer is well suited here. This simplifies the design, since non-sampled (that is, continuous time) implementation suffices. As a result, CTLE-based signal conditioning is usually the lowest power choice. Similar to transmit pre-emphasis, the CTLE addresses pre- and post-cursor ISI but in continuous time versus being limited to a pre-set number of Tx taps.
Figure 20 shows an example of a first-order CTLE transfer function. Zero is inserted to compensate the poles in channel transfer function (see Figure 12 on page 18). This simple implementation has a very low power consumption rate. Many equalizer stages can be added as given links required for a selected data rate. Multiple stages not only increase the order of the resulting equalizer but also increase the maximum boost achieved in a given frequency interval. (It is worthwhile to note that parasitic poles and their location should be carefully considered when designing a CTLE, but a detailed discussion of pole and zero placements is outside of the scope of this paper.)

**Figure 20. Example of a CTLE Transfer Function**

![CTLE Transfer Function Diagram]

Figure 21 uses the example from Figure 19, but with a CTLE. For the same near-end Tx signal, the far end shows an open eye when an internal CTLE is enabled. It is clear that the amount of crosstalk is not increased in a system with a CTLE versus Tx emphasis, because of the reduced high frequency content at the Tx drive. It is important to note that a system that has a CTLE is well suited for real-time adaptation, since the signal information after the channel is readily available for processing and reconditioning at Rx.

**Figure 21. FCTLE at Near End and Far End**

![FCTLE Diagram]
**TFIR**

The transversal FIR (TFIR) is also a non-sample-based discrete equalization, as shown in Figure 22. It is a linear system that addresses post-cursor ISI, but cannot deal with pre-cursor signal distortion unless additional delay is introduced to hold the prior data bit, as this information is not available at the time of signal processing. The requirement of a very accurately matched delay element is another major disadvantage for this approach for two reasons. First, the creation of absolute delays that are accurate is a challenging technical problem considering the device variations over large production quantities in addition to the normal process, voltage, and temperature (PVT) variations. Second, the creation of accurate delay elements restricts a design to a fixed frequency of operation that is inversely proportional to chosen delay. This is a major reason this approach is not found in multi-rate transceivers.

![Figure 22. Diagram of Unsampled Rx FIR](image)

**DFE**

Unlike prior equalization schemes, decision feedback equalization (DFE) is a non-linear system (see Figure 23). The generic DFE system must not only sample the data but also computes the new coefficient prior to the next sample. This makes timing closure extremely challenging. The DFE system requires a proper data sample, leading to increased design complexity of combined equalization and recover sections of the transceiver.

Furthermore, the issue of error propagation arises. The error propagation phenomenon is due to the fact that the present DFE decision is based on past samples. An error in the samples leads to an erroneous coefficient computation for the present data sample, with a single wrongfully captured bit propagating out to a few consecutive bits until correct samples are obtained again. Since the DFE system bases its decisions on prior bits, it only addresses post-cursor ISI and leaves the pre-cursor ISI uncompensated. As a result, a CTLE type of equalization still is required in a DFE system to accommodate the pre-cursor ISI.
The major benefit of DFE is improved immunity in the case of crosstalk, especially when it is assumed to be additive white Gaussian noise (AWGN). In the case of correlated crosstalk, DFE is not effective over a CTLE. The benefit of DFE in an AWGN system is understood by considering the signal-to-noise ratio (SNR) for cases of a CTLE and DFE. The system has predominately post-cursor ISI (since DFE does not address pre-cursor ISI). The SNR is computed as a ratio of the power of the signal to the power of the noise. Since the CTLE is continuous in time and does not really “know” or “need to know” the incoming signal spectral density, it boosts both signal and noise by equal amount. This, in effect, preserves the original link SNR.

The signal, unlike the AWGN, is limited in spectrum to the data rate and harmonics. In the case when DFE is used to equalize the signal, the SNR improves. This is because the DFE operates on sampled data, and not on the whole spectrum. Even though both signal and noise are present in the frequency spectrum of data and are boosted by DFE, boosting the fixed frequency spectrum improves the overall SNR because the power of noise is equally distributed over the whole spectrum, a key AWGN assumption. It is important to underscore the fairness of the AWGN assumption, where the first limit theorem of probability theory (also known as the Central Limit Theorem) simply states that with a large number of independent variables any process approaches normal distribution.

The DFE effectiveness in improving crosstalk is reduced when implementation difficulties are considered. As noted earlier, the timing closure is extremely difficult to meet. In many published high-speed applications, the first tap is not even available due to timing. As illustrated in Figure 24, the feedback loop timing is extremely tight. It is necessary to slice the bit, multiply by the coefficient, and sum it in 0.5 UI. At 10 Gbps, this is leaves 50 ps for the first successful tap operation. Additionally, the clock must be recovered from the serial datastream. It has its own jitter, resulting in further reduction of the available timing margin, and further complicating the design.
A DFE system is rather complex and hence requires a large amount of power. A general industry rule is 5 mW per Gbps of data per each DFE tap. For example, for 10 Gbps with five taps, DFE along would require 250 mW/ch.

**Backplanes and Their Impact on Equalization Selection**

Each link in a system has different characteristics due to many factors, such as the layer it is routed on, length of the route or neighboring signals, board material, etc. The designer must decide which equalization scheme is appropriate for the design, what topology will work best, and how much boost is needed.

**Backplanes and Equalization Selection**

In order to design the correct equalization scheme successfully, it is required to build a database of customer backplanes. Figure 25 shows an overview of this procedure. The critical characteristics of a backplane are extracted with a vector network analyzer (VNA). The extracted S-parameters then are put into a database that can be accessed by the various simulation tools, such as MATLAB, ADS, or hspicerf. Over the years, Altera has created an extensive database of customer backplanes, including those from popular connector vendors and large board manufacturers.
Backplane studies are performed on this internal database, with the attenuation curves analyzed by curve fitting and the different equalization schemes modeled. Simulations run on the database of backplanes determine the equalization order and the architecture required for the best fit.

Figure 26 shows the attenuation of the 40” XAUI legacy backplane used throughout this section, with third- and fourth-order pole functions also plotted. At 6.5 Gbps, a third-order function does a relatively good job of fitting the attenuation curve, while at 10 Gbps, a fourth-order function is required. Curve fitting with the number of poles tells the number of zeroes required in the equalization to undo the poles of the backplane. (High-level modeling is required to model the design exactly.) Once proven, the design is converted to a transistor-level implementation and simulated in the frequency and time domain against the database of extracted backplanes.
The few customer backplanes shown in Figure 27 have quite different attenuation characteristics, so the same equalization transfer curve will not fit all of these designs perfectly. An equalization scheme flexible enough to fit a majority of these curves must be developed.

Figure 27. Attenuation Curves of Sample Customer Backplanes
Analysis of the backplane database of up to 6.5 Gbps shows that all equalizer needs are supported by a maximum slope of 80 dB/dec. Hence, the receiver CTLE has a minimum requirement of four equalizer stages, each with a 20 dB/dec slope and independent control over zero placement, to achieve the overall required curve fit. Each stage contributes a zero in the transfer function. Additionally, each stage is controlled independently to allow tuning of the zero location as well as the slope of the boost. Lower EQ settings are available to prevent over-equalization for short-reach or chip-to-chip applications. Figure 28 shows a few of the over 1200 possible ranges of boost and possible slopes using this architecture.

Figure 28. Equalization Curves of 4-Stage CTLE

At the transmit side, a similar backplane study has revealed the need for one pre-tap to address pre-cursor ISI and two post-taps to compensate for post-cursor ISI. In addition, coefficients on all four taps are individually programmable, as well as signs of pre- and second-post-taps. Table 2 shows the available coefficients for taps, with the main tap shown as a \( V_{o,0} \) selection. This allows for over 2700 unique settings for the one \( V_{o,0} \) setting shown. As a result, a very competitive boost of between 15 and 500 percent is achieved.

Table 2. Available Pre-Emphasis Settings

<table>
<thead>
<tr>
<th>Level</th>
<th>( V_{o,0} ) (mV)</th>
<th>pre_tap</th>
<th>1st post</th>
<th>2nd post</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1000</td>
<td>0.025</td>
<td>0.05</td>
<td>0.025</td>
</tr>
<tr>
<td>2</td>
<td>1000</td>
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<td>0.11</td>
<td>0.05</td>
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<td>4</td>
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<td>0.1</td>
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<tr>
<td>5</td>
<td>1000</td>
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<td>0.27</td>
<td>0.125</td>
</tr>
<tr>
<td>6</td>
<td>1000</td>
<td>0.15</td>
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<td>12</td>
<td>1000</td>
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<td>0.61</td>
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</tr>
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</table>
Additionally, Altera Tx and Rx drivers and receivers are designed to support auto-calibration of the termination resistors. Nominally, the process variation of the resistor in deep sub-micron technologies is on the order of ±20 percent, but this does not take into account the additional variation of the active devices normally used to build termination cells. As a result, an uncalibrated termination cell could vary by over 30 percent due to PVT. Accurate termination resistors reduce reflected back energy, which improves the overall system margins.

An additional Tx feature worth mentioning is programmable slew rate control. The need for agile slew rate is clear from “Transmit Pre-Emphasis/De-Emphasis” on page 20. Reducing the high-frequency content of a transmitted signal edge until it most resembles sine-like edges for a given data rate goes a long way toward reducing the overall system crosstalk level and EMI.

The Need for Adaptive Equalization

One reason DFE is attractive is the assumed ability of the DFE engine to compute coefficients for incoming bits based on the history of received bits. In fact, for data rates above 3 Gbps, the adaptive equalization feature is a key differentiation worth looking for in transceiver vendor offerings. However, it is important to note that there is a clear difference between generic DFE with adaptive equalizers—electronic dispersion compensation (EDC) and adaptive dispersion compensation engine (ADCE)—and “programmable” DFE. The key difference is a real-time adaptation. Programmable DFE presumes prior knowledge of each given channel that must be programmed into the DFE coefficients. All others, like ADCE, compute coefficients in real time without any prior channel or data pattern knowledge, and as mentioned previously, above the 3 Gbps data rate, the number of programmable signal conditioning settings is very large.

System Development Stages

For every new system, four separate development stages (shown in Figure 29) can be identified:

1. **Vendor-selection stage**—The designer must choose a transceiver vendor that offers enough signal conditioning for all links in the system.

2. **Board-design stage**—The SI engineer must select the best setting for each link, often as the board layout is initiated, when new settings must be found rapidly.

3. **Board bring-up stage**—Each link must be activated in such a way so as to improve the overall system-level BER. Tradeoffs are made between the ability to drive an individual link perfectly versus overall system quality, once again iterating priority settings.

4. **In-system stage**—By looking at the system from a long-term perspective, the designer must considering whether the link characteristics will change with time and the environment.

Figure 29. System Development Flowchart
The first key observation is that throughout these four development stages, the designer must select the best setting out of the thousands available. As mentioned previously, one Tx V<sub>DD</sub> level has over 2700 unique settings and the Rx equalizer has over 1200 unique settings, so the task of choosing the optimal setting can be daunting, if not impractical. For the vendor selection and board design stages, Altera offers a fast-simulation, pre-emphasis equalization link estimator (PELE) that, given the link layout or extracted S-parameters, rapidly (within minutes) converges to a proper solution. However, the “board bring-up” and “in system” stages cannot be addressed via simulation, so hardware is required to automate this process.

To do so, Altera developed the ADCE hardware, which automatically and uniquely adapts to each link in the customer’s system. Regardless of the Tx pre-emphasis setting, the ADCE selects one of the available Rx CTLE settings. The adaptive engine has both one-time- and continuous-adaptation selections. One-time adaptation is intended for additional power savings, and is enabled during initial link training. However, the customer may enable it periodically either over predetermined time intervals or by observing degradation in the system BER over time. In this setting, power is used only during the adaptation process, as once convergence is detected, the CTLE settings are frozen. Continuous adaptation constantly monitors the link in mission mode without disturbing normal traffic. Equalization settings adapt to track not only link aging but also PVT variations on both sides of the link.

The goal of the ADCE is to make the system easy to use. Each link in the customer’s design has different characteristics, so the amount of equalization required varies with backplane length, type, data rate, aging, PVT, etc. The ADCE examines the output of all equalizer stages and adjusts the equalizer to increase or decrease the amount of equalization. Setting and forgetting may not be adequate for changing environments or aging (18).

Blind equalization, which means that no specific training pattern is required, is also one of the goals. However, the data must be DC balanced, and have reasonable transition density and run lengths. The ideal patterns would be similar to PRBS 2<sup>_n</sup>-1 or PRBS 2<sup>_n</sup>-1 patterns. This usually matches most customer applications very well, but for those customers with sub-optimal data patterns, a training pattern may still be used. In situations where an optimal solution cannot be found, the ability to read out ADCE values is provided inside the FPGA. These values are used as a starting point for manual adjustment.

The ADCE is controlled by a flexible state machine that allows changing the adaptation sequence as well as the maximum zero locations in the equalizer. The design also allows monitoring the link in real time during continuous adaptation or randomly enabled on the system level to gather link statistics in the field.

Figure 30 shows two eye diagrams after adaptively reaching a solution. Both eyes are open, but the second eye diagram would be closed without equalization. The first diagram is for a 12” trace, while the second diagram is for a 33” trace. Note that both output solutions are roughly the same quality even though the trace length is very different. The eye diagrams are measured after a diagnostic loopback path known to have bandwidth limitations. The actual quality of the eyes inside Rx is even better once measurement bandwidth deterioration is accounted for.
A Historical Overview of Altera’s Equalization Solutions

AnalogZone states, “The two biggest areas that differentiate [Altera’s] Stratix SERDES elements are in their … transceiver equalization technology they use to achieve better signal integrity, reach, and overall performance under real world conditions.” (19)

Altera has demonstrated successful FPGAs with transceivers at the 40 nm process node, qualifying this newly developed TSMC process for advanced analog needs. The 40 nm test chip was demonstrated to perform up to 11.3 Gbps at IEEE 40G/100G standard meetings (2). Altera has nearly a decade of SI experience and five different technology nodes of successful transceiver designs.

BI Oscilloscope

In Stratix IV GT FPGAs, the built-in (BI) oscilloscope feature provides in situ signal and jitter measurement capability at various signal nodes within the transceivers. This signal and jitter information cannot be measured by external equipment, yet it is very important for receiver equalization and clock recovery diagnostics and debug, as well as link characterization and verification. The functionality and performance of the BI oscilloscope are quite similar to those of an external instrument or a tester, without any additional cost. One of the BI oscilloscope’s capabilities is to measure and show the effective eye width of the equalized Rx data. This information not only can be used to monitor Rx signal conditions, but also to adjust the equalization amount and settings, a task that cannot be achieved with external equipment. Since the BI oscilloscope does not require any special or fixed data patterns, this feature is also very useful for system-level debugging in field and live data traffic watching. In short, the BI oscilloscope solves some emerging test, verification, characterization, and debug challenges on the Stratix IV GT FPGA transceiver that are not possible with external test and measurement equipment, and at a cost that is negligible compared to an equivalent lab oscilloscope.
Advanced Clock and Timing Generation

Clocking and timing generation play important roles in high-speed transceivers. Jitter is an important metric used to measure the quality of a clock, since clock jitter affects both transmitter and receiver jitter performance, in turn causing the BER to increase for the link system. (See “Power and Jitter” on page 34 for more details on jitter and noise.) On the transmitter side, the clock jitter limits the eye opening at its output. The clock jitter on the receiver side affects the receiver to latch on to the receiving data correctly, and consumes a portion of the total available jitter budget of the link (that is, 1 UI), leaving less jitter budget available for the transmitter and channel.

All clock generation and distribution circuits in a transceiver produce a certain amount of jitter. The clock generator normally uses PLL circuits. A key component of a PLL is the oscillator, which is the major source of jitter. Currently, there are two main types of oscillator used in multiple-GHz PLLs, ring oscillators and LC oscillators, each of which has advantages and shortfalls. Stratix IV GT FPGAs use both types of VCOs, providing a wide-range frequency coverage (2.5 Gbps to beyond 10 Gbps) and superior jitter performance (a few 100 fs RJ) at the same time.

Ring Oscillators

The ring oscillator is the most widely used VCO architecture due to its well-known design and performance in clock generation and clock recovery. To achieve high oscillating frequencies, the number of inverter stages must be minimized. A normal ring oscillator consists of at least three inverter stages, but some high-frequency oscillators have only two stages, which require adding carefully designed coupling for the extra phase shift. These 2-stage and 4-stage ring oscillators are widely used in transceiver designs as they provide quadrature outputs.

The voltage-control ring oscillator (VCRO) normally has a wide frequency tuning range (from 10–100 MHz to 1–12 GHz), which enables transceivers to accommodate many different data rates, but also results in very large gains. A high VCRO gain makes the PLL more sensitive to front-end noises and spurs. In addition, the ring oscillator is very sensitive to power supply and substrate noises. The VCRO phase noise or jitter is typically dominated by the supply noise injection if there is no high power-supply rejection ratio (PSRR) voltage regulator. Good substrate isolation also improves the phase noise/jitter of a ring oscillator.

In addition, the noise from switching devices and the biasing circuitry is the main contributor to the phase noise/jitter of a ring oscillator in a clean supply and substrate environment. Generally, minimizing the active device count, boosting the current, and removing the biasing circuitry improve the VCRO phase noise. Maintaining a symmetric waveform prevents 1/f noise upconversion and generally improves phase noise at the low end. However, the jitter improvement may not be due to the PLL shaping on the VCRO phase noise.

There are many different inverter structures—single-end, differential, pseudo-differential, etc.—used in ring oscillators, each with its own advantages and disadvantages. Details such as oscillating frequency, power consumption, and area must be taken into account in VCO designs. A well-designed ring oscillator enables a VCRO to achieve phase noise of -70 to -100 dBc/Hz at 1 MHz offset, depending on the oscillating frequencies. The phase noise/jitter of a ring oscillator degrades at higher
frequencies. For example, a 3 GHz (6 Gbps for sub-rate clock architecture) CMOS VCRO manufactured at the 40 nm node achieves a phase noise of -94 dBC/Hz at 1 MHz and a RMS jitter (1–80 MHz) at 1.08 ps. However, a 5.1 GHz (10.2 Gbps) VCRO at the same process node has a phase noise of -91 dBC/Hz at 1 MHz and a RMS jitter (1–80 MHz) at 920 fs.

**LC Oscillators**

The LC oscillator offers a superior phase noise performance due to its highly selective and high Q LC tank. Discrete LC oscillators have been existed in RF applications for long time, but integrating LC oscillators in mixed-signal IC became common only in recent years. There are two main factors driving LC oscillators to be used in integrated transceiver designs. The first is that ring oscillator phase noise has difficulties meeting the transmitter jitter requirements at a 10 GHz or larger frequency range. The second is that, due to the process’s feature size shrinkage, inductors are small enough to be integrated on a die as the LC oscillator frequency increases.

The cross-coupled LC oscillator is the most widely used architecture. The LC tank oscillates in either current mode or voltage mode. In the current mode, the signal amplitude is determined by a biased tail current. Although the waveform is immune to the supply variation, the tail current 1/f noise upconversion degrades its phase noise. In the voltage mode, there is no tail current and the amplitude is limited by supply voltage. A voltage regulator prevents supply noise and spur injection.

Compared to VCRO, VCLCO occupies more die area due to its bulky inductors. Unlike VCRO, integrated VCLCO has a very limited frequency-tuning range. The only tunable element of an on-chip LC oscillator is the varactor. (The tuning range of either diode or MOS varactor is very limited due to the current process technologies.) The continuous frequency tuning range of a VCLCO is typically around 20 percent. However, a VCLCO normally offers much better phase noise/jitter performance than a VCRO. For example, at 40 nm, a 3 GHz (6 Gbps) VCLCO has a phase noise of -110 dBC/Hz at 1 MHz offset and a RMS jitter of 640 fs (1–80 MHz), while a 5.1 GHz (10.2 Gbps) VCLCO has a phase noise of -106 dBC/Hz at 1 MHz offset and a RMS jitter of 520 fs (1–80 MHz).

For best-performance cross variations of PVT, the optimal tuning range for VCLCO is 9.9–11.3 Gbps, although the operational tuning range can be wider. The tuning range of VCRO is 2.5 Gbps to >11.3 Gbps, which is wider and faster than VCLCO, but has a larger jitter. For a given power and bandwidth, a VCLCO has superior jitter performance compared with VCRO. For a VCRO to match the performance of a VCLCO, the VCRO would have to consume a few hundred times the current of the VCLCO, which is not feasible.

Stratix IV GT FPGAs have both ring-based and LC-based VCOs, which provide a wide-range frequency coverage (2.5 Gbps to beyond 10 Gbps) and superior jitter performance (a few 100 fs RMS) at the same time.

**Power and Jitter**

Throughout industry literature, careful partition between digital and analog domains is emphasized to provide the isolation necessary to meet stringent analog jitter requirements.
Power Integrity

In the Stratix IV GT FPGA transceiver, the high-speed analog sections of the receive and transmit paths are separated. This is because the transceiver allows completely independent frequency selection on the Rx path from that chosen for the Tx path. Separated power supplies (V_{CCET} and V_{CCER} in Figure 31) prevent injection of uncorrelated noise sources. In addition, the clock path has its own power supply (V_{CCEL} in Figure 32), which is separated out to prevent noise injection from the data path into the transmitter clocking.

Figure 31. Power Domain Scheme in the Transceiver
The precision analog blocks, such as the bang gap, current bias, and on-chip voltage regulators, receive power from one dedicated $V_{CCEL}$ power supply. One chip voltage regulator isolates the sensitive circuitry of each Tx and Rx PLL, such as VCO, CP, and LF, as shown in Figure 33. The Tx driver in Figure 31 has its own power supply, $V_{CCET}$, which provides different power levels. Both on-chip and on-package de-coupling is used in the transceivers to provide necessary noise filtering from the external power supplies. Figure 34 shows the PSRR for the regulator-supporting CP and LP, and Figure 35 shows the regulator for VCO. Note that the PSRRs are below -50 dB in both cases for frequencies greater than 1 GHz.

**Figure 32. Power for Clock and Data Path in the Transmitter Path**

![Figure 32](image)

**Figure 33. Regulator for VCO/CP/LF in the Tx PLL and CDR**

![Figure 33](image)
Two important metrics for quantifying the performance of a transceiver are jitter and noise. Jitter commonly is defined as any deviation from ideal timings such as an ideal bit clock, and noise is commonly defined as any deviation from a reference voltage or power. Both excessive jitter and/or excessive noise increase the BER for the link system.
Jitter can be separated into deterministic jitter (DJ), which is bounded, and random jitter (RJ), which is unbounded. A jitter component hierarchy is shown in Figure 36.

**Figure 36. Jitter Components and Their Interrelationships**

DJ may include components of data-dependent jitter (DDJ), periodic jitter (PJ), and bounded-uncorrelated jitter (BUJ). DDJ is typically caused by band-limiting effects such as lossy channel. PJ is caused periodic modulation such as switch power-supply coupling, and BUJ is caused by crosstalk. DDJ may include components of ISI and duty-cycle distortion (DCD). ISI and DCD are the consequences of band-limiting effect, though DCD also may be caused by shifting of reference voltage. RJ is commonly caused by thermal noise and its distribution is best described by a Gaussian distribution.

A similar separation concept also can be applied to noise. The statistical properties for jitter and noise are described by a probability density function (PDF) best illustrated by an eye diagram, as shown in Figure 37.
Excessive jitter and/or noise increases the BER, in turn enhancing the chance of data samples falling within the compliance BER zone, resulting in a link failure. Thus, maintaining good jitter and noise performance is the key to achieve good BER performance for a link.

For more information on jitter and noise fundamentals, refer to Jitter, Noise, and Signal Integrity at High-Speed [17].

**Jitter and Noise Generation**

A good transmitter should generate a minimum amount of jitter and noise, which means that the eye diagram measured at the transmitter output should be wide open. Many high-speed I/O standards (such as XLAUI/CAUI of 40G/100G Ethernet, CEI/OIF, PCIe, Fibre Channel) define an eye mask to determine whether the jitter, noise, and signaling of the transmitter output comply with the requirement. The eye mask typically should correspond to a BER of $10^{-12}$ or lower. If no measurement data fall within the eye mask, then the transmitter jitter, noise, and signaling pass the requirements and the transmitter performance is assured.

Transmitter jitter largely depends on the jitter of the PLL that uses a VCO. Due to the advanced design and the use of both ring- and LC-based VCOs, the Stratix IV GT jitter and noise achieves superior performance. Figure 38 shows the Stratix IV GT transmitter (in ring-based VCO mode) jitter and eye-mask compliance test per XALUI/CAUI (10.3125 Gbps) requirement defined in the 40G/100G D1.0 specification [2]. The test pattern is a PRBS $2^{23}-1$, and the differential output voltage is at 600 mV. DJ ($δ$–$δ$, or dual Dirac) is 5.08 ps or 0.0524 UI, which is smaller than or exceeds the XLAUI/CAUI requirement of 16.5 ps or 0.17 UI. The RJ RMS is 1.46 ps or
0.0151 UI, and the TJ at BER = 10^{-12} is 25.6 ps or 0.264 UI, which is smaller than or exceeds the XLAUI/CAUI requirement of 31.03 ps or 0.32 UI. The RJ results are in line with the simulations. If the Stratix IV GT transmitter was in the LC-based VCO mode for this experiment, the RJ would be around 600 fs, and the TJ would be around 13.5 ps, which is almost half of the CALUI/CAUI jitter upper limit.

Figure 38. XLAUI/CAUI Transmitter Test Results From a Stratix IV GT FPGA

Stratix IV GT FPGA transceivers operate up to the 11.3 Gbps data rate. Figure 39 shows the transmitter eye diagram and corresponding jitter at 11.3 Gbps, with a PRBS 2^21 test pattern. The TJ is 19.94 ps (0.225 UI), the DJ is 9.79 ps (0.111 UI), and the RJ is 731 fs (8.26 mUI). The measurement was made when multiple transceiver channels were running.
Jitter and Noise Tolerance

While a good transmitter should generate a minimum amount of jitter and noise, a good receiver should be able to tolerate a minimum amount of jitter and noise. The two important receiver subsystems to test are the clock recovery and the equalization, such as CLTE and/or DFE. To verify whether a receiver CRC has the required jitter-tracking capability, a jitter frequency mask or tolerance mask is often defined by a standard. A jitter tolerance mask curve is the reciprocal of the jitter transfer function of the receiver. A receiver with a good CRC tolerates more jitter than it is required by a standard.

Stratix IV GT FPGAs, due to their innovative hybrid CRC design, have superior jitter tolerance capability. Figure 40 shows the worst eye-stressing receiver tolerance test per XLAUI/CAUI specification requirement. The test pattern is a PRBS $2^{21}-1$, and the eye-height of the input differential signal is only 60 mV, which exceeds the 90 mV specification requirement. The total non-equalizable jitter is larger than the 40.72 ps or 0.42 UI required by the specification, and the TJ exceeds the 60.12 ps or 0.62 UI required by the specification.
**Figure 41** shows the jitter tolerance performance for a Stratix IV GT receiver. The PRBS 2\(^{23}-1\) test-pattern results not only meet the receiver needs, but also exceed the XLAUI/CAUI specifications. If other parts of the link subsystems (such as transmitter and channel) also meet the specification requirements, a receiver better than the specification implies that links built with Stratix IV GT FPGAs have a better (lower) BER than 10\(^{-12}\).

**Figure 41.** XLAUI/CAUI Receiver Jitter Tolerance Compliance Results From a Stratix IV GT FPGA

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**Overall System BER**

BER is a system metric for a link. Thus, BER is tightly coupled with the link system architecture and subsystem performances. A quantitative and accurate system model and understanding is essential for estimating or measuring the system’s BER. The BER for a subsystem may also be defined if the rest of the characteristics of the link system are defined or assumed\(^{(17)}\)\(^{(20)}\).

The BER can be caused by jitter, noise, or both. By definition, the BER is the sum of integrations of PDFs of jitter and noise, manifesting two-dimensional characteristics for such performance metrics. Accordingly, the BER is a cumulative distribution function (CDF). For simplicity, the BER is often estimated and viewed as a function of sampling time at a given reference voltage (such as at zero crossing or 50 percent swing level), or as a function of sampling voltage at a given reference time location (such as at the center of the UI data cell). **Figure 42** shows an eye diagram with the jitter PDF at the zero-crossing level and the BER as a function of sampling time (often called a bathtub curve).
The overall link system BER depends on the jitter, noise, and signaling performances of its subsystems, such as transmitter, channel, and receiver. Due to Altera’s innovative designs in system and subsystem architecture, clock recovery, equalization, power and power integrity, the use of the latest 40 nm process technology for fabrication, and its jitter, noise, and power consumption, the transceiver meets or exceeds the requirements posed by various high-speed I/O standards. Due to the excess margins in jitter and noise, it also enables its users to design systems with lower cost and/or better BER system performance (such as $10^{-15}$).

**Conclusion**

In reviewing the technology trends and associated challenging requirements for high-speed links and transceivers, the challenges range from data rate increases, process node decreases, and optimal power consumption, to stringent performance requirements for jitter, noise, power integrity, and BER, and supportability of various multiple-Gbps high-speed I/O standards. Altera’s Stratix IV GT FPGAs enhanced with transceivers meet and/or exceed those challenges and requirements using 40 nm design and fabrication, innovative hybrid-transceiver architecture, hybrid and mixed-signal clock recovery, complete end-to-end equalizations, and design and use of an ultra-low noise/jitter LC-based oscillator, and BI oscilloscope. The 40 nm process technology allows Stratix IV GT FPGAs to achieve the best possible logical density, memory speed, and capacity, while the transceiver innovations enable superior jitter, noise, signal integrity, and BER performances at the minimum or optimized power.

Stratix IV GT FPGAs provide the density, features, and performance advantages with integrated 11.3 Gbps transceivers. These enable the optimal system integration of 40G/100G applications with the time-to-market advantage of the programmable fabric. Bridging applications requiring maximum bandwidth also benefit from this device. Stratix IV GT devices can connect directly to 40G/100G optical modules, which, overall, enable the lowest system cost and system power with the least board complexity.
New circuits and IP are added to enable Stratix IV GT FPGAs to support leading-edge or emerging standards of IEEE 40G/100G (802.3ba, XLAUI (40G)/CAUI (100G) interface), SERDES Frame Interface Level 5 Phase 2 (SFI-5.2 and CEI/OIF 11G interface), Scalable SERDES Framer Interface (SFI-S and CEI/OIF 11G interface), Interlaken (CEI/OIF 6 G and 11G interfaces), and 10G electrical-to-optical module interfaces (XFI and SFI interfaces). The general-purpose, scalable, and programmable design permits Stratix IV GT FPGAs to support the high-speed link standards to 10 Gbps and beyond.

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## Acknowledgements

- Daniel Chow, Senior Member of Technical Staff, Product Engineering, Altera Corporation
- Weichi Ding, Design Manager, Analog Design Group, Altera Corporation
- Bernhard Friebe, Product Marketing Manager, High-End FPGA Products, Altera Corporation
- Tim Hoang, IC Design Manager, Analog Design Group, Altera Corporation
- Mike Peng Li, Ph.D., Principle Architect/Distinguished Engineer, Product Engineering, Altera Corporation
- Sergey Shumareyev, Director of Engineering, Analog Design Group, Altera Corporation
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## Document Revision History

Table 3 shows the revision history for this document.

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